Data Sheet | January 14, 2014 | FN6236.5

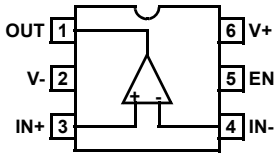
Ultra-Small, 330nA and 1µA Single Supply, Rail-to-Rail Input/Output (RRIO) Op Amps

The ISL28194 is micropower op amps optimized for low-power applications. The part is designed for single-supply operation from 1.8V to 5.5V, making it suitable for applications with two 1.5V alkaline batteries. The ISL28194 consumes typically 330nA of supply current . The part feature rail-to-rail input and output swing (RRIO), allowing for maximum battery usage.

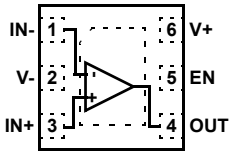
Equipped with a shutdown pin, the part draw typically 2nA when off. The combination of small footprint, low power, single supply, and rail-to-rail operation makes it ideally suited for all battery operated device.

Pinouts

ISL28194
(6 LD SOT-23)
TOP VIEW



ISL28194
(6 LD 1.6X1.6X0.5 UTDFN)
TOP VIEW



Features

- Typical Supply Current 330nA
- Ultra-Low Single-Supply Operation Down to +1.8V
- Rail-to-Rail Input/Output Voltage Range (RRIO)
- Maximum 2mV Offset Voltage
- Maximum 60pA Input Bias Current
- 3.5kHz Gain Bandwidth Product
- ENABLE Pin Feature
- -40°C to +125°C Operation
- Pb-Free (RoHS Compliant)

Applications

- 2-Cell Alkaline Battery-Powered/Portable Systems
- Window Comparators
- Threshold Detectors/Discriminators
- Mobile Communications
- Low Power Sensors

Ordering Information

PART NUMBER (Note 1)	PART MARKING	PACKAGE Tape and Reel (Pb-Free)	PKG. DWG. #
ISL28194FHZ-T7 (Note 2)	GABK (Note 4)	6 Ld SOT-23	P6.064A
ISL28194FRUZ-T7 (Note 3)	M3	6 Ld 1.6x1.6x0.5 UTDFN	L6.1.6x1.6A
ISL28194EVAL1Z	Evaluation Board		

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. The part marking is located on the bottom of the part.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_+, V_-) 5.75V
Supply Turn On Voltage Slew Rate 1V/µs
Differential Input Current 5mA
Differential Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD Rating
Human Body Model 3kV
Machine Model 300V

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
6 Ld SOT-23	230
6 Ld UTDFN	118

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, T_A = +25°C, Unless Otherwise Specified.
Boldface limits apply over -40°C to +125°C.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OS}	Input Offset Voltage		-2 **-2.5**	-0.1	2 **2.5**	mV mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage vs Temperature			1.5		µV/°C
I_{OS}	Input Offset Current		-60 **-100**	10	60 **100**	pA pA
I_B	Input Bias Current		-80 **-150**	15	80 **150**	pA pA
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz		10		μV_{P-P}
	Input Noise Voltage Density	f_o = 100Hz		265		nV/√Hz
i_N	Input Noise Current Density	f_o = 100Hz		0.7		pA/√Hz
CMIR	Common Mode Input Range	Established by CMRR test	**0**		**5**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.5V to 3.5V	70 **70**	100		dB
		V_{CM} = 0V to 5V	55	90		dB
PSRR	Power Supply Rejection Ratio	V_+ = 1.8V to 5.5V	70 **70**	100		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 3.5V, R_L = 100kΩ, R_L = 10kΩ	75	115		dB
V_{OUT}	Maximum Output Voltage Swing R_L terminated to V_+/2	Output low, R_L = 100kΩ		25	40	mV
		Output low, R_L = 10kΩ		50	70	mV
		Output high, R_L = 100kΩ	4.96	4.975		V
		Output high, R_L = 10kΩ	4.93	4.94		V
SR	Slew Rate	±1.5V, A_V = 2		1.2		V/ms
GBW	Gain Bandwidth Product	A_V = 101; R_L = 10kΩ		3.5		kHz
$I_{S,ON}$	Supply Current, Enabled			330	450 **500**	nA
$I_{S,OFF}$	Supply Current, Disabled	EN = 0.4V		2	20 **50**	nA nA
I_{SC}+	Short Circuit Sourcing Capability	R_L = 10Ω	9	11		mA

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, T_A = +25°C, Unless Otherwise Specified.
Boldface limits apply over -40°C to +125°C. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_{SC^-}	Short Circuit Sinking Capability R_L terminated to V+/2	R_L = 10Ω	11	12		mA
V_+	Supply Voltage Range		1.8		5.5	V
ENABLE INPUT						
V_{INH}	Enable Pin High Level		(V+)x(0.8)			V
V_{INL}	Enable Pin Low Level				0.4	V
I_{ENH}	Enable Pin Input Current	V_{EN} = 5V		30	150 **200**	nA
I_{ENL}	Enable Pin Input Current	V_{EN} = 0V		30	150 **200**	nA

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, Unless Otherwise Specified.

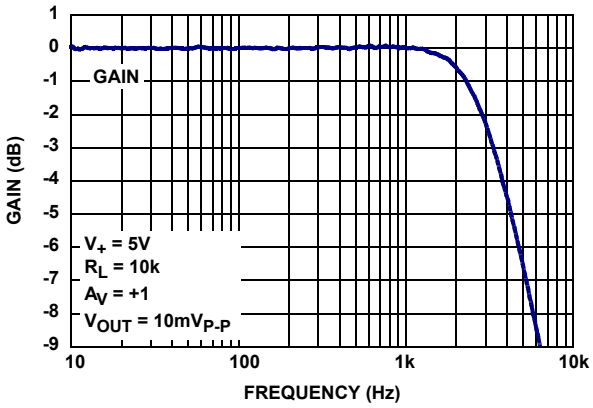


FIGURE 1. CLOSE LOOP GAIN vs FREQUENCY

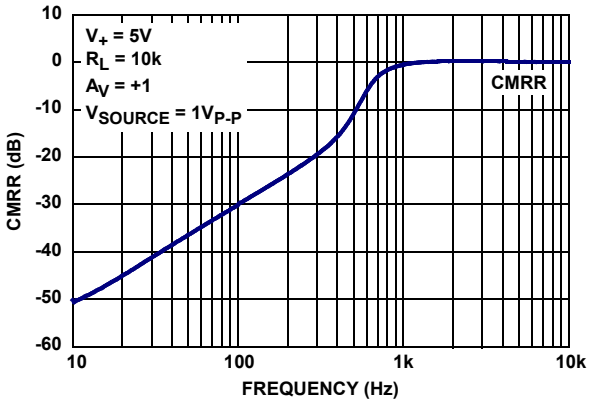


FIGURE 2. CMRR vs FREQUENCY

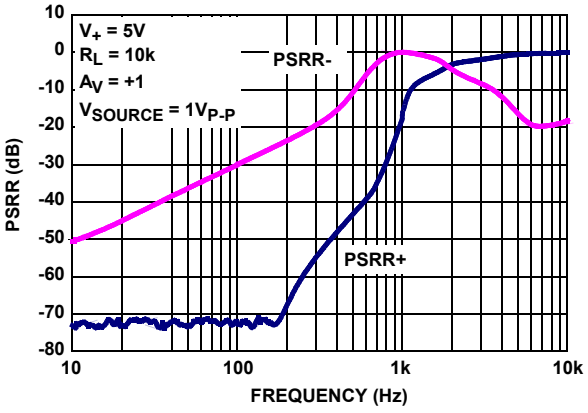


FIGURE 3. PSRR vs FREQUENCY

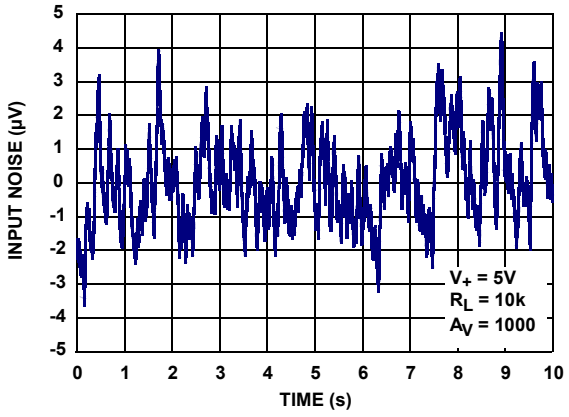


FIGURE 4. 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, Unless Otherwise Specified. **(Continued)**

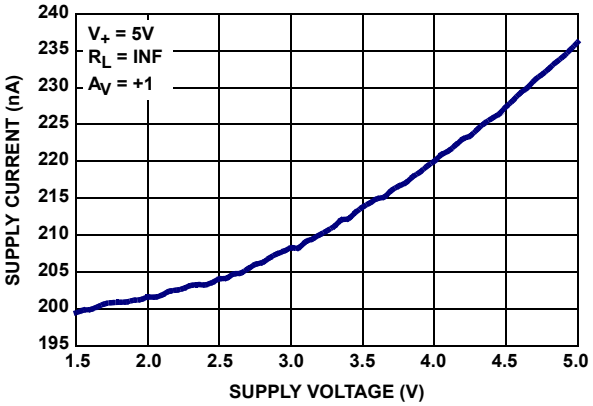


FIGURE 5. SUPPLY CURRENT vs SUPPLY VOLTAGE

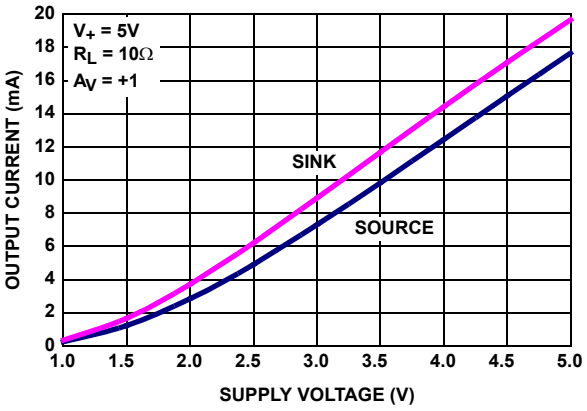


FIGURE 6. OUTPUT SHORT CIRCUIT CURRENT

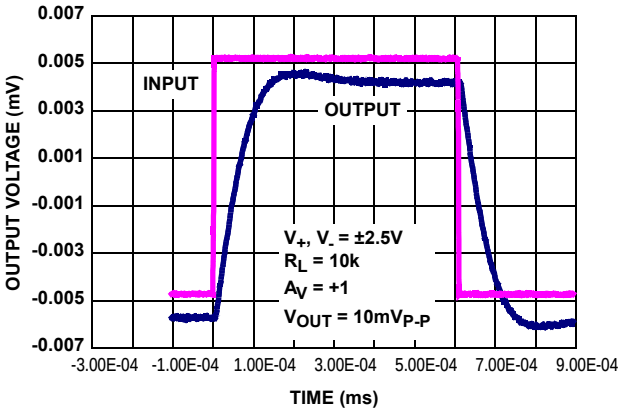


FIGURE 7. SMALL SIGNAL TRANSIENT RESPONSE

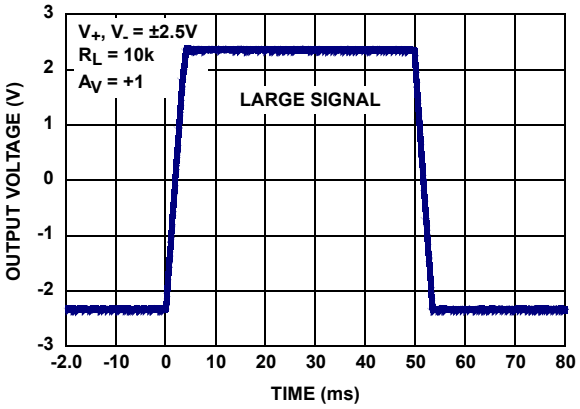


FIGURE 8. LARGE SIGNAL TRANSIENT RESPONSE

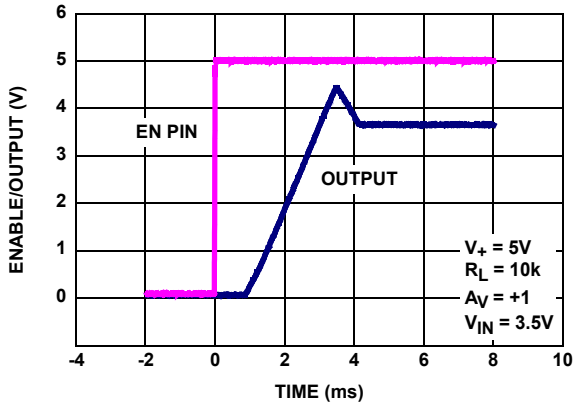


FIGURE 9. ENABLE TO OUTPUT DELAY TIME

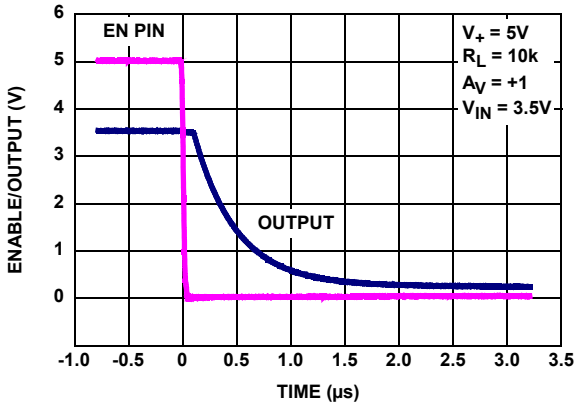


FIGURE 10. DISABLE TO OUTPUT DELAY TIME

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, Unless Otherwise Specified. **(Continued)**

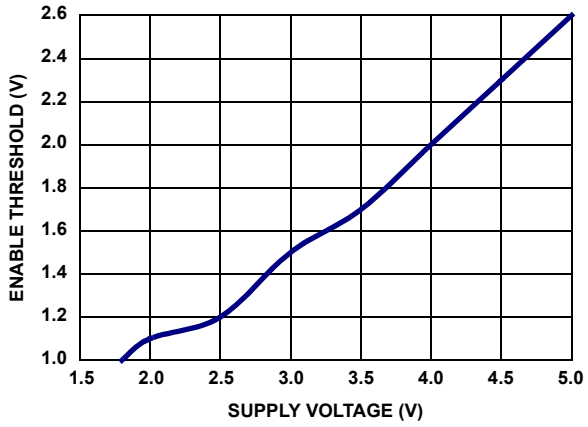


FIGURE 11. ENABLE THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

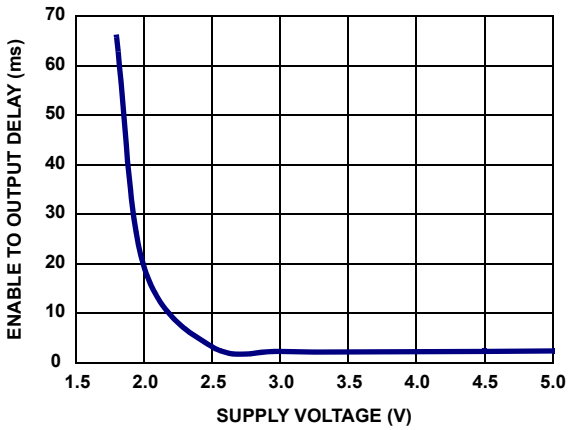


FIGURE 12. ENABLE TO OUTPUT DELAY TIME vs SUPPLY VOLTAGE

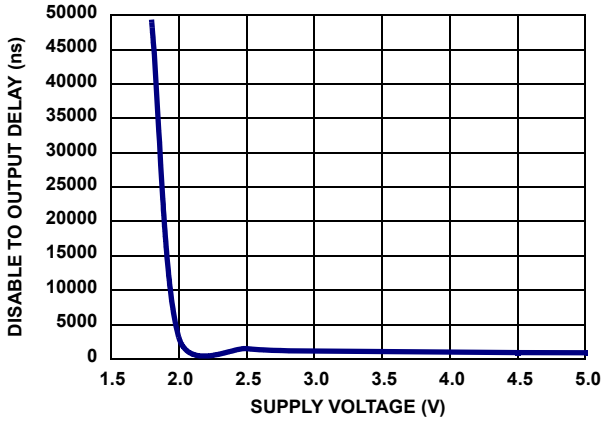


FIGURE 13. ENABLE LOW TO OUTPUT TURN-OFF TIME vs SUPPLY VOLTAGE

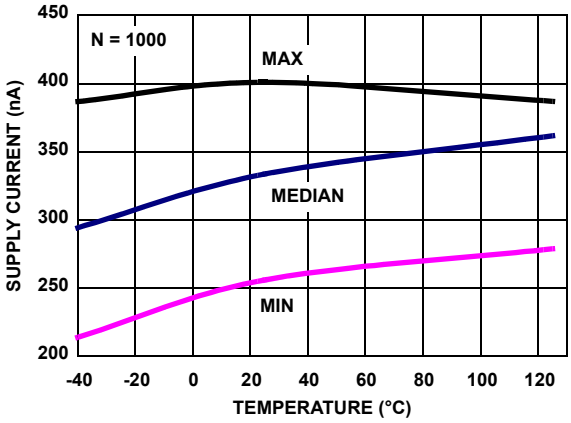


FIGURE 14. SUPPLY CURRENT ENABLED vs TEMPERATURE, $V_+ = 5V$, $V_- = 0V$

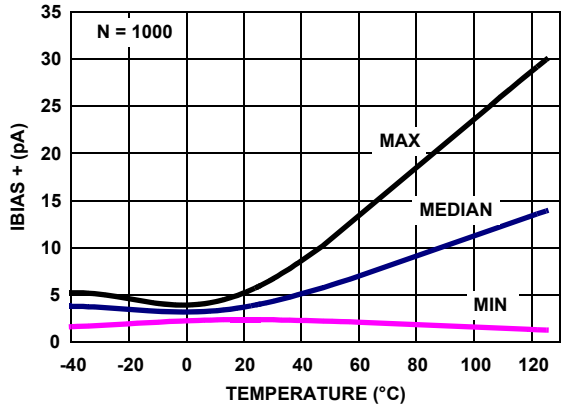


FIGURE 15. IBIAS + vs TEMPERATURE $V_+ = 5V$

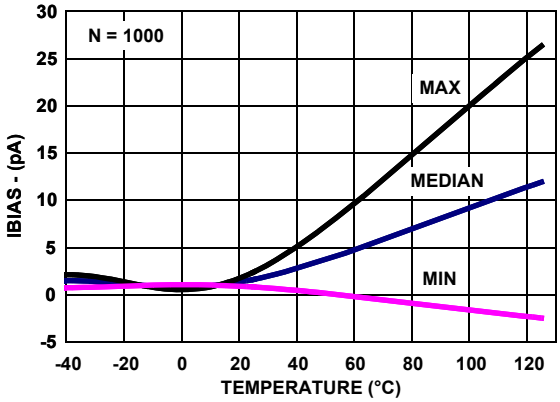


FIGURE 16. BIAS vs TEMPERATURE, $V_+ = 2.4V$

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, Unless Otherwise Specified. **(Continued)**

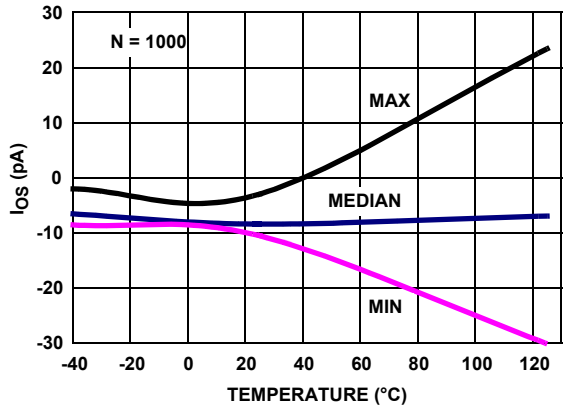


FIGURE 17. I_{OS} vs TEMPERATURE, $V_+ = 5V$

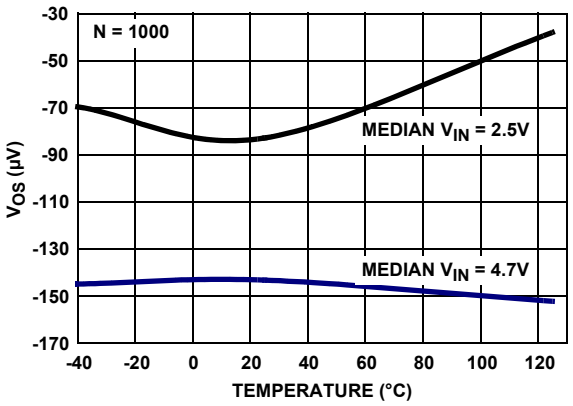


FIGURE 18. V_{OS} vs TEMPERATURE, $V_+ = 5V$ $V_{IN} = 2.5V, 4.7V$

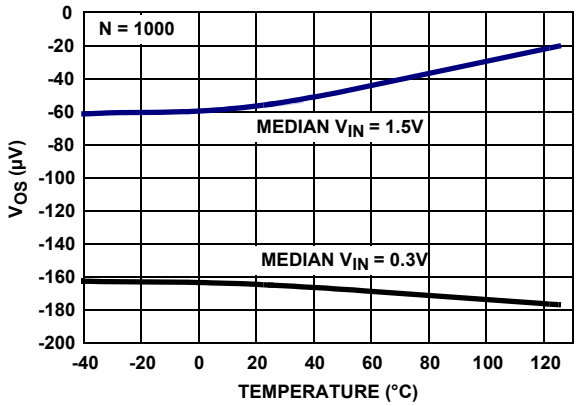


FIGURE 19. V_{OS} vs TEMPERATURE, $V_+ = 1.8V, V_{IN} = 1.5V, 0.3V$

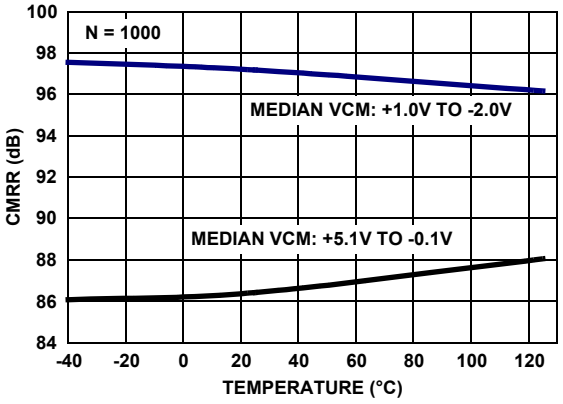


FIGURE 20. CMRR vs TEMPERATURE, VCM = +1.0V TO -2.0V, +5.1V TO -0.1V

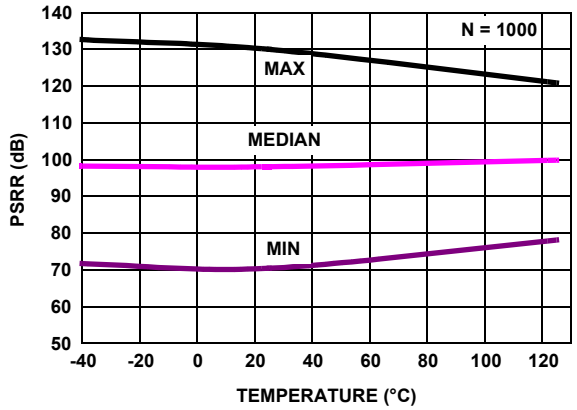


FIGURE 21. PSRR vs TEMPERATURE, V_+, V_- = ±0.9V TO ±2.5V

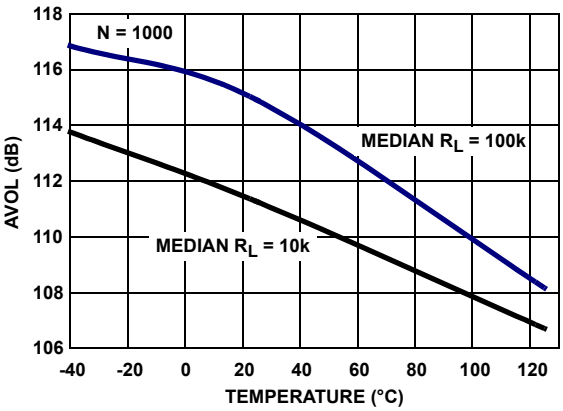


FIGURE 22. AVOL vs TEMPERATURE, $V_+ = 5V$

Typical Performance Curves V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, Unless Otherwise Specified. **(Continued)**

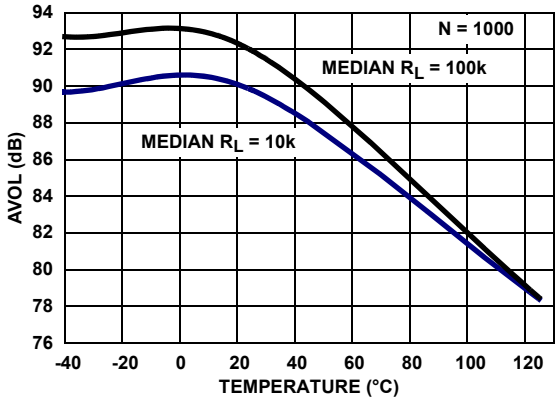


FIGURE 23. AVOL vs TEMPERATURE, V_+ = 1.8V

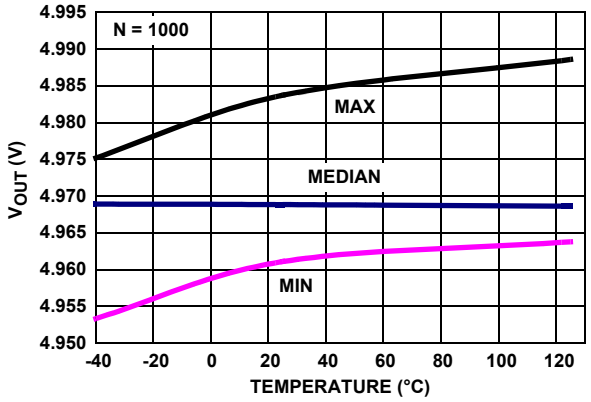


FIGURE 24. V_{OUT} HIGH vs TEMPERATURE, V_+ = 5V, R_L = 100k

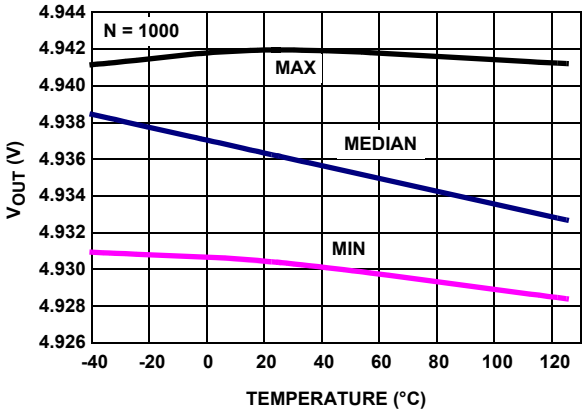


FIGURE 25. V_{OUT} HIGH vs TEMPERATURE, V_+ = 5V, R_L = 10k

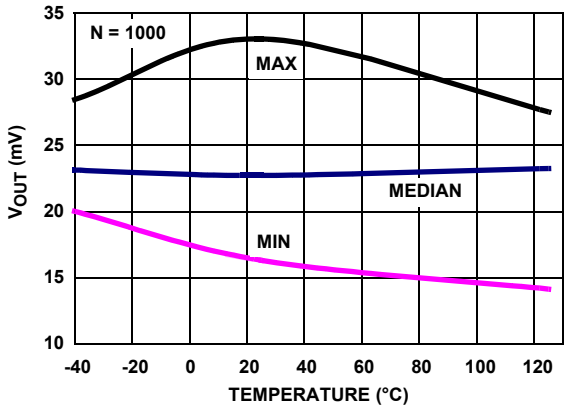


FIGURE 26. V_{OUT} LOW vs TEMPERATURE,V_+, V_- = ±2.5V, R_L = 100k

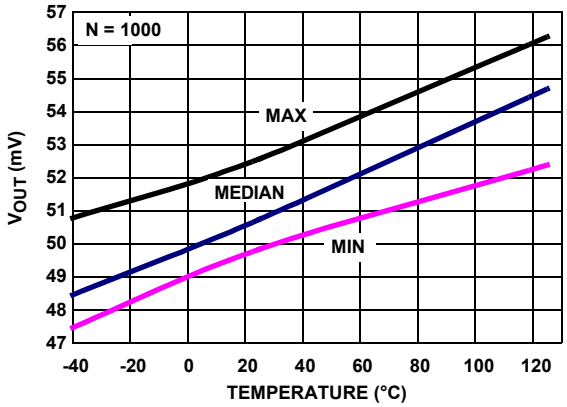
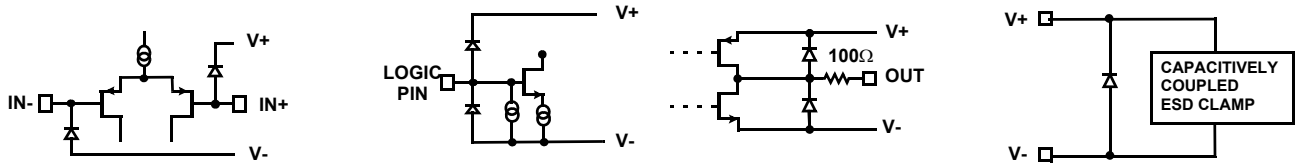


FIGURE 27. V_{OUT} LOW vs TEMPERATURE V_+, V_- = ±2.5V, R_L = 10

Pin Descriptions

ISL28194 (6 LD SOT-23)	ISL28194 (6 LD MTDFN)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	4	OUT_A	Circuit 3	Amplifier output
2	2	V-	Circuit 4	Negative power supply
3	3	IN+	Circuit 1	Amplifier non-inverting input
4	1	IN-	Circuit 1	Amplifier inverting input
5	5	EN	Circuit 2	Amplifier enable pin; Logic “1” selects the enabled state, Logic “0” selects the disabled state.
6	6	V+	Circuit 4	Positive power supply



CIRCUIT 1 CIRCUIT 2 CIRCUIT 3 CIRCUIT 4

AC Test Circuits

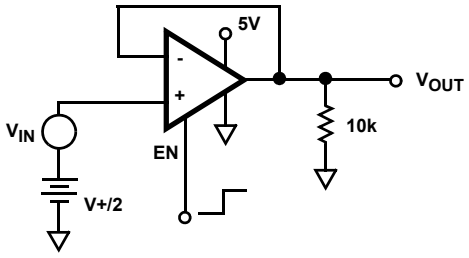


FIGURE 28. TEST CIRCUIT FOR A_V = +1

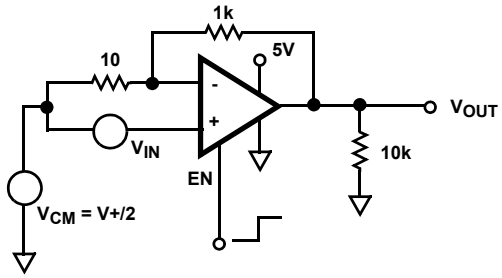


FIGURE 29. TEST CIRCUIT FOR A_V = +101

Applications Information

Introduction

The ISL28194 is a CMOS rail-to-rail input and output (RRIO) micropower operational amplifier. This device is designed to operate from single supply (1.8V to 5.5V) and has an input common mode range that extends to the positive rail and to the negative supply rail for true rail-to-rail performance. The CMOS output can swing within tens of millivolts to the rails. Featuring worst-case maximum supply current of 0.5µA, this amplifier is ideally suited for solar and battery-powered applications.

Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. The ISL28194 has a maximum input differential voltage that includes the rails (-V -0.5V to +V +0.5V).

Rail-to-Rail Output

A pair of complementary MOSFET devices are used to achieve the rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. The ISL28194 will typically swing to within 40mV or less to either rail with a 100kΩ load (reference Figures 24 and 26).

Enable/Disable Feature

This part offers an EN pin that enables the device when pulled high. The enable threshold is referenced to the -V terminal and has a level proportional to the total supply voltage (reference Figure 11 for EN threshold vs supply voltage). The enable circuit has a delay time that changes as a function of supply voltage. Figures 12 and 13 show the effect of supply voltage on the enable and disable times. For supply voltages less than 3V, it is recommended that the user account for the increase enable/disable delay time.

In the disabled state (output in a high impedance state), the supply current is reduced to typical of only 2nA. By disabling the devices, multiple parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the EN pin. The EN pin should never be left floating. The EN pin should be connected directly to the V+ supply when not in use.

The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together.

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a concern, the use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 30 shows a guard ring example for a unity gain amplifier that uses the low impedance amplifier output at the same voltage as the high impedance input to eliminate surface leakage. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

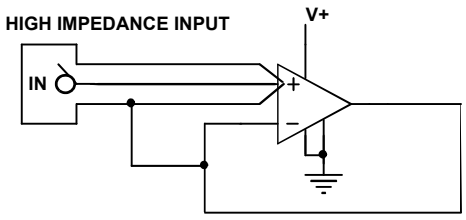


FIGURE 30. GUARD RING EXAMPLE FOR UNITY GAIN AMPLIFIER

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

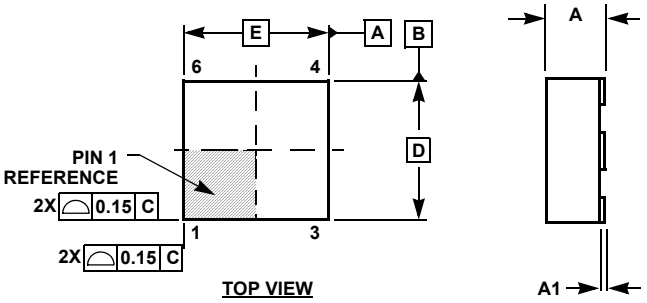
- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated as shown in Equation 2:

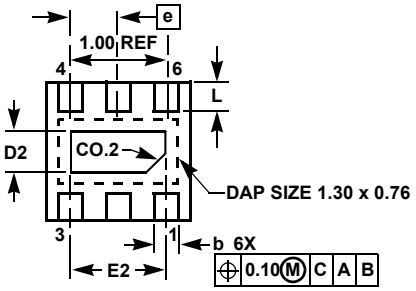
$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

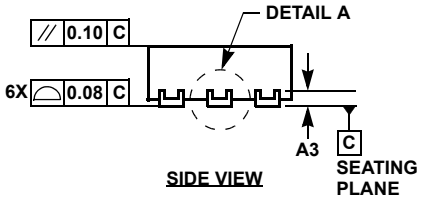
where:

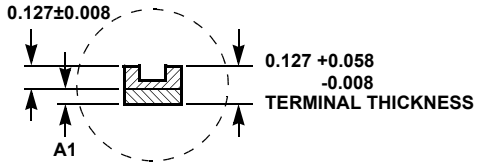
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage (Magnitude of V_+ and V_-)
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

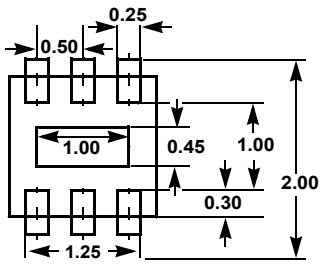
Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)











L6.1.6x1.6A

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	-
D	1.55	1.60	1.65	4
D2	0.40	0.45	0.50	-
E	1.55	1.60	1.65	4
E2	0.95	1.00	1.05	-
e		0.50 BSC		-
L	0.25	0.30	0.35	-

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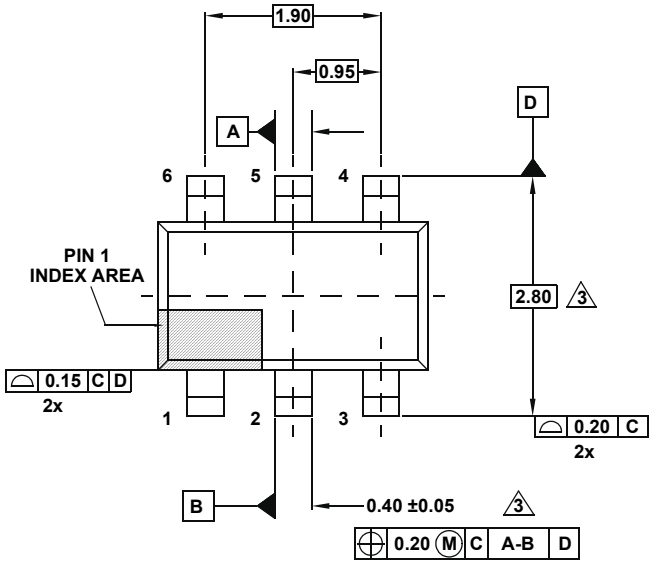
NOTES:

1. Dimensions are in MM. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08mm.
3. Warpage shall not exceed 0.10mm.
4. Package length/package width are considered as special characteristics.
5. JEDEC Reference MO-229.
6. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

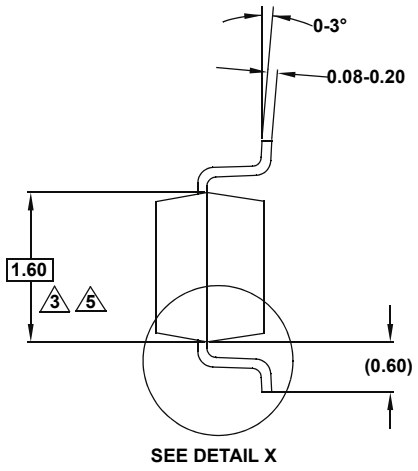
Package Outline Drawing

P6.064A

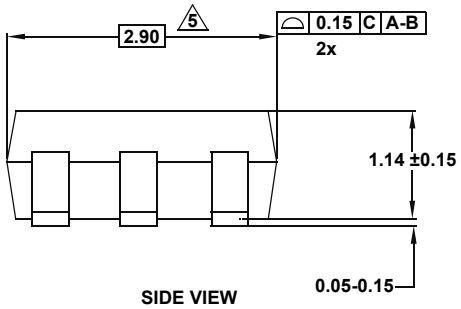
6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10



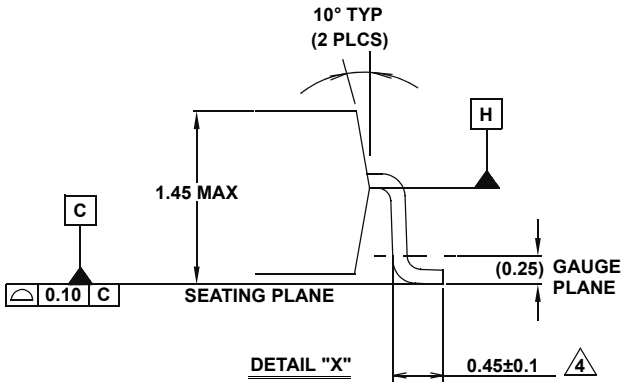
TOP VIEW

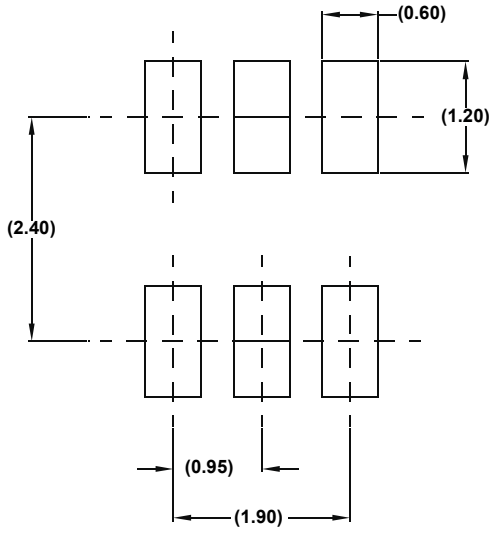


END VIEW



SIDE VIEW





TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.