ISL6324A Hybrid SVI/PVI with I^2C

Monolithic Dual PWM Hybrid Controller Powering AMD SVI Split-Plane and PVI

FN6880
Rev 1.00
May 14, 2010

The ISL6324A dual PWM controller delivers high efficiency and tight regulation from two synchronous buck DC/DC converters. The ISL6324A supports hybrid power control of AMD processors which operate from either a 6-bit parallel VID interface (PVI) or a serial VID interface (SVI). The dual output ISL6324A features a multi-phase controller to support uniplane VDD core voltage and a single phase controller to power the Northbridge (VDDNB) in SVI mode. Only the multi-phase controller is active in PVI mode to support uniplane VDD only processors.

A precision uniplane core voltage regulation system is provided by a 2-to-4-phase PWM voltage regulator (VR) controller. The integration of two power MOSFET drivers, adding flexibility in layout, reduce the number of external components in the multi-phase section. A single phase PWM controller with integrated driver provides a second precision voltage regulation system for the North Bridge portion of the processor. This monolithic, dual controller with integrated driver solution provides a cost and space saving power management solution.

For applications which benefit from load line programming to reduce bulk output capacitors, the ISL6324A features output voltage droop. The multi-phase portion also includes advanced control loop features for optimal transient response to load application and removal. One of these features is highly accurate, fully differential, continuous DCR current sensing for load line programming and channel current balance. Dual edge modulation is another unique feature, allowing for quicker initial response to high di/dt load transients.

The ISL6324A supports Power Savings Mode by dropping phases when the PSI_L bit is set. The number of phases that the ISL6324A will drop to is programmable through an I^2C interface. The number of PWM cycles between both dropping phases when entering Power Savings Mode and adding phases when exiting Power Savings Mode is also programmable through the I^2C interface.

The ISL6324A I^2C interface also allows independent programmable output voltage offset for both the Core and North Bridge regulators. The I^2C interface can also be used to set the PGOOD and OVP trip levels for both regulators as well.

Features

Processor Core Voltage Regulator Features

- Configuration Flexibility
  - 1- or 2-Phase Operation with Internal Drivers
  - 3- or 4-Phase Operation with External PWM Drivers
- Parallel VID (6-bit) Interface Inputs for PVI Mode
- PSI_L Support via Phase Shedding
- Differential Remote Voltage Sensing
- Optimal Processor Core Voltage Transient Response
  - Adaptive Phase Alignment (APA)
  - Active Pulse Positioning Modulation

Processor Core Voltage Regulator and North Bridge Voltage Regulator Shared Features

- Precision Voltage Regulation: ±0.5% System Accuracy Over-Temperature
- Two Wire, AMD Compliant Serial VID Interface Inputs for SVI Mode
- I^2C Interface
  - Voltage Margining, OVP and PGOOD Trip Levels
  - Enhanced PSI_L State Control
- Fully Differential, Continuous DCR Current Sensing
  - Accurate Load Line Programming
  - Precision Channel Current Balancing for Core
- Overcurrent Protection
- Multi-tiered Overvoltage Protection
- Variable Gate Drive Bias: 5V to 12V
- Simultaneous Digital Soft-Start of Both Outputs
- Selectable Switching Frequency up to 1MHz
- Pb-Free (RoHS Compliant)

Ordering Information

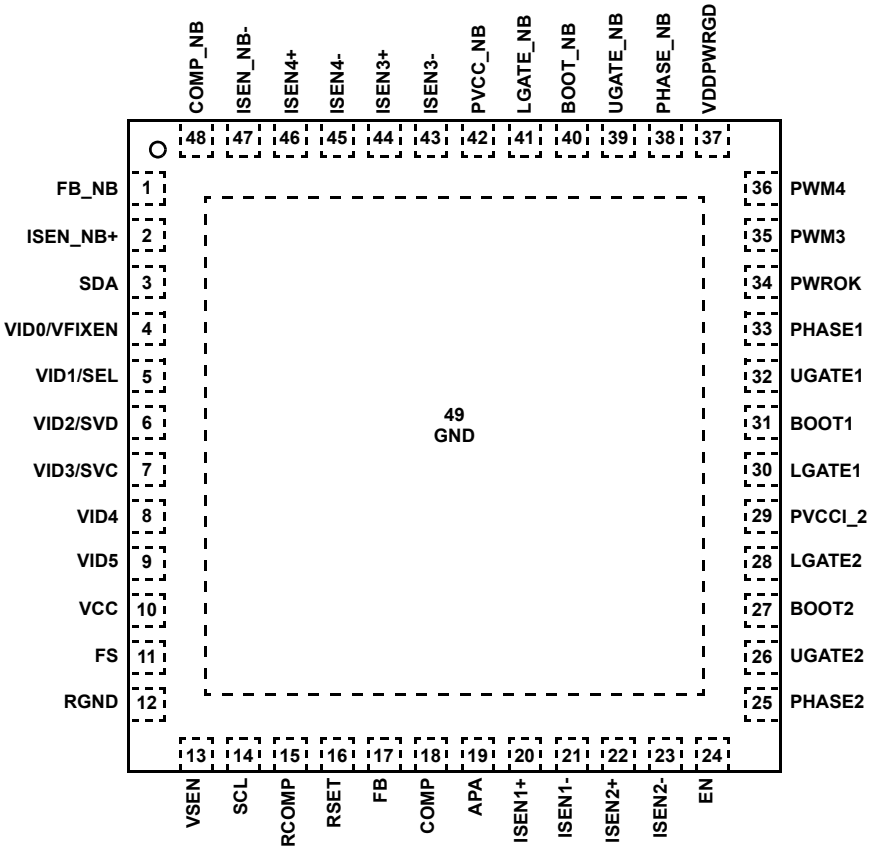
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6324ACRZ*	ISL6324A CRZ	0 to +70	48 Ld 7x7 QFN	L48.7x7
ISL6324AIRZ*	ISL6324A IRZ	-40 to +85	48 Ld 7x7 QFN	L48.7x7

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

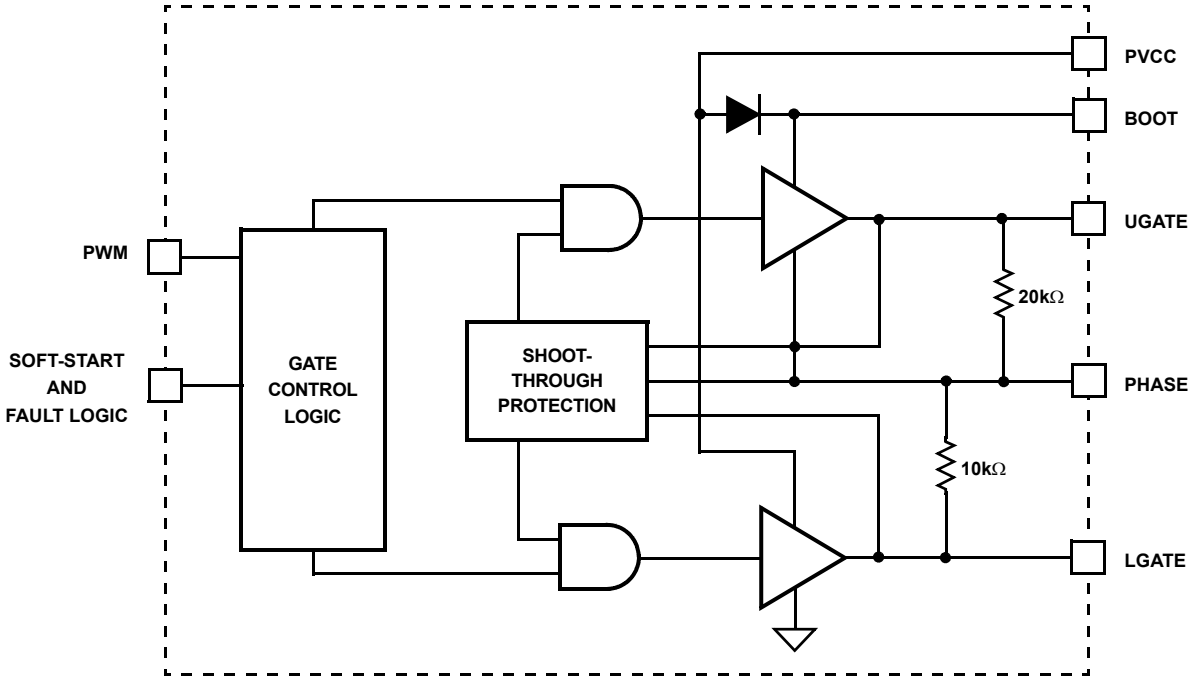
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

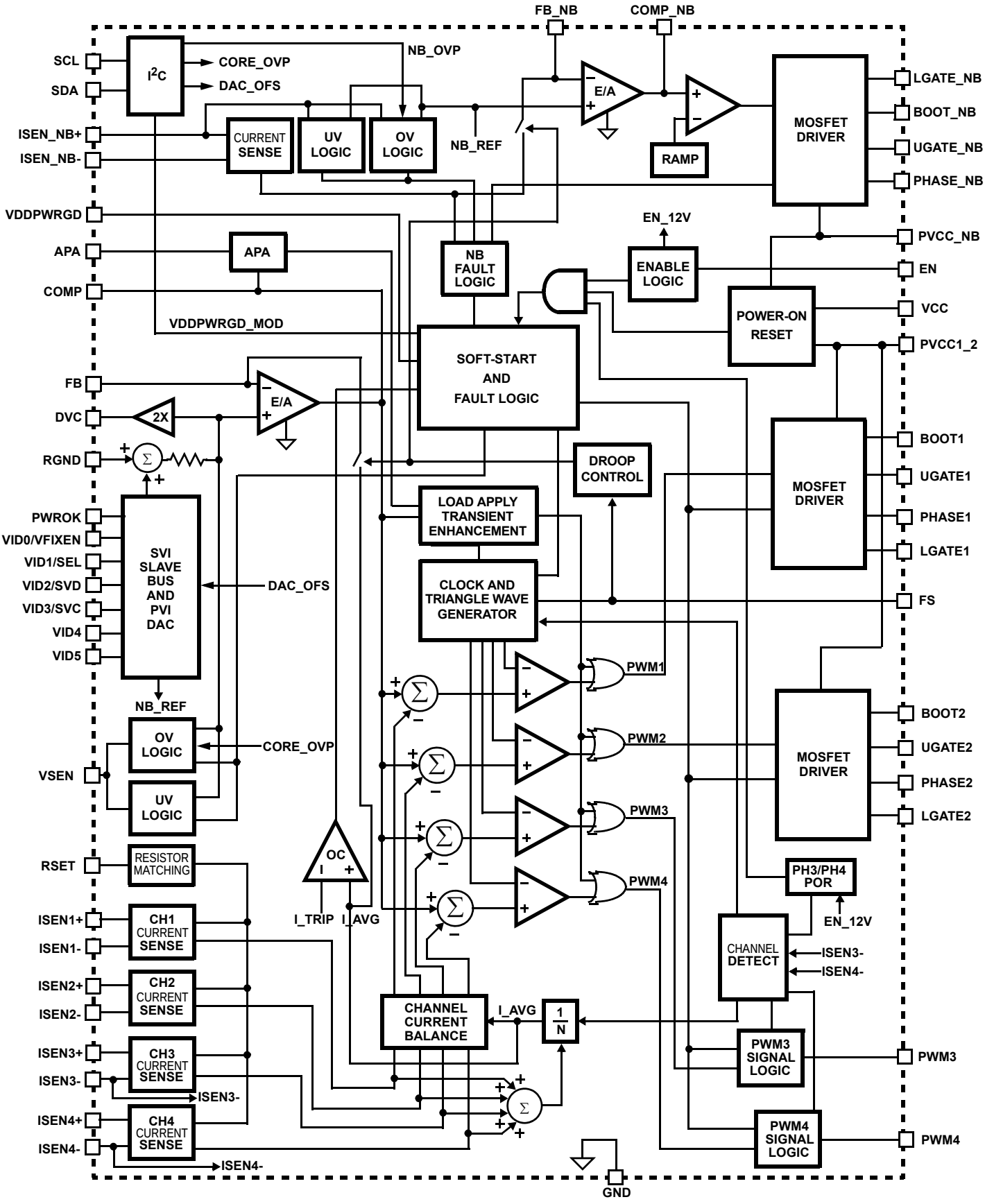
ISL6324A HYBRID SVI AND PVI
(48 LD QFN)
TOP VIEW



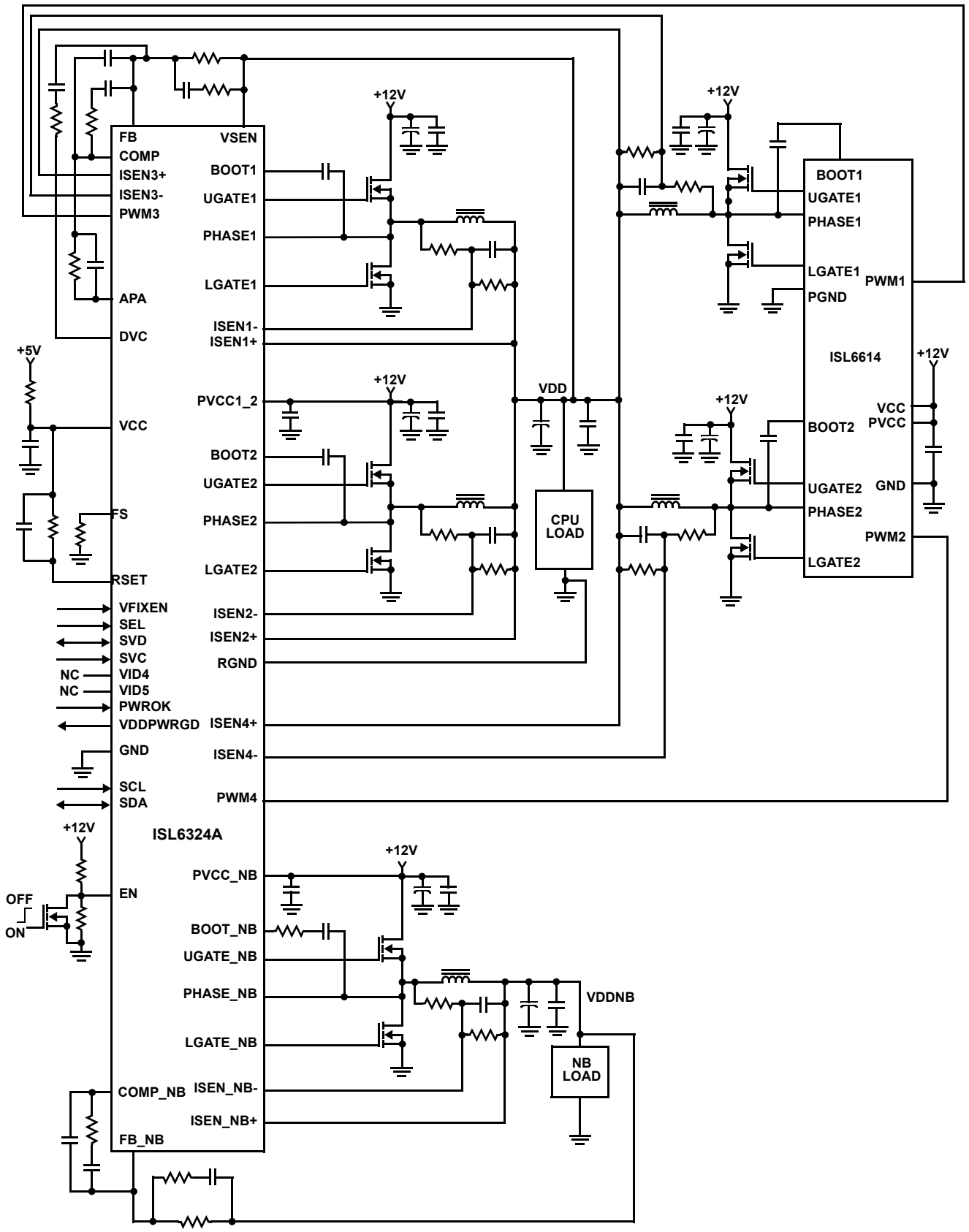
Integrated Driver Block Diagram



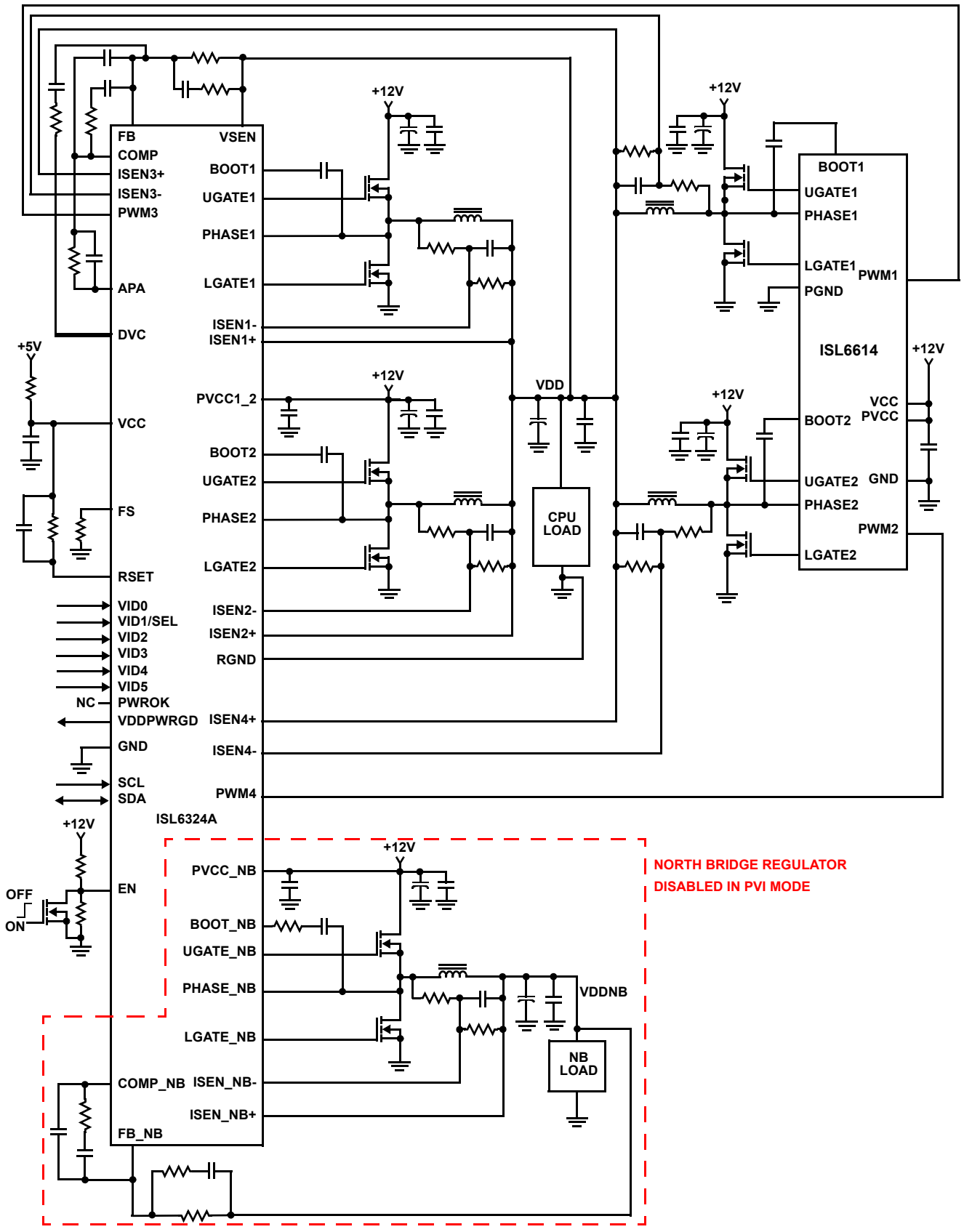
Controller Block Diagram



Typical Application - SVI Mode



Typical Application - PVI Mode



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.3V to +6.2V
Supply Voltage (PVCC) . . . . . -0.3V to +15V
Absolute Boot Voltage (V_{BOOT}) . . . . . GND - 0.3V to GND + 36V
Phase Voltage (V_{PHASE}) . . . . . GND - 0.3V to 15V (PVCC = 12)
GND - 8V (<400ns, 20µJ) to 24V (<200ns, $V_{BOOT-PHASE}$ = 12V)
Upper Gate Voltage (V_{UGATE}) . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
Lower Gate Voltage (V_{LGATE}) . . . . . GND - 0.3V to PVCC + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to PVCC+ 0.3V
Input, Output, or I/O Voltage . . . . . GND - 0.3V to VCC + 0.3V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	27	2

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

VCC Supply Voltage . . . . . +5V ±5%
PVCC Supply Voltage . . . . . +5V to 12V ±5%
Ambient Temperature
ISL6324ACRZ . . . . . 0°C to +70°C
ISL6324AIRZ . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions (0°C to +70°C), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
BIAS SUPPLIES					
Input Bias Supply Current	I_{VCC}; EN = high	15	22	25	mA
Gate Drive Bias Current - PVCC1_2 Pin	I_{PVCC1_2}; EN = high	1	1.8	3	mA
Gate Drive Bias Current - PVCC_NB Pin	I_{PVCC_NB}; EN = high	0.3	0.9	2	mA
VCC POR (Power-On Reset) Threshold	VCC Rising	4.20	4.35	4.50	V
	VCC Falling	3.70	3.85	4.05	V
PVCC POR (Power-On Reset) Threshold	PVCC Rising	4.20	4.35	4.50	V
	PVCC Falling	3.70	3.85	4.05	V
PWM MODULATOR					
Oscillator Frequency Accuracy, f_{SW}	R_T = 100kΩ (±0.1%) to Ground, (All Temps) (Droop Enabled)	225	250	265	kHz
	R_T = 100kΩ (±0.1%) to VCC, T_A = 0°C to +70°C (Droop Disabled)	245	275	310	kHz
	R_T = 100kΩ (±0.1%) to VCC, T_A = -40°C to +85°C (Droop Disabled)	240	275	310	kHz
Typical Adjustment Range of Switching Frequency	(Note 3)	0.08		1.0	MHz
Oscillator Ramp Amplitude, V_{P-P}	(Note 3)		1.50		V
Maximum Duty Cycle	(Note 3)		99.5		%
CONTROL THRESHOLDS					
EN Rising Threshold		0.80	0.88	0.92	V
EN Hysteresis		70	130	190	mV
PWROK Input HIGH Threshold			1.1		V
PWROK Input LOW Threshold			0.95		V
VDDPWRGD Sink Current	Open drain, V_VDDPWRGD = 400mV			4	mA
PWM Channel Disable Threshold	V_{ISEN3-}, V_{ISEN4-}, V_{ISEN2-}	4.4			V
REFERENCE AND DAC					
System Accuracy (VDAC > 1.000V)		-0.6		0.6	%

Electrical Specifications Recommended Operating Conditions (0°C to +70°C), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
System Accuracy (0.600V < VDAC < 1.000V)		-1.0		1.0	%
System Accuracy (VDAC < 0.600V)		-2.0		2.0	%
DVC Voltage Gain	VDAC = 1V		2.0		V
APA Current Tolerance	V_{APA} = 1V	90	100	108	µA
ERROR AMPLIFIER					
DC Gain	R_L = 10k to ground, (Note 3)		96		dB
Gain-Bandwidth Product (Note 3)	C_L = 100pF, R_L = 10k to ground, (Note 3)		20		MHz
Slew Rate (Note 3)	C_L = 100pF, Load = ±400µA, (Note 3)		8		V/µs
Maximum Output Voltage	Load = 1mA	3.80	4.20		V
Minimum Output Voltage	Load = -1mA		1.3	1.6	V
SOFT-START RAMP					
Soft-Start Ramp Rate		2.2	3.0	4.0	mV/µs
PWM OUTPUTS					
PWM Output Voltage LOW Threshold	I_{LOAD} = ±500µA			0.5	V
PWM Output Voltage HIGH Threshold	I_{LOAD} = ±500µA	4.5			V
CURRENT SENSING - CORE CONTROLLER					
Sensed Current Tolerance	V_{ISENn-} - V_{ISENn+} = 23.2mV, R_{SET} = 37.6kΩ, 4 Phases, T_A = +25°C	68		88	µA
CURRENT SENSING - NB CONTROLLER					
Sensed Current Tolerance	V_{ISEN_NB-} - V_{ISEN_NB+} = 23.2mV, R_{SET} = 37.6kΩ, 4 Phases, T_A = +25°C	68		89	µA
DROOP CURRENT					
Tolerance	V_{ISENn-} - V_{ISENn+} = 23.2mV, R_{SET} = 37.6kΩ, 4 Phases, T_A = +25°C	68		88	µA
OVERCURRENT PROTECTION					
Overcurrent Trip Level - Average Channel	Normal Operation, R_{SET} = 28.2kΩ	87	100	120	µA
	Dynamic VID Change (Note 3)		130		µA
Overcurrent Limiting- Individual Channel	Normal Operation, R_{SET} = 28.2kΩ		142		µA
	Dynamic VID Change (Note 3)		190		µA
POWER-GOOD					
Core Overvoltage Threshold	VSEN Rising Bit 6 of I^2C data = 0	VDAC + 225mV	VDAC + 250mV	VDAC + 275mV	V
Undervoltage Threshold	VSEN Falling (Core) Bit 6 of I^2C data = 0	VDAC - 325mV	VDAC - 300mV	VDAC - 270mV	mV
	ISEN_NB+ Falling (North Bridge) Bit 6 of I^2C data = 0	VDAC - 310mV	VDAC - 275mV	VDAC - 235mV	mV
Power Good Hysteresis			50		mV
OVERVOLTAGE PROTECTION					
OVP Trip Level	Bit 7 of I^2C data = 0, VDAC ≤ 1.55V	1.73	1.80	1.84	V
OVP Lower Gate Release Threshold		350	400		mV
SWITCHING TIME (Note 3) [See "Timing Diagram" on page 8]					
UGATE Rise Time	t_{RUGATE}; V_{PVCC} = 12V, 3nF Load, 10% to 90%		26		ns
LGATE Rise Time	t_{RLGATE}; V_{PVCC} = 12V, 3nF Load, 10% to 90%		18		ns
UGATE Fall Time	t_{FUGATE}; V_{PVCC} = 12V, 3nF Load, 90% to 10%		18		ns
LGATE Fall Time	t_{FLGATE}; V_{PVCC} = 12V, 3nF Load, 90% to 10%		12		ns

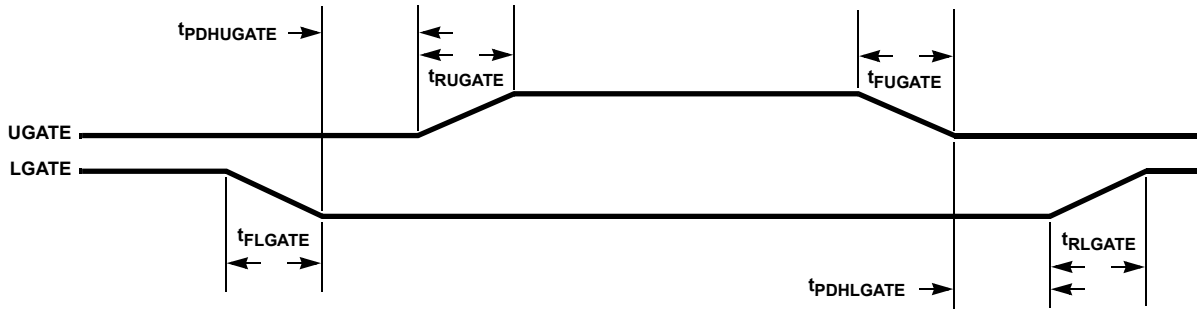
Electrical Specifications Recommended Operating Conditions (0°C to +70°C), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
UGATE Turn-On Non-overlap	$t_{PDHUGATE}$; V_{PVCC} = 12V, 3nF Load, Adaptive		10		ns
LGATE Turn-On Non-overlap	$t_{PDHLGATE}$; V_{PVCC} = 12V, 3nF Load, Adaptive		10		ns
GATE DRIVE RESISTANCE (Note 3)					
Upper Drive Source Resistance	V_{PVCC} = 12V, 15mA Source Current		2.0		Ω
Upper Drive Sink Resistance	V_{PVCC} = 12V, 15mA Sink Current		1.65		Ω
Lower Drive Source Resistance	V_{PVCC} = 12V, 15mA Source Current		1.25		Ω
Lower Drive Sink Resistance	V_{PVCC} = 12V, 15mA Sink Current		0.80		Ω
MODE SELECTION					
VID1/SEL Input Low	EN taken from HI to LO, VDDIO = 1.5V			0.6	V
VID1/SEL Input High	EN taken from LO to HI, VDDIO = 1.5V	1.00			V
PVI INTERFACE					
VIDx Pull-down	VDDIO = 1.5V		30	40	µA
VIDx Input Low	VDDIO = 1.5V			0.6	V
VIDx Input High	VDDIO = 1.5V	1.00			V
SVI INTERFACE					
SVC, SVD Input LOW (VIL)				0.4	V
SVC, SVD Input HIGH (VIH)		0.95			V
Schmitt Trigger Input Hysteresis		0.14	0.35	0.45	V
SVD Low Level Output Voltage	3mA Sink Current			0.285	V
Maximum SVC, SVD Leakage (Note 3)			±5		µA
I^2C INTERFACE					
SCL, SDA Input LOW (VIL)				1.10	V
SCL, SDA Input HIGH (VIH)		1.75			V
Schmitt Trigger Input Hysteresis		0.18	0.35	0.50	V
SDA Low Level Output Voltage	3mA Sink Current			0.2	V
Maximum SCL, SDA Leakage (Note 3)			±5		µA

NOTES:

3. Limits should be considered typical and are not production tested.
4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Timing Diagram



Functional Pin Description

VID1/SEL

This pin selects SVI or PVI mode operation based on the state of the pin prior to enabling the ISL6324A. If the pin is LO prior to enable, the ISL6324A is in SVI mode and the dual purpose pins [VID0/VFIXEN, VID2/SVC, VID3/SVD] use their SVI mode related functions. If the pin held HI prior to enable, the ISL6324A is in PVI mode and dual purpose pins use their VIDx related functions to decode the correct DAC code.

VID0/VFIXEN

If VID1 is LO prior to enable [SVI Mode], the pin is functions as the VFIXEN selection input from the AMD processor for determining SVI mode versus VFIX mode of operation.
If VID1 is HI prior to enable [PVI Mode], the pin is used as DAC input VID0. This pin has an internal 30µA pull-down current applied to it at all times.

VID2/SVD

If VID1 is LO prior to enable [SVI Mode], this pin is the serial VID data bi-directional signal to and from the master device on AMD processor. If VID1 is HI prior to enable [PVI Mode], this pin is used to decode the programmed DAC code for the processor. In PVI mode, this pin has an internal 30µA pull-down current applied to it. There is no pull-down current in SVI mode.

VID3/SVC

If VID1 is LO prior to enable [SVI Mode], this pin is the serial VID clock input from the AMD processor. If VID1 is HI prior to enable [PVI Mode], the ISL6324A is in PVI mode and this pin is used to decode the programmed DAC code for the processor. In PVI mode, this pin has an internal 30µA pull-down current applied to it. There is no pull-down current in SVI mode.

VID4

This pin is active only when the ISL6324A is in PVI mode. When VID1 is HI prior to enable, the ISL6324A decodes the programmed DAC voltage required by the AMD processor. This pin has an internal 30µA pull-down current applied to it at all times.

VID5

This pin is active only when the ISL6324A is in PVI mode. When VID1 is HI prior to enable, the ISL6324A decodes the programmed DAC voltage required by the AMD processor. This pin has an internal 30µA pull-down current applied to it at all times.

VCC

VCC is the bias supply for the ICs small-signal circuitry. Connect this pin to a +5V supply and decouple using a quality 0.1µF ceramic capacitor.

PVCC1_2

The power supply pin for the multi-phase internal MOSFET drivers. Connect this pin to any voltage from +5V to +12V depending on the desired MOSFET gate-drive level. Decouple this pin with a quality 1.0µF ceramic capacitor.

PVCC_NB

The power supply pin for the internal MOSFET driver for the Northbridge controller. Connect this pin to any voltage from +5V to +12V depending on the desired MOSFET gate-drive level. Decouple this pin with a quality 1.0µF ceramic capacitor.

GND

GND is the bias and reference ground for the IC. The GND connection for the ISL6324A is through the thermal pad on the bottom of the package.

EN

This pin is a threshold-sensitive (approximately 0.85V) system enable input for the controller. Held low, this pin disables both CORE and NB controller operation. Pulled high, the pin enables both controllers for operation.

When the EN pin is pulled high, the ISL6324A will be placed in either SVI or PVI mode. The mode is determined by the latched value of VID1 on the rising edge of the EN signal.

A third function of this pin is to provide driver bias monitor for external drivers. A resistor divider with the center tap connected to this pin from the drive bias supply prevents enabling the controller before insufficient bias is provided to external driver. The resistors should be selected such that when the POR-trip point of the external driver is reached, the voltage at this pin meets the above mentioned threshold level.

FS

A resistor, placed from FS to Ground or from FS to VCC, sets the switching frequency of both controllers. Refer to Equation 1 for proper resistor calculation.

$$R_T = 10^{[10.61 - 1.035\log(f_s)]} \quad \text{(EQ. 1)}$$

With the resistor tied from FS to Ground, Droop is enabled. With the resistor tied from FS to VCC, Droop is disabled.

VSEN and RGND

VSEN and RGND are inputs to the core voltage regulator (VR) controller precision differential remote-sense amplifier and should be connected to the sense pins of the remote processor core(s), VDDFB[H,L].

FB and COMP

These pins are the internal error amplifier inverting input and output respectively of the core VR controller. FB, VSEN and COMP are tied together through external R-C networks to compensate the regulator.

APA

Adaptive Phase Alignment (APA) pin for setting trip level and adjusting time constant. A 100µA current flows into the APA pin and by tying a resistor from this pin to COMP the trip level for the Adaptive Phase Alignment circuitry can be set.

ISEN1-, ISEN1+, ISEN2-, ISEN2+, ISEN3-, ISEN3+, ISEN4-, and ISEN4+

These pins are used for differentially sensing the corresponding channel output currents. The sensed currents are used for channel balancing, protection, and core load line regulation.

Connect ISEN1-, ISEN2-, ISEN3-, and ISEN4- to the node between the RC sense elements surrounding the inductor of their respective channel. Tie the ISEN+ pins to the VCORE side of their corresponding channel's sense capacitor.

UGATE1 and UGATE2

Connect these pins to the corresponding upper MOSFET gates. These pins are used to control the upper MOSFETs and are monitored for shoot-through prevention purposes. Maximum individual channel duty cycle is limited to 93.3%.

BOOT1 and BOOT2

These pins provide the bias voltage for the corresponding upper MOSFET drives. Connect these pins to appropriately chosen external bootstrap capacitors. Internal bootstrap diodes connected to the PVCC1_2 pin provide the necessary bootstrap charge.

PHASE1 and PHASE2

Connect these pins to the sources of the corresponding upper MOSFETs. These pins are the return path for the upper MOSFET drives.

LGATE1 and LGATE2

These pins are used to control the lower MOSFETs. Connect these pins to the corresponding lower MOSFETs' gates.

PWM3 and PWM4

Pulse-width modulation outputs. Connect these pins to the PWM input pins of an Intersil driver IC if 3- or 4-phase operation is desired. Connect the ISEN- pins of the channels not desired to +5V to disable them and configure the core VR controller for 2-phase or 3-phase operation.

PWROK

System wide Power Good signal. If this pin is low, the two SVI bits are decoded to determine the "metal VID". When the pin is high, the SVI is actively running its protocol.

RSET

Connect this pin to the VCC pin through a resistor (R_{SET}) to set the effective value of the internal R_{ISEN} current sense resistors. The values of the R_{SET} resistor should be no less than 20kΩ and no more than 80kΩ. A 0.1µF capacitor should be placed in parallel to the R_{SET} resistor.

VDDPWRGD

During normal operation this pin indicates whether both output voltages are within specified overvoltage and undervoltage limits. If either output voltage exceeds these limits or a reset event occurs (such as an overcurrent event), the pin is pulled low. This pin is always low prior to the end of soft-start.

DVC

The DVC pin is a buffered version of the reference to the error amplifier. A series resistor and capacitor between the DVC pin and FB pin smooth the voltage transition during VID-on-the-fly operations.

FB_NB and COMP_NB

These pins are the internal error amplifier inverting input and output respectively of the NB VR controller. FB_NB, VDIFF_NB, and COMP_NB are tied together through external R-C networks to compensate the regulator.

ISEN_NB-, ISEN_NB+

These pins are used for differentially sensing the North Bridge output current. The sensed current is used for protection and load line regulation if droop is enabled.

Connect ISEN_NB- to the node between the RC sense element surrounding the inductor. Tie the ISEN_NB+ pin to the VNB side of the sense capacitor.

UGATE_NB

Connect this pin to the corresponding upper MOSFET gate. This pin provides the PWM-controlled gate drive for the upper MOSFET and is monitored for shoot-through prevention purposes.

BOOT_NB

This pin provides the bias voltage for the corresponding upper MOSFET drive. Connect this pin to appropriately chosen external bootstrap capacitor. The internal bootstrap diode connected to the PVCC_NB pin provides the necessary bootstrap charge.

PHASE_NB

Connect this pin to the source of the corresponding upper MOSFET. This pin is the return path for the upper MOSFET drive. This pin is used to monitor the voltage drop across the upper MOSFET for overcurrent protection.

LGATE_NB

Connect this pin to the corresponding MOSFET's gate. This pin provides the PWM-controlled gate drive for the lower MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.

SCL

Connect this pin to the clock signal for the I^2C bus, which is a logic level input signal. The clock signal tells the controller when data is available on the I^2C bus.

SDA

Connect this pin to the bidirectional data line of the I^2C bus, which is a logic level input/output signal. All I^2C data is sent over this line, including the address of the device the bus is trying to communicate with, and what functions the device should perform.

Operation

The ISL6324A utilizes a multi-phase architecture to provide a low cost, space saving power conversion solution for the processor core voltage. The controller also implements a simple single phase architecture to provide the Northbridge voltage on the same chip.

Multi-phase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multi-phase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter that is both cost-effective and thermally viable have forced a change to the cost-saving approach of multi-phase. The ISL6324A controller helps simplify implementation by integrating vital functions and requiring minimal external components. The “Controller Block Diagram” on page 3 provides a top level view of the multi-phase power conversion using the ISL6324A controller.

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out-of-phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 2 and 3). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the DC components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine Equation 2, which represents an individual channel peak-to-peak inductor current.

$$I_{P-P} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{Lf_S V_{IN}} \quad \text{(EQ. 2)}$$

In Equation 2, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 2 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 3. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C(P-P)} = \frac{(V_{IN} - N\,V_{OUT})V_{OUT}}{Lf_S V_{IN}} \quad \text{(EQ. 3)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 1.5V to a 36A load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has $11.9A_{RMS}$ input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

Figures 26, 27 and 28 in the section entitled “Input Capacitor Selection” on page 35 can be used to determine the input capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution.

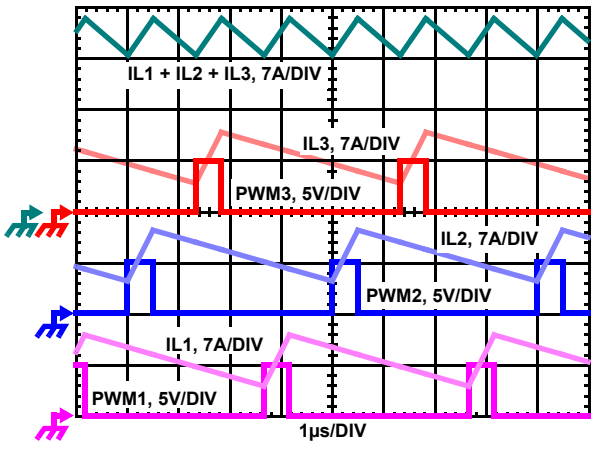


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

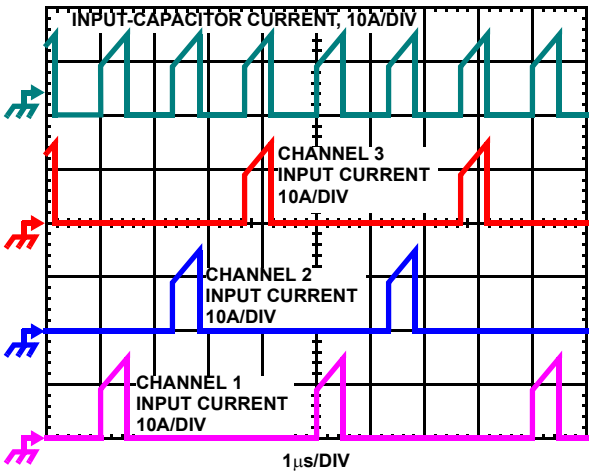


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Active Pulse Positioning Modulated PWM Operation

The ISL6324A uses a proprietary Active Pulse Positioning (APP) modulation scheme to control the internal PWM signals that command each channel's driver to turn their upper and lower MOSFETs on and off. The time interval in which a PWM signal can occur is generated by an internal clock, whose cycle time is the inverse of the switching frequency set by the resistor between the FS pin and ground. The advantage of Intersil's proprietary Active Pulse Positioning (APP) modulator is that the PWM signal has the ability to turn on at any point during this PWM time interval, and turn off immediately after the PWM signal has transitioned high. This is important because it allows the controller to quickly respond to output voltage drops associated with current load spikes, while avoiding the ring back affects associated with other modulation schemes.

The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, minus the current correction signal relative to the proprietary modulator ramp waveform as illustrated in Figure 3. At the beginning of each PWM time interval, this modified V_{COMP} signal is compared to the internal modulator waveform. As long as the modified V_{COMP} voltage is lower then the modulator waveform voltage, the PWM signal is commanded low. The internal MOSFET driver detects the low state of the PWM signal and turns off the upper MOSFET and turns on the lower synchronous MOSFET. When the modified V_{COMP} voltage crosses the modulator ramp, the PWM output transitions high, turning off the synchronous MOSFET and turning on the upper MOSFET. The PWM signal will remain high until the modified V_{COMP} voltage crosses the modulator ramp again. When this occurs the PWM signal will transition low again.

During each PWM time interval the PWM signal can only transition high once. Once PWM transitions high it can not transition high again until the beginning of the next PWM time interval. This prevents the occurrence of double PWM pulses occurring during a single period.

To further improve the transient response, ISL6324A also implements Intersil's proprietary Adaptive Phase Alignment (APA) technique, which turns on all phases together under transient events with large step current. With both APP and APA control, ISL6324A can achieve excellent transient performance and reduce the demand on the output capacitors.

Adaptive Phase Alignment (APA)

To further improve the transient response, the ISL6324A also implements Intersil's proprietary Adaptive Phase Alignment (APA) technique, which turns on all of the channels together at the same time during large current step transient events. As Figure 3 shows, the APA circuitry works by monitoring the voltage on the APA pin and comparing it to a filtered copy of the voltage on the COMP pin. The voltage on the APA pin is a copy of the COMP pin voltage that has been negatively offset. If the APA pin exceeds the filtered COMP pin voltage an APA event occurs and all of the channels are forced on.

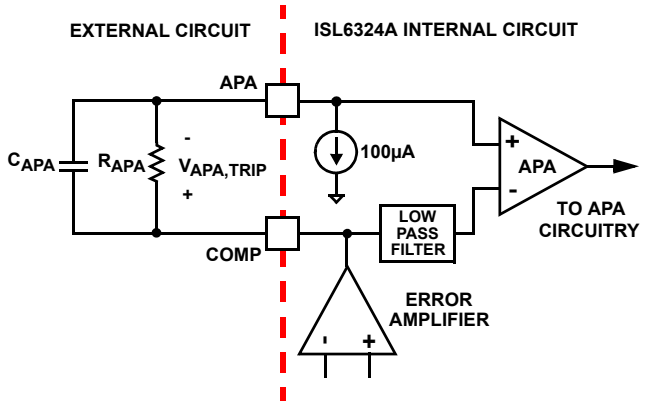


FIGURE 3. ADAPTIVE PHASE ALIGNMENT DETECTION

The APA trip level is the amount of DC offset between the COMP pin and the APA pin. This is the voltage excursion that the APA and COMP pins must have during a transient event to activate the Adaptive Phase Alignment circuitry. This APA trip level is set through a resistor, R_{APA}, that connects from the APA pin to the COMP pin. A 100µA current flows across R_{APA} into the APA pin to set the APA trip level as described in Equation 4. An APA trip level of 500mV is recommended for most applications. A 0.1µF capacitor, C_{APA}, should also be placed across the R_{APA} resistor to help with noise immunity.

$$V_{APA,TRIP} = R_{APA} \cdot 100 \times 10^{-6} \quad \text{(EQ. 4)}$$

PWM Operation

The timing of each core channel is set by the number of active channels. Channel detection on the ISEN2-, ISEN3- and ISEN4- pins selects 1-Channel to 4-Channel operation for the ISL6323A. The switching cycle is defined as the time between PWM pulse termination signals of each channel. The cycle time of the pulse signal is the inverse of the switching frequency set by the resistor between the FS pin and ground.

The PWM signals command the MOSFET driver to turn on/off the channel MOSFETs.

For 4-channel operation, the channel firing order is 1-2-3-4: PWM3 pulse happens 1/4 of a cycle after PWM4, PWM2 output follows another 1/4 of a cycle after PWM3, and PWM1 delays another 1/4 of a cycle after PWM2. For 3-channel operation, the channel firing order is 1-2-3.

Connecting ISEN4- to VCC selects three channel operation and the pulse times are spaced in 1/3 cycle increments. If ISEN3- is also connected to VCC, 2-Channel operation is selected and the PWM2 pulse happens 1/2 of a cycle after PWM1 pulse. If ISEN2- is also connected to VCC, 1-Channel operation is selected.

Continuous Current Sampling

In order to realize proper current-balance, the currents in each channel are sampled continuously every switching cycle. During this time, the current-sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. This sensed current, I_{SEN}, is simply a scaled version of the inductor current.

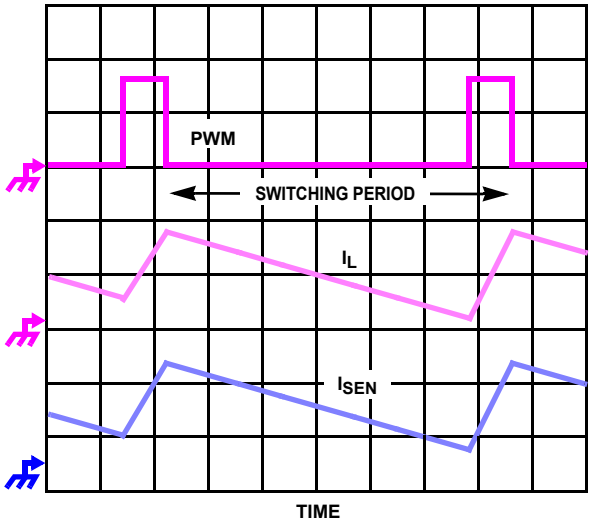


FIGURE 4. CONTINUOUS CURRENT SAMPLING

The ISL6324A supports Inductor DCR current sensing to continuously sample each channel's current for channel-current balance. The internal circuitry, shown in Figure 6 represents Channel N of an N-Channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on how many channels are operating.

Inductor windings have a characteristic distributed resistance or DCR (Direct Current Resistance). For simplicity, the inductor DCR is considered as a separate lumped quantity, as shown in Figure 6. The channel current I_{Ln}, flowing through the inductor, passes through the DCR. Equation 5 shows the S-domain equivalent voltage, V_L, across the inductor.

$$V_L(s) = I_{L_n} \cdot (s \cdot L + DCR) \quad \text{(EQ. 5)}$$

A simple R-C network across the inductor (R_1, R_2 and C) extracts the DCR voltage, as shown in Figure 6. The voltage across the sense capacitor, V_C, can be shown to be proportional to the channel current I_{Ln}, shown in Equation 6.

$$V_C(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{\left(s \cdot \frac{(R_1 \cdot R_2)}{R_1 + R_2} \cdot C + 1\right)} \cdot K \cdot DCR \cdot I_{L_n} \quad \text{(EQ. 6)}$$

Where:

$$K = \frac{R_2}{R_2 + R_1} \quad \text{(EQ. 7)}$$

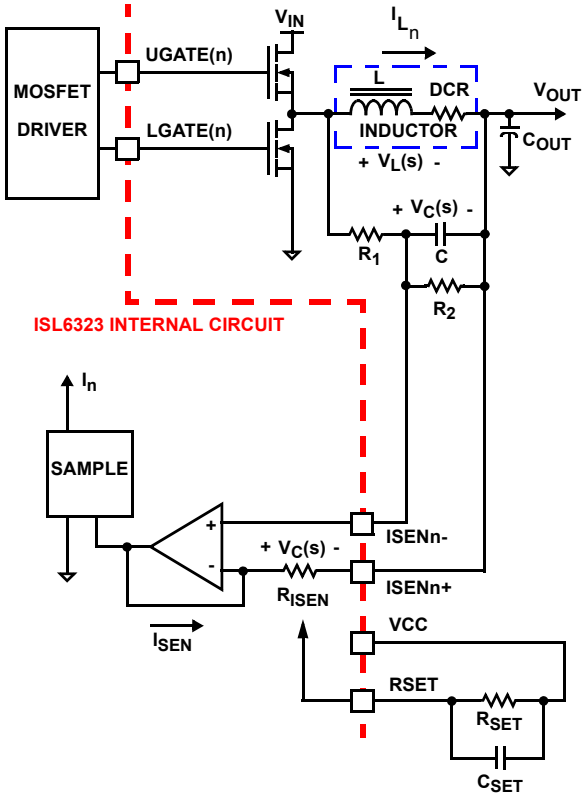


FIGURE 5. INDUCTOR DCR CURRENT SENSING CONFIGURATION

If the R-C network components are selected such that the RC time constant matches the inductor L/DCR time constant (see Equation 8), then V_C is equal to the voltage drop across the DCR multiplied by the ratio of the resistor divider, K. If a resistor divider is not being used, the value for K is 1.

$$\frac{L}{DCR} = \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C \quad \text{(EQ. 8)}$$

The capacitor voltage V_C, is then replicated across the effective internal sense resistor, R_{ISEN}. This develops a current through R_{ISEN} which is proportional to the inductor current. This current, I_{SEN}, is continuously sensed and is then used by the controller for load-line regulation, channel-current balancing, and overcurrent detection and limiting. Equation 9 shows that the proportion between the channel current, I_L, and the sensed

current, I_{SEN}, is driven by the value of the effective sense resistance, R_{ISEN}, and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 9)}$$

The effective internal R_{ISEN} resistance is important to the current sensing process because it sets the gain of the load line regulation loop when droop is enabled as well as the gain of the channel-current balance loop and the overcurrent trip level. The effective internal R_{ISEN} resistance is user programmable and is set through use of the RSET pin. Placing a single resistor, R_{SET}, from the RSET pin to the VCC pin programs the effective internal R_{ISEN} resistance according to Equation 10.

$$R_{ISEN} = \frac{3}{400} \cdot R_{SET} \quad \text{(EQ. 10)}$$

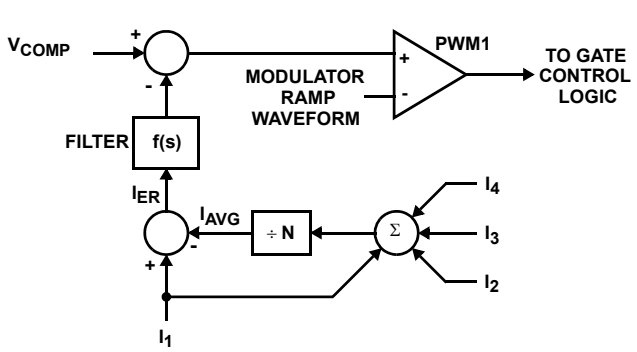
The North Bridge regulator samples the load current in the same manner as the Core regulator does. The R_{SET} resistor will program all the effective internal R_{ISEN} resistors to the same value.

Channel-Current Balance

One important benefit of multi-phase operation is the thermal advantage gained by distributing the dissipated heat over multiple devices and greater area. By doing this the designer avoids the complexity of driving parallel MOSFETs and the expense of using expensive heat sinks and exotic magnetic materials.

In order to realize the thermal advantage, it is important that each channel in a multi-phase converter be controlled to carry about the same amount of current at any load level. To achieve this, the currents through each channel must be sampled every switching cycle. The sampled currents, I_n, from each active channel are summed together and divided by the number of active channels. The resulting cycle average current, I_{AVG}, provides a measure of the total load current demand on the converter during each switching cycle. Channel-current balance is achieved by comparing the sampled current of each channel to the cycle average current, and making the proper adjustment to each channel pulse width based on the error. Intersil's patented current balance method is illustrated in Figure 6, with error correction for Channel 1 represented. In the figure, the cycle average current, I_{AVG}, is compared with the Channel 1 sample, I_1, to create an error signal I_{ER}.

The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.



NOTE: Channel 3 and 4 are optional.

FIGURE 6. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

VID Interface

The ISL6324A supports hybrid power control of AMD processors which operate from either a 6-bit parallel VID interface (PVI) or a serial VID interface (SVI). The VID1/SEL pin is used to command the ISL6324A into either the PVI mode or the SVI mode. Whenever the EN pin is held LOW, both the multi-phase Core and single-phase North Bridge Regulators are disabled and the ISL6324A is continuously sampling voltage on the VID1/SEL pin. When the EN pin is toggled HIGH, the status of the VID1/SEL pin will latch the ISL6324A into either PVI or SVI mode. This latching occurs on the rising edge of the EN signal.If the VID1/SEL pin is held LOW during the latch, the ISL6324A will be placed into SVI mode. If the VID1/SEL pin is held HIGH during the latch, the ISL6324A will be placed into PVI mode. For the ISL6324A to properly enter into either mode, the level on the VID1/SEL pin must be stable no less that 1µs prior to the EN signal transitioning from low to high.

6-bit Parallel VID Interface (PVI)

With the ISL6324A in PVI mode, the single-phase North Bridge regulator is disabled. Only the multi-phase controller is active in PVI mode to support uniplane VDD only processors. Table 1 shows the 6-bit parallel VID codes and the corresponding reference voltage.

TABLE 1. 6-BIT PARALLEL VID CODES

VID5	VID4	VID3	VID2	VID1	VID0	VREF
0	0	0	0	0	0	1.5500
0	0	0	0	0	1	1.5250
0	0	0	0	1	0	1.5000
0	0	0	0	1	1	1.4750
0	0	0	1	0	0	1.4500
0	0	0	1	0	1	1.4250
0	0	0	1	1	0	1.4000
0	0	0	1	1	1	1.3750
0	0	1	0	0	0	1.3500
0	0	1	0	0	1	1.3250

TABLE 1. 6-BIT PARALLEL VID CODES (Continued)

VID5	VID4	VID3	VID2	VID1	VID0	VREF
0	0	1	0	1	0	1.3000
0	0	1	0	1	1	1.2750
0	0	1	1	0	0	1.2500
0	0	1	1	0	1	1.2250
0	0	1	1	1	0	1.2000
0	0	1	1	1	1	1.1750
0	1	0	0	0	0	1.1500
0	1	0	0	0	1	1.1250
0	1	0	0	1	0	1.1000
0	1	0	0	1	1	1.0750
0	1	0	1	0	0	1.0500
0	1	0	1	0	1	1.0250
0	1	0	1	1	0	1.0000
0	1	0	1	1	1	0.9750
0	1	1	0	0	0	0.9500
0	1	1	0	0	1	0.9250
0	1	1	0	1	0	0.9000
0	1	1	0	1	1	0.8750
0	1	1	1	0	0	0.8500
0	1	1	1	0	1	0.8250
0	1	1	1	1	0	0.8000
0	1	1	1	1	1	0.7750
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.7500
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7250
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7000
1	0	0	1	1	0	0.6875
1	0	0	1	1	1	0.6750
1	0	1	0	0	0	0.6625
1	0	1	0	0	1	0.6500
1	0	1	0	1	0	0.6375
1	0	1	0	1	1	0.6250
1	0	1	1	0	0	0.6125
1	0	1	1	0	1	0.6000
1	0	1	1	1	0	0.5875
1	0	1	1	1	1	0.5750
1	1	0	0	0	0	0.5625
1	1	0	0	0	1	0.5500
1	1	0	0	1	0	0.5375
1	1	0	0	1	1	0.5250
1	1	0	1	0	0	0.5125
1	1	0	1	0	1	0.5000

TABLE 1. 6-BIT PARALLEL VID CODES (Continued)

VID5	VID4	VID3	VID2	VID1	VID0	VREF
1	1	0	1	1	0	0.4875
1	1	0	1	1	1	0.4750
1	1	1	0	0	0	0.4625
1	1	1	0	0	1	0.4500
1	1	1	0	1	0	0.4375
1	1	1	0	1	1	0.4250
1	1	1	1	0	0	0.4125
1	1	1	1	0	1	0.4000
1	1	1	1	1	0	0.3875
1	1	1	1	1	1	0.3750

Serial VID Interface (SVI)

The on-board Serial VID interface (SVI) circuitry allows the processor to directly drive the core voltage and Northbridge voltage reference level within the ISL6324A. The SVC and SVD states are decoded with direction from the PWROK and VFIXEN inputs as described in the following sections. The ISL6324A uses a digital to analog converter (DAC) to generate a reference voltage based on the decoded SVI value. See Figure 7 for a simple SVI interface timing diagram.

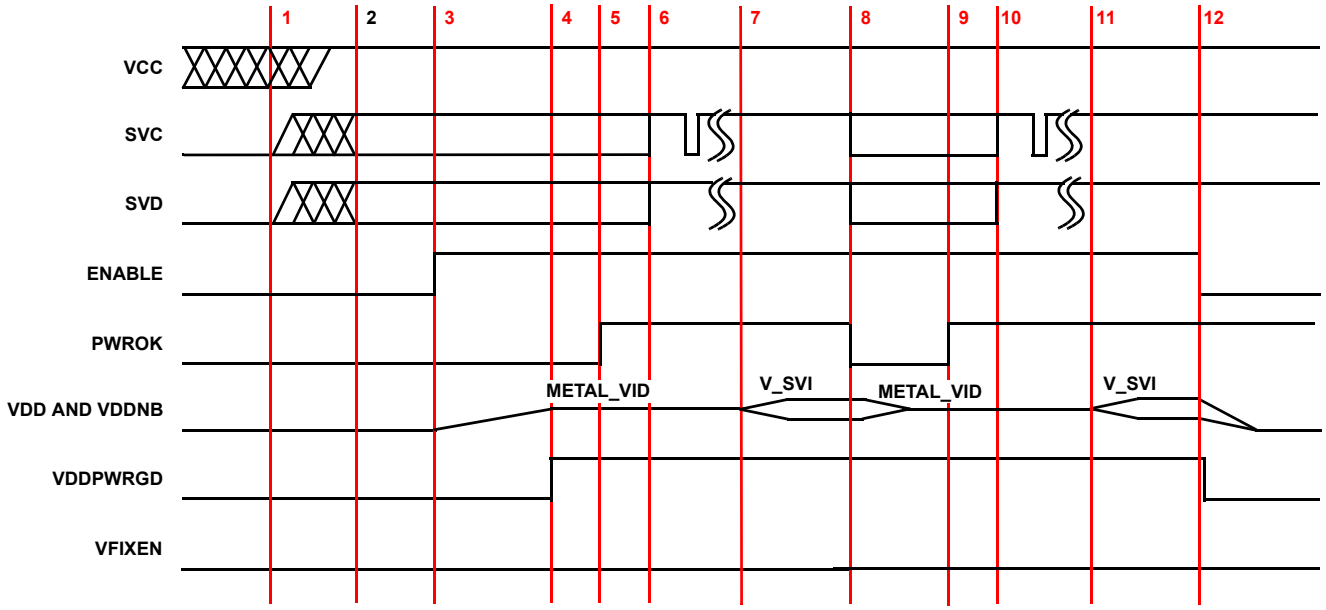


FIGURE 7. SVI INTERFACE TIMING DIAGRAM: TYPICAL PRE-PWROK METAL VID START-UP

PRE-PWROK METAL VID

Typical motherboard start-up occurs with the VFIXEN input low. The controller decodes the SVC and SVD inputs to determine the Pre-PWROK metal VID setting. Once the POR circuitry is satisfied, the ISL6324A begins decoding the inputs per Table 2. Once the EN input exceeds the rising enable threshold, the ISL6324A saves the Pre-PWROK metal VID value in an on-board holding register and passes this target to the internal DAC circuitry.

TABLE 2. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

The Pre-PWROK metal VID code is decoded and latched on the rising edge of the enable signal. Once enabled, the ISL6324A passes the Pre-PWROK metal VID code on to internal DAC circuitry. The internal DAC circuitry begins to ramp both the VDD and VDDNB planes to the decoded Pre-PWROK metal VID output level. The digital soft-start circuitry actually stair steps the internal reference to the target gradually over a fix interval. The controlled ramp of both output voltage planes reduces in-rush current during the soft-start interval. At the end of the soft-start interval, the VDDPWRGD output transitions high indicating both output planes are within regulation limits.

If the EN input falls below the enable falling threshold, the ISL6324A ramps the internal reference voltage down to near zero. The VDDPWRGD de-asserts with the loss of enable. The VDD and VDDNB planes will linearly decrease to near zero.

VFIX MODE

In VFIX Mode, the SVC, SVD and VFIXEN inputs are fixed external to the controller through jumpers to either GND or VDDIO. These inputs are not expected to change, but the ISL6324A is designed to support the potential change of state of these inputs. If VFIXEN is high, the IC decodes the SVC and SVD states per Table 3.

Once enabled, the ISL6324A begins to soft-start both VDD and VDDNB planes to the programmed VFIX level. The internal soft-start circuitry slowly stair steps the reference up to the target value and this results in a controlled ramp of the power planes. Once soft-start has ended and both output planes are within regulation limits, the VDDPWRGD pin transitions high. If the EN input falls below the enable falling threshold, then the controller ramps both VDD and VDDNB down to near zero.

TABLE 3. VFIXEN VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

SVI MODE

Once the controller has successfully soft-started and VDDPWRGD transitions high, the Northbridge SVI interface can assert PWROK to signal the ISL6324A to prepare for SVI commands. The controller actively monitors the SVI interface for set VID commands to move the plane voltages to start-up VID values. Details of the SVI Bus protocol are provided in the

AMD Design Guide for Voltage Regulator Controllers Accepting Serial VID Codes specification.

Once the set VID command is received, the ISL6324A decodes the information to determine which plane and the VID target required. See Table 4. The internal DAC circuitry steps the required output plane voltage to the new VID level. During this time one or both of the planes could be targeted. In the event the core voltage plane, VDD, is commanded to power off by serial VID commands, the VDDPWRGD signal remains asserted. The Northbridge voltage plane must remain active during this time.

If the PWROK input is de-asserted, then the controller steps both VDD and VDDNB planes back to the stored Pre-PWROK metal VID level in the holding register from initial soft-start. No attempt is made to read the SVC and SVD inputs during this time. If PWROK is reasserted, then the on-board SVI interface waits for a set VID command.

If VDDPWRGD deasserts during normal operation, both voltage planes are powered down in a controlled fashion. The internal DAC circuitry stair steps both outputs down to near zero.

TABLE 4. SERIAL VID CODES

SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)
000_0000b	1.5500	010_0000b	1.1500	100_0000b	0.7500	110_0000b	0.3500*
000_0001b	1.5375	010_0001b	1.1375	100_0001b	0.7375	110_0001b	0.3375*
000_0010b	1.5250	010_0010b	1.1250	100_0010b	0.7250	110_0010b	0.3250*
000_0011b	1.5125	010_0011b	1.1125	100_0011b	0.7125	110_0011b	0.3125*
000_0100b	1.5000	010_0100b	1.1000	100_0100b	0.7000	110_0100b	0.3000*
000_0101b	1.4875	010_0101b	1.0875	100_0101b	0.6875	110_0101b	0.2875*
000_0110b	1.4750	010_0110b	1.0750	100_0110b	0.6750	110_0110b	0.2750*
000_0111b	1.4625	010_0111b	1.0625	100_0111b	0.6625	110_0111b	0.2625*
000_1000b	1.4500	010_1000b	1.0500	100_1000b	0.6500	110_1000b	0.2500*
000_1001b	1.4375	010_1001b	1.0375	100_1001b	0.6375	110_1001b	0.2375*
000_1010b	1.4250	010_1010b	1.0250	100_1010b	0.6250	110_1010b	0.2250*
000_1011b	1.4125	010_1011b	1.0125	100_1011b	0.6125	110_1011b	0.2125*
000_1100b	1.4000	010_1100b	1.0000	100_1100b	0.6000	110_1100b	0.2000*
000_1101b	1.3875	010_1101b	0.9875	100_1101b	0.5875	110_1101b	0.1875*
000_1110b	1.3750	010_1110b	0.9750	100_1110b	0.5750	110_1110b	0.1750*
000_1111b	1.3625	010_1111b	0.9625	100_1111b	0.5625	110_1111b	0.1625*
001_0000b	1.3500	011_0000b	0.9500	101_0000b	0.5500	111_0000b	0.1500*
001_0001b	1.3375	011_0001b	0.9375	101_0001b	0.5375	111_0001b	0.1375*
001_0010b	1.3250	011_0010b	0.9250	101_0010b	0.5250	111_0010b	0.1250*
001_0011b	1.3125	011_0011b	0.9125	101_0011b	0.5125	111_0011b	0.1125*
001_0100b	1.3000	011_0100b	0.9000	101_0100b	0.5000	111_0100b	0.1000*
001_0101b	1.2875	011_0101b	0.8875	101_0101b	0.4875*	111_0101b	0.0875*
001_0110b	1.2750	011_0110b	0.8750	101_0110b	0.4750*	111_0110b	0.0750*
001_0111b	1.2625	011_0111b	0.8625	101_0111b	0.4625*	111_0111b	0.0625*
001_1000b	1.2500	011_1000b	0.8500	101_1000b	0.4500*	111_1000b	0.0500*
001_1001b	1.2375	011_1001b	0.8375	101_1001b	0.4375*	111_1001b	0.0375*
001_1010b	1.2250	011_1010b	0.8250	101_1010b	0.4250*	111_1010b	0.0250*
001_1011b	1.2125	011_1011b	0.8125	101_1011b	0.4125*	111_1011b	0.0125*
001_1100b	1.2000	011_1100b	0.8000	101_1100b	0.4000*	111_1100b	OFF
001_1101b	1.1875	011_1101b	0.7875	101_1101b	0.3875*	111_1101b	OFF
001_1110b	1.1750	011_1110b	0.7750	101_1110b	0.3750*	111_1110b	OFF
001_1111b	1.1625	011_1111b	0.7625	101_1111b	0.3625*	111_1111b	OFF

NOTE: * Indicates a VID not required for AMD Family 10h processors.

POWER SAVINGS MODE: PSI_L

Bit 7 of the Serial VID code transmitted as part of the 8-bit data phase over the SVI bus is allocated for the PSI_L. If Bit 7 is 0, then the processor is at an optimal load for the regulator to enter power savings mode. If Bit 7 is 1, then the regulator should not be in power savings mode.

With the ISL6324A, Power Savings mode is realized through phase shedding. Once a Serial VID command with Bit 7 set to 0 is received, the ISL6324A will shed phases in a sequential manner. The default number of phases that the ISL6324A will run on in Power Savings Mode is two. This number is programmable through the I^2C interface and can be set to three phases or to one phase (See "I2C Bus Interface" on page 23). Phases are shed decrementally, starting with Channel 4. When a phase is shed, that phase will not go into a tri-state mode until that phase would have had its PWM go HIGH.

After a phase is shed, the ISL6324A will wait, by default, 1 full PWM cycle before shedding the next phase. This delay can be changed to 0, 2 or 4 PWM cycle delays through the I^2C interface (See "I2C Bus Interface" on page 23). It should be noted that with a 0 cycle delay, all phases that are to be shed will be turned off at the same time. While the option to shed all phases at once is available, it is not recommended as the Core voltage could be subjected to large output deviations during the transition.

When leaving Power Savings Mode, through the reception of a Serial VID command with Bit 7 set to 1, the ISL6324A will sequentially turn on phases starting with the lowest numbered phase that has been shed. When a phase is being reactivated, it will not leave a tri-state until the PWM of that phase goes HIGH.

After a phase is reactivated, the ISL6324A will wait, by default, 1 full PWM cycle before reactivating the next phase. This delay can be changed to 0, 2 or 4 PWM cycle delays through the I^2C interface (See "I2C Bus Interface" on page 23). It should be noted that with a 0 cycle delay, all phases that have been shed will be turned on at the same time. While the option to reactivate all phases at once is available, it is not recommended as the Core voltage could be subjected to large output deviations during the transition.

If, while in Power Savings Mode, a Serial VID command is received that forces a VID level change while maintaining Bit 7 at 0, the ISL632A will first exit the Power Savings Mode state as previously described. The output voltage will then be stepped up or down to the appropriate VID level. Finally, the ISL6324A will then re-enter Power Savings Mode.

If the Core regulator has had an offset voltage added to the DAC through the I^2C interface, this offset will, by default, remain while in Power Savings Mode. Through the I^2C interface, the offset can be disabled while in Power Savings Mode (See "I2C Bus Interface" on page 23).

Voltage Regulation

The integrating compensation network shown in Figure 8 insures that the steady-state error in the output voltage is limited only to the error in the reference voltage, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6324A to include the combined tolerances of each of these elements.

The output of the error amplifier, V_{COMP}, is used by the modulator to generate the PWM signals. The PWM signals control the timing of the Internal MOSFET drivers and regulate the converter output so that the voltage at FB is equal to the voltage at REF. This will regulate the output voltage to be equal to Equation 11. The internal and external circuitry that controls voltage regulation is illustrated in Figure 8.

$$V_{OUT} = V_{REF} - V_{DROOP} \quad \text{(EQ. 11)}$$

The ISL6324A incorporates differential remote-sense amplification in the feedback path. The differential sensing removes the voltage error encountered when measuring the output voltage relative to the controller ground reference point resulting in a more accurate means of sensing output voltage.

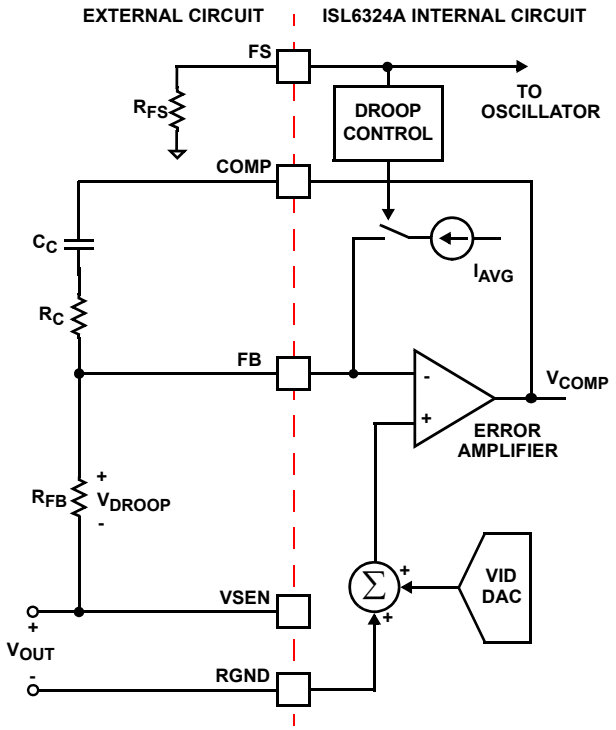


FIGURE 8. OUTPUT VOLTAGE AND LOAD-LINE REGULATION

Load-Line (Droop) Regulation

By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction which works to achieve a cost-effective solution can help to reduce the output-voltage spike that results from fast load-current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

As shown in Figure 8, with the FS resistor tied to ground, the average current of all active channels, I_{AVG}, flows from FB through a load-line regulation resistor R_{FB}. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined as in Equation 12:

$$V_{DROOP} = I_{AVG} \cdot R_{FB} \quad \text{(EQ. 12)}$$

The regulated output voltage is reduced by the droop voltage V_{DROOP}. The output voltage as a function of load current is shown in Equation 13.

$$V_{OUT} = V_{REF} - \left(\frac{I_{OUT}}{N} \cdot DCR \cdot \left(\frac{400}{3} \cdot \frac{1}{R_{SET}} \right) \cdot K \cdot R_{FB} \right) \quad \text{(EQ. 13)}$$

In Equation 13, V_{REF} is the reference voltage, I_{OUT} is the total output current of the converter, K is the DC gain of the RC filter across the inductor (K is defined in Equation 7), N is the number of active channels, and DCR is the Inductor DCR value.

Dynamic VID

The AMD processor does not step the output voltage commands up or down to the target voltage, but instead passes only the target voltage to the ISL6324A through either the PVI or SVI interface. The ISL6324A manages the resulting VID-on-the-Fly transition in a controlled manner, supervising a safe output voltage transition without discontinuity or disruption. The ISL6324A begins slewing the DAC at 3.25mV/µs until the DAC and target voltage are equal. Thus, the total time required for a dynamic VID transition is dependent only on the size of the DAC change.

To further improve dynamic VID performance, ISL6324A also implements a proprietary DAC smoothing feature. The external series RC components connected between DVC and FB limit any stair-stepping of the output voltage during a VID-on-the-Fly transition.

Compensating Dynamic VID Transitions

During a VID transition, the resulting change in voltage on the FB pin and the COMP pin causes an AC current to flow through the error amplifier compensation components from the FB to the COMP pin. This current then flows through the feedback resistor, R_{FB}, and can cause the output voltage to overshoot or undershoot at the end of the VID transition. In order to ensure the smooth transition of the output voltage

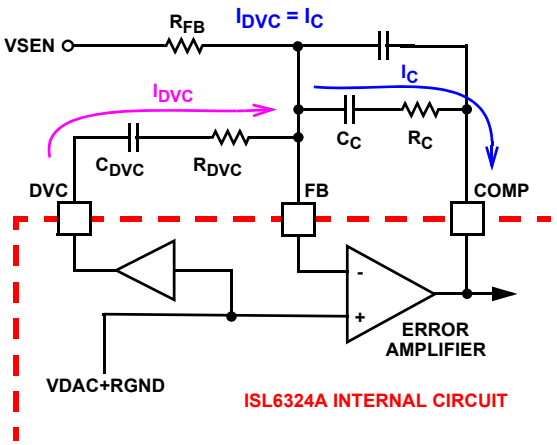


FIGURE 9. DYNAMIC VID COMPENSATION NETWORK

during a VID change, a VID-on-the-fly compensation network is required. This network is composed of a resistor and capacitor in series, R_{DVC} and C_{DVC}, between the DVC and the FB pin.

This VID-on-the-fly compensation network works by sourcing AC current into the FB node to offset the effects of the AC current flowing from the FB to the COMP pin during a VID transition. To create this compensation current the ISL6324A sets the voltage on the DVC pin to be 2x the voltage on the REF pin. Since the error amplifier forces the voltage on the FB pin and the REF pin to be equal, the resulting voltage across the series RC between DVC and FB is equal to the REF pin voltage. The RC compensation components, R_{DVC} and C_{DVC}, can then be selected to create the desired amount of compensation current.

The amount of compensation current required is dependant on the modulator gain of the system, K1, and the error amplifier RC components, R_C and C_C, that are in series between the FB and COMP pins. Use Equations 14, 15 and 16 to calculate the RC component values, R_{DVC} and C_{DVC}, for the VID-on-the-fly compensation network. For these equations: V_{IN} is the input voltage for the power train; V_{P-P} is the oscillator ramp amplitude (1.5V); and R_C and C_C are the error amplifier RC components between the FB and COMP pins.

$$A = \frac{K1}{K1 - 1} \quad \text{(EQ. 14)}$$

$$K1 = \frac{V_{IN}}{V_{P-P}}$$

$$R_{RCOMP} = A \times R_C \quad \text{(EQ. 15)}$$

$$C_{RCOMP} = \frac{C_C}{A} \quad \text{(EQ. 16)}$$

Advanced Adaptive Zero Shoot-Through Deadtime Control (Patent Pending)

The integrated drivers incorporate a unique adaptive deadtime control technique to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower

MOSFET body-diode conduction, and to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

During turn-off of the lower MOSFET, the PHASE voltage is monitored until it reaches a -0.3V/+0.8V (forward/reverse inductor current). At this time the UGATE is released to rise. An auto-zero comparator is used to correct the $r_{DS(ON)}$ drop in the phase voltage preventing false detection of the -0.3V phase level during $r_{DS(ON)}$ conduction period. In the case of zero current, the UGATE is released after 35ns delay of the LGATE dropping below 0.5V. When LGATE first begins to transition low, this quick transition can disturb the PHASE node and cause a false trip, so there is 20ns of blanking time once LGATE falls until PHASE is monitored.

Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn-on.

Initialization

Prior to initialization, proper conditions must exist on the EN, VCC, PVCC1_2, PVCC_NB, ISEN3-, and ISEN4- pins. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, the controller asserts VDDPWRGD.

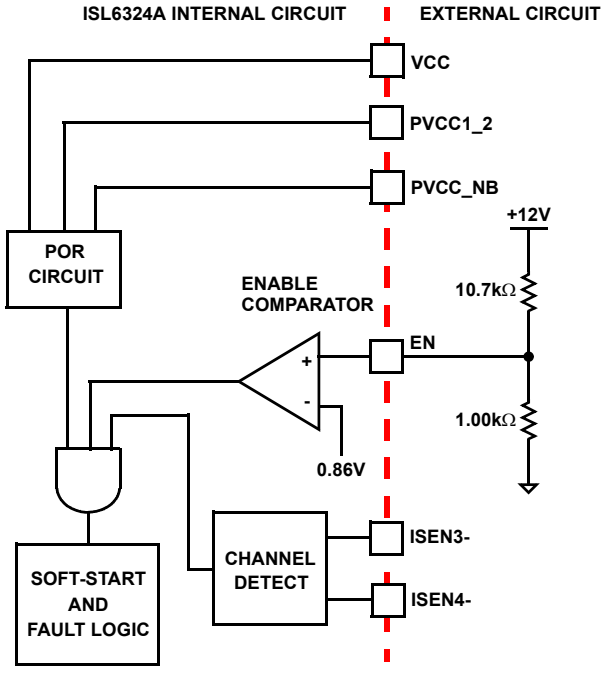


FIGURE 10. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

Power-On Reset

The ISL6324A requires VCC, PVCC1_2, and PVCC_NB inputs to exceed their rising POR thresholds before the ISL6324A has sufficient bias to guarantee proper operation.

The bias voltage applied to VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, the ISL6324A has enough bias to begin checking the driver POR inputs, EN, and channel detect portions of the initialization cycle. Hysteresis between the rising and falling thresholds assure the ISL6324A will not advertently turn off unless the bias voltage drops substantially (see “Electrical Specifications” on page 6).

The bias voltage applied to the PVCC1_2 and PVCC_NB pins power the internal MOSFET drivers of each output channel. In order for the ISL6324A to begin operation, both PVCC inputs must exceed their POR rising threshold to guarantee proper operation of the internal drivers. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6324A will not inadvertently turn off unless the PVCC bias voltage drops substantially (see “Electrical Specifications” on page 6). Depending on the number of active CORE channels determined by the Phase Detect block, the external driver POR checking is supported by the Enable Comparator.

Enable Comparator

The ISL6324A features a dual function enable input (EN) for enabling the controller and power sequencing between the controller and external drivers or another voltage rail. The enable comparator holds the ISL6324A in shutdown until the voltage at EN rises above 0.86V. The enable comparator has about 110mV of hysteresis to prevent bounce. It is important that the driver ICs reach their rising POR level before the ISL6324A becomes enabled. The schematic in Figure 10 demonstrates sequencing the ISL6324A with the ISL66xx family of Intersil MOSFET drivers, which require 12V bias.

When selecting the value of the resistor divider the driver maximum rising POR threshold should be used for calculating the proper resistor values. This will prevent improper sequencing events from creating false trips during soft-start.

If the controller is configured for 2-phase CORE operation, then the resistor divider can be used for sequencing the controller with another voltage rail. The resistor divider to EN should be selected using a similar approach as the previous driver discussion.

The EN pin is also used to force the ISL6324A into either PVI or SVI mode. The mode is set upon the rising edge of the EN signal. When the voltage on the EN pin rises above 0.86V, the mode will be set depending upon the status of the VID1/SEL pin.

Phase Detection

The ISEN3- and ISEN4- pins are monitored prior to soft-start to determine the number of active CORE channel phases.

If ISEN4- is tied to VCC, the controller will configure the channel firing order and timing for 3-phase operation. If ISEN3- and ISEN4- are tied to VCC, the controller will set the channel firing order and timing for 2-phase operation (see “PWM Operation” on page 12 for details). If Channel 4 and/or Channel 3 are disabled, then the corresponding PWMn and ISENn+ pins may be left unconnected

Soft-Start Output Voltage Targets

Once the POR and Phase Detect blocks and enable comparator are satisfied, the controller will begin the soft-start sequence and will ramp the CORE and NB output voltages up to the SVI interface designated target level if the controller is set SVI mode. If set to PVI mode, the North Bridge regulator is disabled and the core is soft started to the level designated by the parallel VID code.

SVI MODE

Prior to soft-starting both CORE and NB outputs, the ISL6324A must check the state of the SVI interface inputs to determine the correct target voltages for both outputs. When the controller is enabled, the state of the VFIXEN, SVD and SVC inputs are checked and the target output voltages set for both CORE and NB outputs are set by the DAC (see “Serial VID Interface (SVI)” on page 15). These targets will only change if the EN signal is pulled low or after a POR reset of VCC.

Soft-Start

The soft-start sequence is composed of three periods, as shown in Figure 11. At the beginning of soft-start, the DAC immediately obtains the output voltage targets for both outputs by decoding the state of the SVI or PVI inputs. A 100µs fixed delay time, TDA, proceeds the output voltage rise. After this delay period the ISL6324A will begin ramping both CORE and NB output voltages to the programmed DAC level at a fixed rate of 3.25mV/µs. The amount of time required to ramp the output voltage to the final DAC voltage is referred to as TDB, and can be calculated as shown in Equation 17.

$$TDB = \frac{V_{DAC}}{3.25 \times 10^{-3}} \quad \text{(EQ. 17)}$$

After the DAC voltage reaches the final VID setting, VDDPWRGD will be set to high.

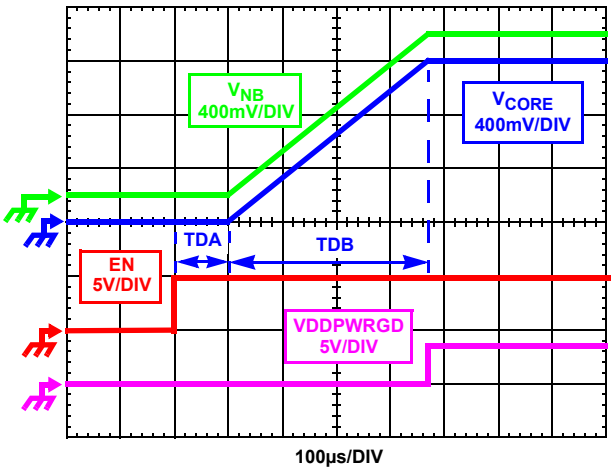


FIGURE 11. SOFT-START WAVEFORMS

Pre-Biased Soft-Start

The ISL6324A also has the ability to start up into a pre-charged output, without causing any unnecessary disturbance. The FB pin is monitored during soft-start, and should it be higher than the equivalent internal ramping reference voltage, the output drives hold both MOSFETs off.

Once the internal ramping reference exceeds the FB pin potential, the output drives are enabled, allowing the output to ramp from the pre-charged level to the final level dictated by the DAC setting. Should the output be pre-charged to a level exceeding the DAC setting, the output drives are enabled at the end of the soft-start period, leading to an abrupt correction in the output voltage down to the DAC-set level.

Both CORE and NB output support start up into a pre-charged output.

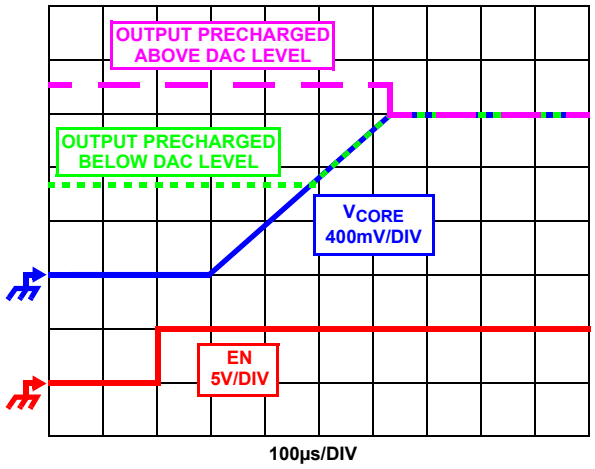


FIGURE 12. SOFT-START WAVEFORMS FOR ISL6324A-BASED MULTI-PHASE CONVERTER

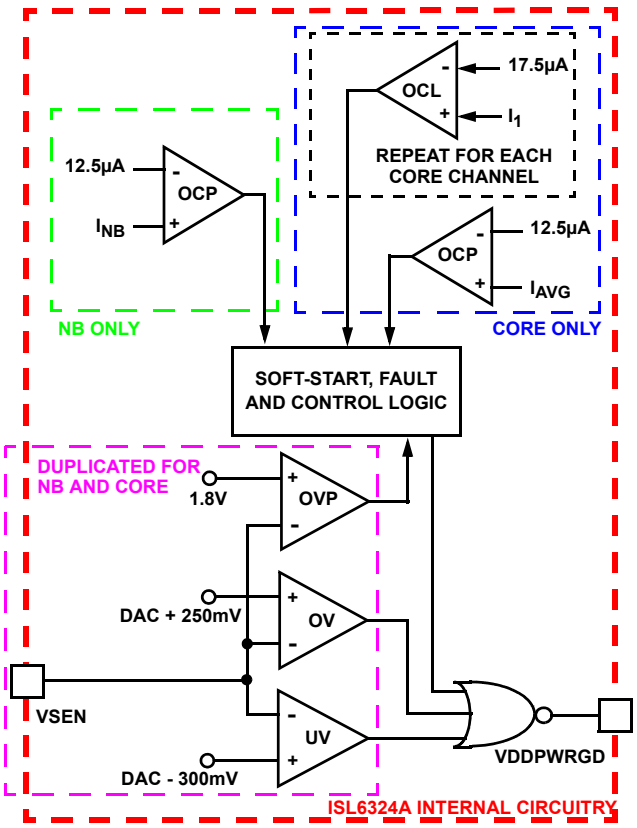


FIGURE 13. POWER-GOOD AND PROTECTION CIRCUITRY

Fault Monitoring and Protection

The ISL6324A actively monitors both CORE and NB output voltages and currents to detect fault conditions. Fault monitors trigger protective measures to prevent damage to either load. One common power-good indicator is provided for linking to external system monitors. The schematic in Figure 13 outlines the interaction between the fault monitors and the power good signal.

Power-Good Signal

The power good pin (VDDPWRGD) is an open-drain logic output that signals whether or not the ISL6324A is regulating both NB and CORE output voltages within the proper levels, and whether any fault conditions exist. This pin should be tied to a +5V source through a resistor.

During shutdown and soft-start, VDDPWRGD pulls low and releases high after a successful soft-start and both output voltages are operating between the undervoltage and overvoltage limits. VDDPWRGD transitions low when an undervoltage, overvoltage, or overcurrent condition is detected on either regulator output or when the controller is disabled by a POR reset or EN. In the event of an overvoltage or overcurrent condition, the controller latches off and VDDPWRGD will not return high. Pending a POR reset of the ISL6324A and successful soft-start, the VDDPWRGD will return high.

Overvoltage Protection

The ISL6324A constantly monitors the sensed output voltage on the VSEN pin to detect if an overvoltage event occurs. When the output voltage rises above the OVP trip level and exceeds the VDDPWRGD OV limit actions are taken by the ISL6324A to protect the microprocessor load.

At the inception of an overvoltage event, both on-board lower gate pins are commanded low as are the active PWM outputs to the external drivers, the VDDPWRGD signal is driven low, and the ISL6324A latches off normal PWM action. This turns on the all of the lower MOSFETs and pulls the output voltage below a level that might cause damage to the load. The lower MOSFETs remain driven ON until VDIFF falls below 400mV. The ISL6324A will continue to protect the load in this fashion as long as the overvoltage condition recurs. Once an overvoltage condition ends the ISL6324A latches off, and must be reset by toggling POR, before a soft-start can be re-initiated.

Pre-POR Overvoltage Protection

Prior to PVCC and VCC exceeding their POR levels, the ISL6324A is designed to protect either load from any overvoltage events that may occur. This is accomplished by means of an internal 10kΩ resistor tied from PHASE to LGATE, which turns on the lower MOSFET to control the output voltage until the overvoltage event ceases or the input power supply cuts off. For complete protection, the low side MOSFET should have a gate threshold well below the maximum voltage rating of the load/microprocessor.

In the event that during normal operation the PVCC or VCC voltage falls back below the POR threshold, the pre-POR overvoltage protection circuitry reactivates to protect from any more pre-POR overvoltage events.

Undervoltage Detection

The undervoltage threshold is set at VDAC - 300mV typical. When the output voltage (VSEN-RGND) is below the undervoltage threshold, VDDPWRGD gets pulled low. No other action is taken by the controller. VDDPWRGD will return high if the output voltage rises above VDAC - 250mV typical.

Open Sense Line Protection

In the case that either of the remote sense lines, VSEN or GND, become open, the ISL6324A is designed to detect this and shut down the controller. This event is detected by monitoring small currents that are fed out the VSEN and RGND pins. In the event of an open sense line fault, the controller will continue to remain off until the fault goes away, at which point the controller will re-initiate a soft-start sequence.

Overcurrent Protection

The ISL6324A takes advantage of the proportionality between the load current and the average current, I_{AVG}, to detect an overcurrent condition. See “Continuous Current Sampling” on page 13 and “Channel-Current Balance” on page 14 for more detail on how the average current is measured. Once the

average current exceeds 100µA, a comparator triggers the converter to begin overcurrent protection procedures. The Core regulator and the North Bridge regulator have the same type of overcurrent protection.

The overcurrent trip threshold is dictated by the DCR of the inductors, the number of active channels, the DC gain of the inductor RC filter and the R_{SET} resistor. The overcurrent trip threshold is shown in Equation 18.

$$I_{OCP} = 100\mu A \cdot \frac{N}{DCR} \cdot \frac{1}{K} \cdot \left(\frac{3}{400} \cdot R_{SET}\right) - \frac{V_{IN} - N \cdot V_{OUT}}{2 \cdot L \cdot f_S} \cdot \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 18)}$$

Where:

$K = \frac{R_2}{R_1 + R_2}$ See “Continuous Current Sampling” on page 13.

f_S = Switching Frequency

Equation 18 is valid for both the Core regulator and the North Bridge regulator. This equation includes the DC load current as well as the total ripple current contributed by all the phases. For the North Bridge regulator, N is 1.

During soft-start, the overcurrent trip point is boosted by a factor of 1.4. Instead of comparing the average measured current to 100µA, the average current is compared to 140µA. Immediately after soft-start is over, the comparison level changes to 100µA. This is done to allow for start-up into an active load while still supplying output capacitor in-rush current.

CORE REGULATOR OVERCURRENT

At the beginning of overcurrent shutdown, the controller sets all of the UGATE and LGATE signals low, puts PWM3 and PWM4 (if active) in a high-impedance state, and forces VDDPWRGD low. This turns off all of the upper and lower MOSFETs. The system remains in this state for fixed period of 12ms. If the controller is still enabled at the end of this wait period, it will attempt a soft-start, as shown in Figure 14. If the fault remains, the trip-retry cycles will continue until either the fault is cleared or for a total of seven attempts. If the fault is not cleared on the final attempt, the controller disables UGATE and LGATE signals for both Core and North Bridge and latches off requiring a POR of VCC to reset the ISL6324A.

It is important to note that during soft start, the overcurrent trip point is increased by a factor of 1.4. If the fault draws enough current to trip overcurrent during normal run mode, it may not draw enough current during the soft-start ramp period to trip overcurrent while the output is ramping up. If a fault of this type is affecting the output, then the regulator will complete soft-start and the trip-retry counter will be reset to zero. Once the regulator has completed soft-start, the overcurrent trip point will return to it’s nominal setting and an overcurrent shutdown will be initiated. This will result in a continuous hiccup mode.

Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard.

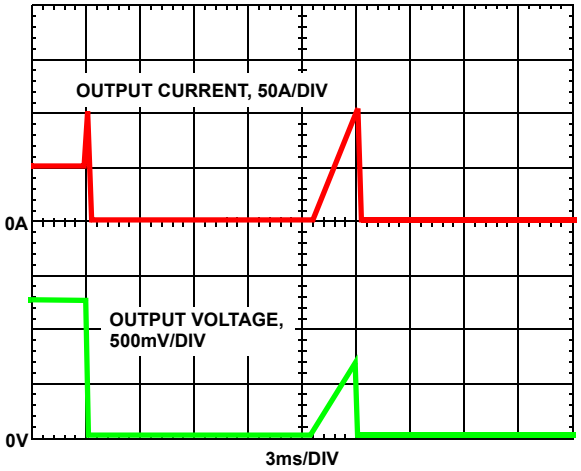


FIGURE 14. OVERCURRENT BEHAVIOR IN HICCUP MODE

NORTH BRIDGE REGULATOR OVERCURRENT

The overcurrent shutdown sequence for the North Bridge regulator is identical to the Core regulator with the exception that it is a single phase regulator and will only disable the MOSFET drivers for the North Bridge. Once 7 retry attempts have been executed unsuccessfully, the controller will disable UGATE and LGATE signals for both Core and North Bridge and will latch off requiring a POR of VCC to reset the ISL6324A.

Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard.

Individual Channel Overcurrent Limiting

The ISL6324A has the ability to limit the current in each individual channel of the Core regulator without shutting down the entire regulator. This is accomplished by continuously comparing the sensed currents of each channel with a constant 140µA OCL reference current. If a channel’s individual sensed current exceeds this OCL limit, the UGATE signal of that channel is immediately forced low, and the LGATE signal is forced high. This turns off the upper MOSFET(s), turns on the lower MOSFET(s), and stops the rise of current in that channel, forcing the current in the channel to decrease. That channel’s UGATE signal will not be able to return high until the sensed channel current falls back below the 140µA reference.

I^2C Bus Interface

The ISL6324A includes an I^2C bus interface which allows for user programmability of three of the controller’s operating parameters and programmability of the Power Savings Mode feature. The parameters that can be adjusted through the I^2C are:

1. **Voltage Margining Offset**: The DAC voltage can be offset in 25mV increments.

2. **VDDPWRGD Trip Level**: The PGOOD trip level for either the Core regulator or the North Bridge regulator can be increased.
3. **Overvoltage Trip Level**: The OVP trip level of either the Core or North Bridge regulator can be increased.
4. **Power Savings Mode Options:**
   a. The number of phases to drop to in Power Savings Mode can be programmed
   b. The number of PWM cycles between dropping phases while entering Power Savings Mode can be programmed.
   c. The number of PWM cycles between adding phases when exiting Power Savings Mode can be programmed.
   d. Core Voltage Margining Offset can be Enabled or Disabled while in Power Savings Mode.

To adjust these parameters, data transmission from the main microprocessor to the ISL6324A and vice versa must take place through the two wire I^2C bus interface. The two wires of the I^2C bus consist of the SDA line, over which all data is sent, and the SCL line, which is a clock signal used to synchronize sending/receiving of the data.

Both SDA and SCL are bidirectional lines, externally connected to a positive supply voltage via a pull-up resistor. Pull-up resistor values should be chosen to limit the input current to less then 3mA. When the bus is free, both lines are HIGH. The output stages of ISL6324A have an open drain/open collector in order to perform the wired-AND function. Data on the I^2C bus can be transferred up to 100Kbps in the standard-mode or up to 400Kbps in the fast-mode. The level of logic “0” and logic “1” is dependent on associated value of V_{DD} as per electrical specification table. One clock pulse is generated for each data bit transferred. The ISL6324A is a “SLAVE only” device, so the SCL line must always be controlled by an external master.

It is important to note that the I^2C interface of the ISL6324A only works once the voltage on the VCC pin has risen above the POR rising threshold. The I^2C will continue to remain active until the voltage on the VCC pin falls back below the falling POR threshold level.

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 15.

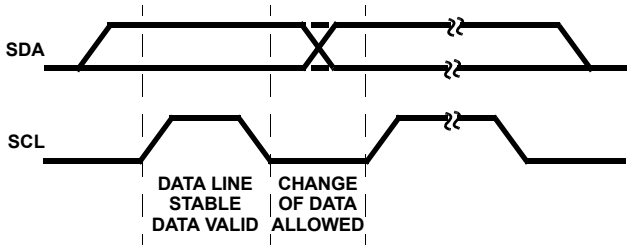


FIGURE 15. DATA VALIDITY

START and STOP Conditions

Figure 16 shows a START (S) condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP (P) condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition..

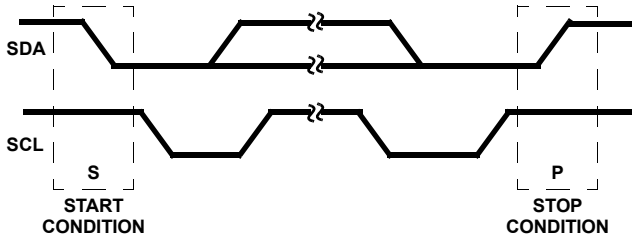


FIGURE 16. START AND STOP WAVEFORMS

Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB) and the least significant bit last (LSB).

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (A). After the start condition, the master sends 7 slave address bits and a R/W bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data as described in Figure 17.

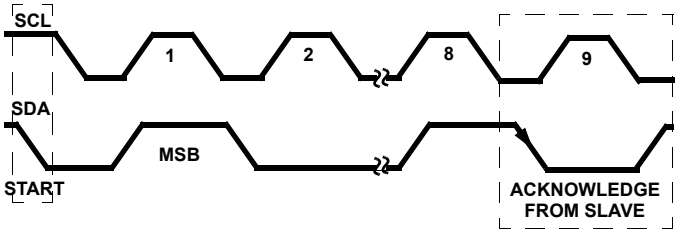


FIGURE 17. ACKNOWLEDGE ON THE I^2C BUS

ISL6324A I^2C Slave Address

All devices on the I^2C bus must have a 7-Bit I^2C address in order to be recognized. The address for the ISL6324A is 1000_110.

Communicating Over the I^2C Bus

Two transactions are supported on the I^2C interface:

1. Write register
2. Read register from current address.

All transactions start with a control byte sent from the I^2C master device. The control byte begins with a Start condition, followed by 7-Bits of slave address. The last bit sent by the

master is the R/W bit and is 0 for a write or 1 for a read. If any slaves on the I2C bus recognize their address, they will Acknowledge by pulling the serial data line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition.

Once the control byte is sent, and the ISL6324A acknowledges it, the 2nd byte sent by the master must be a register address byte. This register address byte tells the ISL6324A which one of the internal registers it wants to write to or read from. The address of the first internal register, RGS1, is 0000_0000. This register sets the North Bridge Offset, Overvoltage trip point and Power-good trip level. The address of the second internal register, RGS2, is 0000_0001. This register sets the Core Offset, Overvoltage trip point and Power-good trip level. The address of the third register, RGS3, is 0000_0010. The third register is for programming of the Power Savings Mode features. Once the ISL6324A receives a correct register address byte, it responds with an acknowledge.

TABLE 5. I2C REGISTER FUNCTIONS

REGISTER	ADDRESS	FUNCTION
RGS1	0000_0000	North Bridge DAC Offset, OVP, PGOOD
RGS2	0000_0001	Core DAC Offset, OVP, PGOOD
RGS3	0000_0010	Power Savings Mode Functionality

Writing to the Internal Registers

In order to change any of the three operating parameters via the I2C bus, the internal registers must be written to. The two registers inside the ISL6324A can be written individually with two separate write transactions or sequentially with one write transaction by sending two data bytes. See “Reading from the Internal Registers” on page 25.

To write to a single register in the ISL6324A, the master sends a control byte with the R/W bit set to 0, indicating a write. If it receives an Acknowledge from the ISL6324A, it sends a register address byte representing the internal register it wants to write to (0000_0000 for RGS1, 0000_0001 for RGS2 or 0000_0010 for RGS3). The ISL6324A will respond with an Acknowledge. The master then sends a byte representing the data byte to be written into the desired register. The ISL6324A will respond with an Acknowledge. The master then issues a Stop condition, indicating to the ISL6324A that the current transaction is complete. Once this transaction completes, the ISL6324A will immediately update and change the operating parameters on-the-fly.

It is also possible to write to the all the registers sequentially. To do this the master must write to register RGS1first. This transaction begins with the master sending a control byte with the R/W bit set to 0. If it receives an Acknowledge from the ISL6324A, it sends the register address byte 0000_0000, representing the internal register RGS1. The ISL6324A will respond with an Acknowledge. After sending the data byte to RGS1 and receiving an Acknowledge from the ISL6324A, instead of sending a Stop condition, the master sends the data byte to be stored in register RGS2. After the ISL6324A responds with another Acknowledge, the master can either send a Stop condition to indicate that the current transaction is complete, or it can send the data byte to be stored in register RGS3. If register RGS3 is written to, the ISL6324A will respond with an Acknowledge and the master would send a Stop condition, completing the transaction. Once this transaction completes the ISL6324A will immediately update and change the operating parameters on-the-fly.

Reading from the Internal Registers

The ISL6324A has the ability to read from both registers separately or read from them consecutively. Prior to reading from an internal register, the master must first select the desired register by writing to it and sending the register’s address byte. This process begins by the master sending a control byte with the R/W bit set to 0, indicating a write. Once it receives an Acknowledge from the ISL6324A, it sends a register address byte representing the internal register it wants to read from (0000_0000 for RGS1, 0000_0001 for RGS2 or 0000_0010 for RGS3). The ISL6324A will respond with an Acknowledge. The master must then respond with a Stop condition. After the Stop condition, the master follows with a new Start condition, and then sends a new control byte with the R/W bit set to 1, indicating a read. The ISL6324A will then respond by sending the master an Acknowledge, followed by the data byte stored in that register. The master must then send a Not Acknowledge followed by a Stop command, which will complete the read transaction.

It is also possible for all registers to be read consecutively. To do this the master must read from register RGS1 first. This transaction begins with the master sending a control byte with the R/W bit set to 0. If it receives an Acknowledge from the ISL6324A, it sends the register address byte 0000_0000, representing the internal register RGS1. The ISL6324A will respond with an Acknowledge. The master must then respond with a Stop condition. After the Stop condition the master follows with a new Start condition, and then sends a new control byte with the R/W bit set to 1, indicating a read. The ISL6324A will then respond by sending the master an Acknowledge, followed by the data byte stored in register RGS1. The master must then send an Acknowledge, and after doing so, the ISL6324A will respond by sending the data byte stored in register RGS2. The master must then send another Acknowledge, which the ISL6324A will respond to by sending the data byte stored in register RGS3. The master must then send a Not Acknowledge followed by a Stop command, which will complete the read transaction.

Resetting the Internal Registers

The ISL6324A’s internal I2C registers always initialize to the states shown in Table 6 when the controller first receives power. Once the voltage on the VCC pin rises above the POR rising threshold level, these registers can be changed at any

time via the I2C interface. If the voltage on the VCC pin falls below the POR falling threshold, the internal registers are automatically reset to their initial states.

TABLE 6. I2C REGISTER INITIAL STATES

REGISTER	ADDRESS	INITIAL STATE
RGS1	0000_0000	0000_0000
RGS2	0000_0001	0000_0000

TABLE 6. I2C REGISTER INITIAL STATES

REGISTER	ADDRESS	INITIAL STATE
RGS3	0000_0010	0000_0001

It is possible to reset the internal registers without powering down the controller and without requiring the controller to stop regulating and soft-start again. Simply write the initial states to the internal registers over the I2C interface.

I2C Read and Write Protocol

WRITE TO A SINGLE REGISTER

WRITE TO ALL REGISTERS

READ FROM SINGLE REGISTER

READ FROM ALL REGISTERS

DRIVEN BY MASTER — S = START CONDITION — A = ACKNOWLEDGE

DRIVEN BY ISL6324A — P = STOP CONDITION — N = NO ACKNOWLEDGE

Register Bit Definitions

The bits for RGS1 and RGS2 are utilized in the same manner by the ISL6324A (see Table 5). Bit-7 enables the overvoltage protection trip point to be increased. Bit-6 enables the Power-good trip point to be increased. These bits will be interpreted by the ISL6324A according to Table 7. Bits 5 through 0 determine the amount of offset for the particular regulator. See Table 8 for the bit codes and the corresponding offset voltages from the nominal DAC.

TABLE 7. BIT [7] AND [6] of REGISTER RGS1 AND RGS2

BIT 7	OVP TRIP LEVEL
0	1.8V or V_{DAC} + 250mV, whichever is greater
1	1.8V or V_{DAC} + 500mV, whichever is greater
BIT 6	**PGOOD TRIP LEVEL**
0	$VDAC_{CORE}$ +250mV/-300mV $VDAC_{NB}$ - 300mV
1	$VDAC_{CORE}$ +300mV/-350mV $VDAC_{NB}$ - 350mV

NOTE: All Pgood trip points have 50mV hysteresis

TABLE 8. BITS [5:0] REGISTER RGS1 and RGS2 (VOLTAGE MARGINING OFFSET)

BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	V_{OFFSET} (mV)
VO5	VO4	VO3	VO2	VO1	VO0	
1	0	0	0	0	0	-800
1	0	0	0	0	1	-775
1	0	0	0	1	0	-750
1	0	0	0	1	1	-725
1	0	0	1	0	0	-700
1	0	0	1	0	1	-675
1	0	0	1	1	0	-650
1	0	0	1	1	1	-625
1	0	1	0	0	0	-600
1	0	1	0	0	1	-575
1	0	1	0	1	0	-550
1	0	1	0	1	1	-525
1	0	1	1	0	0	-500
1	0	1	1	0	1	-475
1	0	1	1	1	0	-450
1	0	1	1	1	1	-425
1	1	0	0	0	0	-400
1	1	0	0	0	1	-375
1	1	0	0	1	0	-350
1	1	0	0	1	1	-325
1	1	0	1	0	0	-300
1	1	0	1	0	1	-275

TABLE 8. BITS [5:0] REGISTER RGS1 and RGS2 (VOLTAGE MARGINING OFFSET) (Continued)

BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	V_{OFFSET} (mV)
VO5	VO4	VO3	VO2	VO1	VO0	
1	1	0	1	1	0	-250
1	1	0	1	1	1	-225
1	1	1	0	0	0	-200
1	1	1	0	0	1	-175
1	1	1	0	1	0	-150
1	1	1	0	1	1	-125
1	1	1	1	0	0	-100
1	1	1	1	0	1	-75
1	1	1	1	1	0	-50
1	1	1	1	1	1	-25
0	0	0	0	0	0	0
0	0	0	0	0	1	25
0	0	0	0	1	0	50
0	0	0	0	1	1	75
0	0	0	1	0	0	100
0	0	0	1	0	1	125
0	0	0	1	1	0	150
0	0	0	1	1	1	175
0	0	1	0	0	0	200
0	0	1	0	0	1	225
0	0	1	0	1	0	250
0	0	1	0	1	1	275
0	0	1	1	0	0	300
0	0	1	1	0	1	325
0	0	1	1	1	0	350
0	0	1	1	1	1	375
0	1	0	0	0	0	400
0	1	0	0	0	1	425
0	1	0	0	1	0	450
0	1	0	0	1	1	475
0	1	0	1	0	0	500
0	1	0	1	0	1	525
0	1	0	1	1	0	550
0	1	0	1	1	1	575
0	1	1	0	0	0	600
0	1	1	0	0	1	625
0	1	1	0	1	0	650
0	1	1	0	1	1	675
0	1	1	1	0	0	700
0	1	1	1	0	1	725

TABLE 8. BITS [5:0] REGISTER RGS1 and RGS2 (VOLTAGE MARGINING OFFSET) (Continued)

BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	V_{OFFSET} (mV)
VO5	VO4	VO3	VO2	VO1	VO0	
0	1	1	1	1	0	750
0	1	1	1	1	1	775

The bits for Register RGS3 control some of the functionality of the ISL6324A for Power Savings Mode. Bits 0 and 1 control the number of phases that the ISL6324A will drop to when in Power Savings Mode. Bits 2 and 3 control the number of PWM cycles between adding of phases when exiting Power Savings Mode. Bits 4 and 5 control the number of PWM cycles between dropping of phases when entering Power Savings Mode. Bit 6 will disable/enable the Core DAC offset when in Power Savings Mode. Bit 7 is reserved. See Table 9 for a complete description of register RGS3 bits and their functionality.

TABLE 9. BITS [7:0] REGISTER RGS3

Bit 7	**Reserved**
Bit 6	**Core DAC Offset**
0	ENABLED
1	DISABLED
Bits [5:4]	**Number of PWM Cycles Between Dropping Phases**
00	1 PWM Cycle (default)
01	2 PWM Cycles
10	4 PWM Cycles
11	0 PWM Cycles (All Phases Drop at Once)
Bits [3:2]	**Number of PWM Cycles Between Adding Phases**
00	1 PWM Cycle (Default)
01	2 PWM Cycles
10	4 PWM Cycles
11	0 PWM Cycles (All Phases Added at Once)
Bits [1:0]	**Number of Phases Active in Power Savings Mode**
00	1 Phase
01	2 Phases (Default)
1X	3 Phases

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multi-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following sections. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

Power Stages

The first step in designing a multi-phase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board, whether through-hole components are permitted, the total board space available for power-supply circuitry, and the maximum amount of load current. Generally speaking, the most economical solutions are those in which each phase handles between 25A and 30A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat dissipating surfaces.

MOSFETS

The choice of MOSFETs depends on the current each MOSFET will be required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for power loss in the lower MOSFET is simple, since virtually all of the loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 19, I_M is the maximum continuous output current, I_{P-P} is the peak-to-peak inductor current (see Equation 20), and d is the duty cycle (V_{OUT}/V_{IN}).

$$P_{LOW,1} = r_{DS(ON)} \cdot \left[\left(\frac{I_M}{N}\right)^2 \cdot (1-d) + \frac{I_{L(P-P)}^2 \cdot (1-d)}{12}\right] \quad \text{(EQ. 19)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$, the switching frequency, f_S, and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)} \cdot f_S \cdot \left[\left(\frac{I_M}{N} + \frac{I_{P-P}}{2}\right) \cdot t_{d1} + \left(\frac{I_M}{N} - \frac{I_{P+P}}{2}\right) \cdot t_{d2}\right] \quad \text{(EQ. 20)}$$

The total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$ and $P_{LOW,2}$.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate

components involving the upper-MOSFET switching times, the lower-MOSFET body-diode reverse recovery charge, Q_{rr}, and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 21, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP(1)}$.

$$P_{UP(1)} \approx V_{IN} \cdot \left(\frac{I_M}{N} + \frac{I_{P-P}}{2}\right) \cdot \left(\frac{t_1}{2}\right) \cdot f_S \quad \text{(EQ. 21)}$$

At turn-on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 22, the approximate power loss is $P_{UP(2)}$.

$$P_{UP(2)} \approx V_{IN} \cdot \left(\frac{I_M}{N} - \frac{I_{P-P}}{2}\right) \cdot \left(\frac{t_2}{2}\right) \cdot f_S \quad \text{(EQ. 22)}$$

A third component involves the lower MOSFET reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET body diode can recover all of Q_{rr}, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is $P_{UP(3)}$ as shown in Equation 23.

$$P_{UP(3)} = V_{IN} \cdot Q_{rr} \cdot f_S \quad \text{(EQ. 23)}$$

Finally, the resistive part of the upper MOSFET is given in Equation 24 as $P_{UP(4)}$.

$$P_{UP(4)} \approx r_{DS(ON)} \cdot \left[\left(\frac{I_M}{N}\right)^2 \cdot d + \frac{I_{P-P}^2}{12}\right] \quad \text{(EQ. 24)}$$

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 21, 22, 23 and 24. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

Internal Bootstrap Device

All three integrated drivers feature an internal bootstrap Schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the PHASE node. This reduces voltage stress on the boot to phase pins.

The bootstrap capacitor must have a maximum voltage rating above PVCC + 4V and its capacitance value can be chosen from Equation 25:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \quad \text{(EQ. 25)}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet PVCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

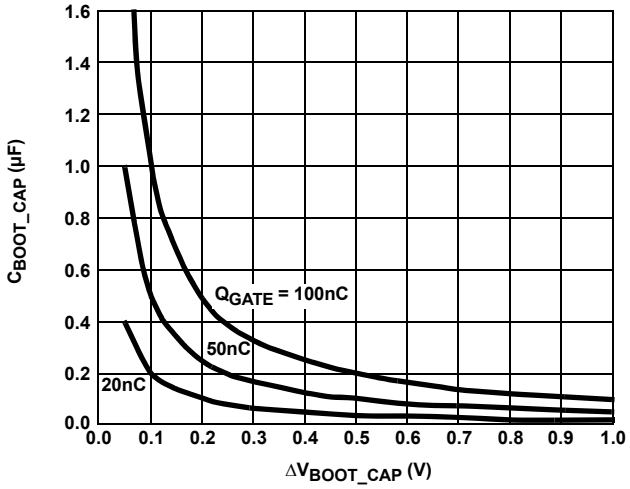


FIGURE 18. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Gate Drive Voltage Versatility

The ISL6324A provides the user flexibility in choosing the gate drive voltage for efficiency optimization. The controller ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

Package Power Dissipation

When choosing MOSFETs it is important to consider the amount of power being dissipated in the integrated drivers located in the controller. Since there are a total of three drivers in the controller package, the total power dissipated by all three drivers must be less than the maximum allowable power dissipation for the QFN package.

Calculating the power dissipation in the drivers for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for the 7x7 QFN package is approximately 3.5W at room temperature. See “Layout Considerations” on page 36 for thermal transfer improvement suggestions.

When designing the ISL6324A into an application, it is recommended that the following calculations is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses, P_{Qg_TOT}, due to the gate charge of MOSFETs and the integrated driver’s

internal circuitry and their corresponding average driver current can be estimated with Equations 26 and 27, respectively.

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \cdot VCC \quad \text{(EQ. 26)}$$

$$P_{Qg\_Q1} = \frac{3}{2} \cdot Q_{G1} \cdot PVCC \cdot f_{SW} \cdot N_{Q1} \cdot N_{PHASE}$$

$$P_{Qg\_Q2} = Q_{G2} \cdot PVCC \cdot f_{SW} \cdot N_{Q2} \cdot N_{PHASE}$$

$$I_{DR} = \left(\frac{3}{2} \cdot Q_{G1} \cdot N_{Q1} + Q_{G2} \cdot N_{Q2}\right) \cdot N_{PHASE} \cdot f_{SW} + I_Q \quad \text{(EQ. 27)}$$

In Equations 26 and 27, P_{Qg_Q1} is the total upper gate drive power loss and P_{Qg_Q2} is the total lower gate drive power loss; the gate charge (Q_{G1} and Q_{G2}) is defined at the particular gate to source drive voltage PVCC in the corresponding MOSFET data sheet; I_Q is the driver total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are the number of upper and lower MOSFETs per phase, respectively; N_{PHASE} is the number of active phases. The I_Q*VCC product is the quiescent power of the controller without capacitive load and is typically 75mW at 300kHz.

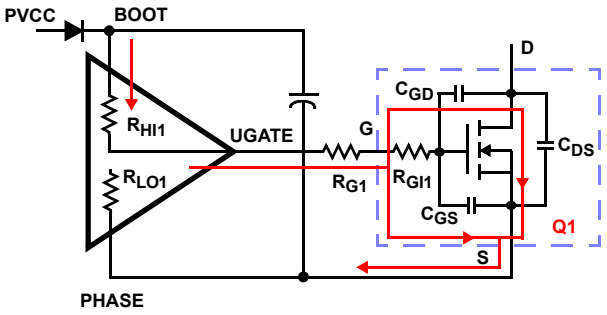


FIGURE 19. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

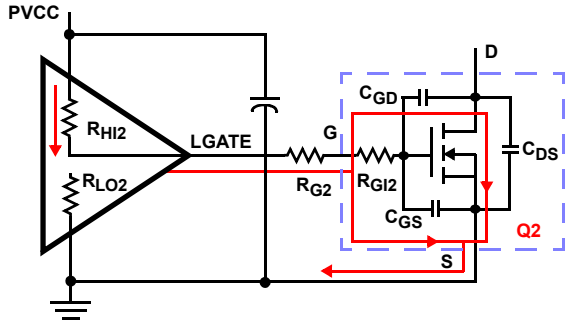


FIGURE 20. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

The total gate drive power losses are dissipated among the resistive components along the transition path and in the bootstrap diode. The portion of the total power dissipated in the controller itself is the power dissipated in the upper drive path resistance (P_{DR_UP}) the lower drive path resistance (P_{DR_UP}) and in the boot strap diode (P_{BOOT}). The rest of the power will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of the MOSFETs. Figures 19 and 20 show the typical upper and lower gate drives turn-on transition path. The total power dissipation in the controller itself, P_{DR}, can be roughly estimated as Equation 28:

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + P_{BOOT} + (I_Q \cdot VCC)$$

$$P_{BOOT} = \frac{P_{Qg\_Q1}}{3} \quad \text{(EQ. 28)}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \cdot \frac{P_{Qg\_Q1}}{3}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \cdot \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

Inductor DCR Current Sensing Component Selection and R_{SET} Value Calculation

With the single R_{SET} resistor setting the value of the effective internal sense resistors for both the North Bridge and Core regulators, it is important to set the R_{SET} value and the inductor RC filter gain, K, properly. See “Continuous Current Sampling” on page 13 and “Channel-Current Balance” on page 14 for more details on the application of the R_{SET} resistor and the RC filter gain.

There are 3 separate cases to consider when calculating these component values. If the system under design will never utilize the North Bridge regulator and the ISL6323 will always be in parallel mode, then follow the instructions for Case 3 and only calculate values for Core regulator components.

For all three cases, use the expected VID voltage that would be used at TDC for Core and North Bridge for the V_{CORE} and V_{NB} variables, respectively.

CASE 1

$$I_{NB_{MAX}} \cdot DCR_{NB} < \frac{I_{Core_{MAX}}}{N} \cdot DCR_{Core} \quad \text{(EQ. 29)}$$

In Case 1, the DC voltage across the North Bridge inductor at full load is less than the DC voltage across a single phase of the Core regulator while at full load. Here, the DC voltage across the Core inductors must be scaled down to match the DC voltage across the North Bridge inductor, which will be impressed across the ISEN_NB pins without any gain. Thus, the R_2 resistor for the North Bridge inductor RC filter is left unpopulated and K = 1.

3. Choose a capacitor value for the North Bridge RC filter. A 0.1µF capacitor is a recommended starting point.
4. Calculate the value for resistor R_1 using Equation 30:

$$R_{1_{NB}} = \frac{L_{NB}}{DCR_{NB} \cdot C_{NB}} \quad \text{(EQ. 30)}$$

5. Calculate the value for the R_{SET} resistor using Equation 31:

$$R_{SET} = \frac{400}{3} \cdot \frac{DCR_{NB} \cdot K}{100\mu A} \cdot \left(I_{OCP_{NB}} + \frac{V_{IN} - V_{NB}}{2 \cdot L_{NB} \cdot f_S} \cdot \frac{V_{NB}}{V_{IN}} \right) \quad \text{(EQ. 31)}$$

Where: K = 1

(Derived from Equation 18).

6. Using Equation 32 (also derived from Equation 18), calculate the value of K for the Core regulator.

$$K = \frac{3}{400} \cdot R_{SET} \cdot \frac{N}{DCR_{CORE}} \cdot \frac{100\mu A}{I_{OCP_{CORE}} + \frac{V_{IN} - N \cdot V_{CORE}}{2 \cdot L_{CORE} \cdot f_S} \cdot \frac{V_{CORE}}{V_{IN}}} \quad \text{(EQ. 32)}$$

7. Choose a capacitor value for the Core RC filters. A 0.1µF capacitor is a recommended starting point.
8. Calculate the values for R_1 and R_2 for Core. Equations 33 and 34 will allow for their computation.

$$K = \frac{R_{2_{Core}}}{R_{1_{Core}} + R_{2_{Core}}} \quad \text{(EQ. 33)}$$

$$\frac{L_{Core}}{DCR_{Core}} = \frac{R_{1_{Core}} \cdot R_{2_{Core}}}{R_{1_{Core}} + R_{2_{Core}}} \cdot C_{Core} \quad \text{(EQ. 34)}$$

CASE 2

$$I_{NB_{MAX}} \cdot DCR_{NB} > \frac{I_{Core_{MAX}}}{N} \cdot DCR_{Core} \quad \text{(EQ. 35)}$$

In Case 2, the DC voltage across the North Bridge inductor at full load is greater than the DC voltage across a single phase of the Core regulator while at full load. Here, the DC voltage across the North Bridge inductor must be scaled down to match the DC voltage across the Core inductors, which will be impressed across the ISEN pins without any gain. So, the R_2 resistor for the Core inductor RC filters is left unpopulated and K = 1.

1. Choose a capacitor value for the Core RC filter. A 0.1µF capacitor is a recommended starting point.
2. Calculate the value for resistor R_1:

$$R_{1_{Core}} = \frac{L_{Core}}{DCR_{Core} \cdot C_{Core}} \quad \text{(EQ. 36)}$$

3. Calculate the value for the R_{SET} resistor using Equation 37:(Derived from Equation 18).

$$R_{SET} = \frac{400}{3} \cdot \frac{DCR_{CORE} \cdot K}{100\mu A \cdot N} \cdot \left(I_{OCP_{CORE}} + \frac{V_{IN} - V_{CORE}}{2 \cdot L_{CORE} \cdot f_S} \cdot \frac{V_{CORE}}{V_{IN}} \right)$$

Where: K = 1 (EQ. 37)

4. Using Equation 38 (also derived from Equation 18), calculate the value of K for the North bridge regulator.

$$K = \frac{3}{400} \cdot R_{SET} \cdot \frac{1}{DCR_{NB}} \cdot \frac{100\mu A}{I_{OCP_{NB}} + \frac{V_{IN} - V_{NB}}{2 \cdot L_{NB} \cdot f_S} \cdot \frac{V_{NB}}{V_{IN}}} \quad \text{(EQ. 38)}$$

5. Choose a capacitor value for the North Bridge RC filter. A 0.1µF capacitor is a recommended starting point.
6. Calculate the values for R_1 and R_2 for North Bridge. Equations 39 and 40 will allow for their computation.

$$K = \frac{R_{2_{NB}}}{R_{1_{NB}} + R_{2_{NB}}} \quad \text{(EQ. 39)}$$

$$\frac{L_{NB}}{DCR_{NB}} = \frac{R_{1_{NB}} \cdot R_{2_{NB}}}{R_{1_{NB}} + R_{2_{NB}}} \cdot C_{NB} \quad \text{(EQ. 40)}$$

CASE 3

$$I_{NB_{MAX}} \cdot DCR_{NB} = \frac{I_{Core_{MAX}}}{N} \cdot DCR_{Core} \quad \text{(EQ. 41)}$$

In Case 3, the DC voltage across the North Bridge inductor at full load is equal to the DC voltage across a single phase of the Core regulator while at full load. Here, the full scale DC inductor voltages for both North Bridge and Core will be impressed across the ISEN pins without any gain. So, the R_2 resistors for the Core and North Bridge inductor RC filters are left unpopulated and K = 1 for both regulators.

For this Case, it is recommended that the overcurrent trip point for the North Bridge regulator be equal to the overcurrent trip point for the Core regulator divided by the number of core phases.

1. Choose a capacitor value for the North Bridge RC filter. A 0.1µF capacitor is a recommended starting point.
2. Calculate the value for the North Bridge resistor R_1:

$$R_{1_{NB}} = \frac{L_{NB}}{DCR_{NB} \cdot C_{NB}} \quad \text{(EQ. 42)}$$

3. Choose a capacitor value for the Core RC filter. A 0.1µF capacitor is a recommended starting point.
4. Calculate the value for the Core resistor R_1:

$$R_{1_{Core}} = \frac{L_{Core}}{DCR_{Core} \cdot C_{Core}} \quad \text{(EQ. 43)}$$

5. Calculate the value for the R_{SET} resistor using Equation 44:

$$R_{SET} = \frac{400}{3} \cdot \frac{DCR_{CORE} \cdot K}{100\mu A \cdot N} \cdot \left(I_{OCP_{CORE}} + \frac{V_{IN} - V_{CORE}}{2 \cdot L_{CORE} \cdot f_S} \cdot \frac{V_{CORE}}{V_{IN}} \right)$$

Where: K = 1 (EQ. 44)

6. Calculate the OCP trip point for the North Bridge regulator using Equation 45. If the OCP trip point is higher than desired, then the component values must be recalculated utilizing Case 1. If the OCP trip point is lower than desired,

then the component values must be recalculated utilizing Case 2.

$$I_{OCP_{NB}} = 100\mu A \cdot \frac{1}{DCR_{NB}} \cdot \left(\frac{3}{400} \cdot R_{SET}\right) + \frac{V_{IN} - V_{NB}}{2 \cdot L_{NB} \cdot f_S} \cdot \frac{V_{NB}}{V_{IN}} \quad \text{(EQ. 45)}$$

NOTE: The values of R_{SET} must be greater than 20kΩ and less than 80kΩ. For all of the 3 cases, if the calculated value of R_{SET} is less than 20kΩ, then either the OCP trip point needs to be increased or the inductor must be changed to an inductor with higher DCR. If the R_{SET} resistor is greater than 80kΩ, then a value of R_{SET} that is less than 80kΩ must be chosen and a resistor divider across both North Bridge and Core inductors must be set up with proper gain. This gain will represent the variable “K” in all equations. It is also very important that the R_{SET} resistor be tied between the RSET pin and the VCC pin of the ISL6323.

Inductor DCR Current Sensing Component Fine Tuning

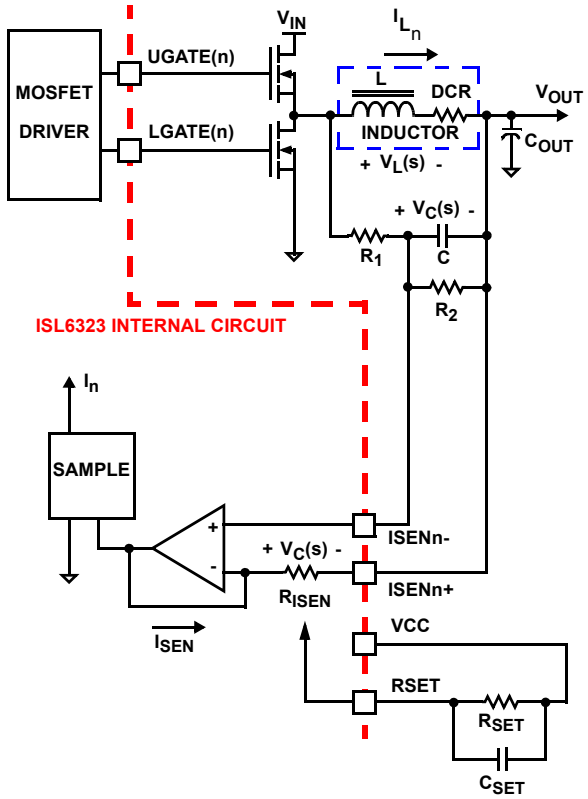


FIGURE 21. DCR SENSING CONFIGURATION

Due to errors in the inductance and/or DCR it may be necessary to adjust the value of R_1 and R_2 to match the time constants correctly. The effects of time constant mismatch can be seen in the form of droop overshoot or undershoot during the initial load transient spike, as shown in Figure 22. Follow the steps below to ensure the RC and inductor L/DCR time constants are matched accurately.

1. If the regulator is not utilizing droop, modify the circuit by placing the frequency set resistor between FS and Ground for the duration of this procedure.
2. Capture a transient event with the oscilloscope set to about L/DCR/2 (sec/div). For example, with L = 1µH and DCR = 1mΩ, set the oscilloscope to 500µs/div.
3. Record ΔV1 and ΔV2 as shown in Figure 22. Select new values, $R_{1(NEW)}$ and $R_{2(NEW)}$ for the time constant resistors based on the original values, $R_{1(OLD)}$ and $R_{2(OLD)}$ using Equations 46 and 47.

$$R_{1(NEW)} = R_{1(OLD)} \cdot \frac{\Delta V_1}{\Delta V_2} \quad \text{(EQ. 46)}$$

$$R_{2(1)(NEW)} = R_{2(OLD)} \cdot \frac{\Delta V_1}{\Delta V_2} \quad \text{(EQ. 47)}$$

4. Replace R_1 and R_2 with the new values and check to see that the error is corrected. Repeat the procedure if necessary.

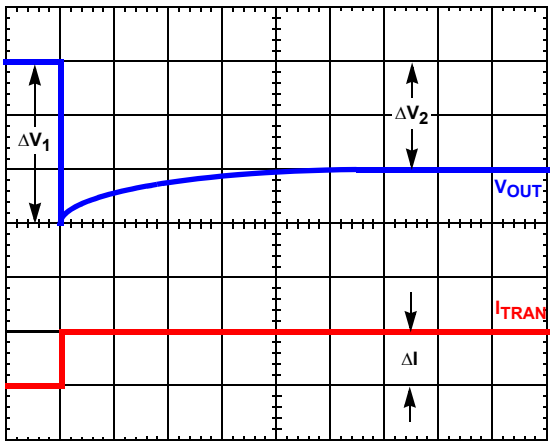


FIGURE 22. TIME CONSTANT MISMATCH BEHAVIOR

Loadline Regulation Resistor

The loadline regulation resistor, labeled R_{FB} in Figure 8, sets the desired loadline required for the application. Equation 48 can be used to calculate R_{FB}.

$$R_{FB} = \frac{V_{DROOP_{MAX}}}{\frac{400}{3} \cdot \frac{I_{OUT_{MAX}}}{N} \cdot \frac{DCR}{R_{SET}} \cdot K} \quad \text{(EQ. 48)}$$

Where K is defined in Equation 7.

If no loadline regulation is required, FS resistor should be tied between the FS pin and VCC. To choose the value for R_{FB} in

this situation, please refer to “Compensation Without Loadline Regulation” on page 33.

Compensation With Loadline Regulation

The load-line regulated converter behaves in a similar manner to a peak current mode controller because the two poles at the output filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C.

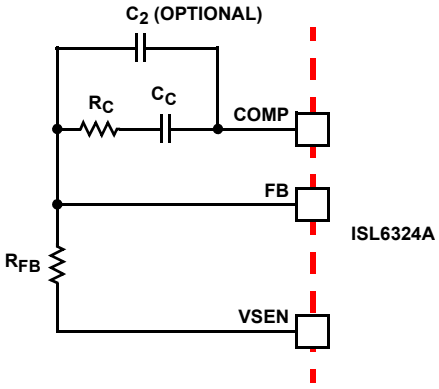


FIGURE 23. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL6324A CIRCUIT

Since the system poles and zero are affected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately, there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator, by compensating the L-C poles and the ESR zero of the voltage mode approximation, yields a solution that is always stable with very close to ideal transient performance.

Select a target bandwidth for the compensated system, f_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of f_0 to the L-C pole frequency and the ESR zero frequency. For each of the following three, there is a separate set of equations for the compensation components.

In Equation 49, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent series resistance of the bulk output filter capacitance; and V_{P-P} is the peak-to-peak sawtooth signal amplitude as described in the “Electrical Specifications” table on page 6.

Once selected, the compensation values in Equation 49 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_C. Slowly increase the value of R_C while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_C will not need adjustment. Keep the value of C_C from Equation 49 unless some performance issue is noted.

The optional capacitor C_2, is sometimes needed to bypass noise away from the PWM comparator (see Figure 23). Keep a position available for C_2, and be prepared to install a high frequency capacitor of between 22pF and 150pF in case any leading edge jitter problem is noted.

Case 1:

$$\frac{1}{2\cdot\pi\cdot\sqrt{L\cdot C}} > f_0$$

$$R_C = R_{FB}\cdot\frac{2\cdot\pi\cdot f_0\cdot V_{P\text{-}P}\cdot\sqrt{L\cdot C}}{0.66\cdot V_{IN}}$$

$$C_C = \frac{0.66\cdot V_{IN}}{2\cdot\pi\cdot V_{P\text{-}P}\cdot R_{FB}\cdot f_0}$$

Case 2:

$$\frac{1}{2\cdot\pi\cdot\sqrt{L\cdot C}} \le f_0 < \frac{1}{2\cdot\pi\cdot C\cdot ESR}$$

$$R_C = R_{FB}\cdot\frac{V_{PP}\cdot(2\cdot\pi)^2\cdot f_0^2\cdot L\cdot C}{0.66\cdot V_{IN}} \qquad \text{(EQ. 49)}$$

$$C_C = \frac{0.66\cdot V_{IN}}{(2\cdot\pi)^2\cdot f_0^2\cdot V_{P\text{-}P}\cdot R_{FB}\cdot\sqrt{L\cdot C}}$$

Case 3:

$$f_0 > \frac{1}{2\cdot\pi\cdot C\cdot ESR}$$

$$R_C = R_{FB}\cdot\frac{2\cdot\pi\cdot f_0\cdot V_{P\text{-}P}\cdot L}{0.66\cdot V_{IN}\cdot ESR}$$

$$C_C = \frac{0.66\cdot V_{IN}\cdot ESR\cdot\sqrt{C}}{2\cdot\pi\cdot V_{P\text{-}P}\cdot R_{FB}\cdot f_0\cdot\sqrt{L}}$$

Compensation Without Loadline Regulation

The non load-line regulated converter is accurately modeled as a voltage-mode regulator with two poles at the L-C resonant frequency and a zero at the ESR frequency. A type-III controller, as shown in Figure 24, provides the necessary compensation.

The first step is to choose the desired bandwidth, f_0, of the compensated system. Choose a frequency high enough to assure adequate transient performance but not higher than 1/3 of the switching frequency. The type-III compensator has an extra high-frequency pole, f_{HF}. This pole can be used for added noise rejection or to assure adequate attenuation at the error amplifier high-order pole and zero frequencies. A good general rule is to choose $f_{HF} = 10f_0$, but it can be higher if desired. Choosing f_{HF} to be lower than $10f_0$ can cause problems with too much phase shift below the system bandwidth as shown in Equation 50.

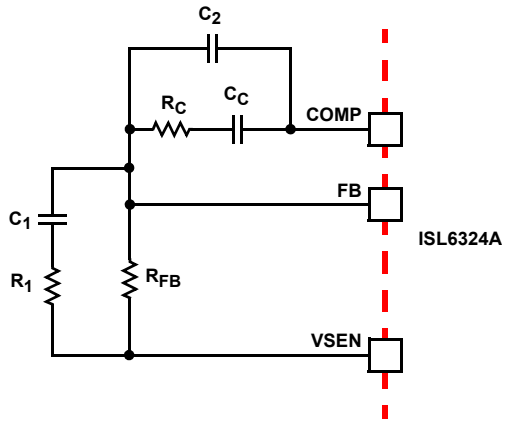


FIGURE 24. COMPENSATION CIRCUIT WITHOUT LOAD-LINE REGULATION

$$R_1 = R_{FB} \cdot \frac{C \cdot ESR}{\sqrt{L \cdot C} - C \cdot ESR} \qquad \text{(EQ. 50)}$$

$$C_1 = \frac{\sqrt{L \cdot C} - C \cdot ESR}{R_{FB}}$$

$$C_2 = \frac{0.75 \cdot V_{IN}}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{P-P}}$$

$$R_C = \frac{V_{PP} \cdot (2\pi)^2 \cdot f_0 \cdot f_{HF} \cdot L \cdot C \cdot R_{FB}}{0.75 \cdot V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)}$$

$$C_C = \frac{0.75 \cdot V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{P-P}}$$

In the solutions to the compensation equations, there is a single degree of freedom. For the solutions presented in Equation 51, R_{FB} is selected arbitrarily. The remaining compensation components are then selected according to Equation 51.

In Equation 51, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{P-P} is the peak-to-peak sawtooth signal amplitude as described in “Electrical Specifications” on page 6.

Output Filter Design

Case 1:

$$\frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} > f_0$$

$$R_C = R_{FB} \cdot \frac{2 \cdot \pi \cdot f_0 \cdot V_{P-P} \cdot \sqrt{L \cdot C}}{0.66 \cdot V_{IN}}$$

$$C_C = \frac{0.66 \cdot V_{IN}}{2 \cdot \pi \cdot V_{P-P} \cdot R_{FB} \cdot f_0}$$

Case 2:

$$\frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \leq f_0 < \frac{1}{2 \cdot \pi \cdot C \cdot ESR}$$

$$R_C = R_{FB} \cdot \frac{V_{P-P} \cdot (2 \cdot \pi)^2 \cdot f_0^2 \cdot L \cdot C}{0.66 \cdot V_{IN}} \qquad \text{(EQ. 51)}$$

$$C_C = \frac{0.66 \cdot V_{IN}}{(2 \cdot \pi)^2 \cdot f_0^2 \cdot V_{P-P} \cdot R_{FB} \cdot \sqrt{L \cdot C}}$$

Case 3:

$$f_0 > \frac{1}{2 \cdot \pi \cdot C \cdot ESR}$$

$$R_C = R_{FB} \cdot \frac{2 \cdot \pi \cdot f_0 \cdot V_{P-P} \cdot L}{0.66 \cdot V_{IN} \cdot ESR}$$

$$C_C = \frac{0.66 \cdot V_{IN} \cdot ESR \cdot \sqrt{C}}{2 \cdot \pi \cdot V_{P-P} \cdot R_{FB} \cdot f_0 \cdot \sqrt{L}}$$

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter limits the system transient response. The output capacitors must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI, the load-current slew rate, di/dt, and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount as shown in Equation 52:

$$\Delta V \approx ESL \cdot \frac{di}{dt} + ESR \cdot \Delta I \qquad \text{(EQ. 52)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-

frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see "Interleaving" on page 11 and Equation 3), a voltage develops across the bulk capacitor ESR equal to $I_{C(P-P)}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{P-P(MAX)}$, determines the lower limit on the inductance.

$$L \geq ESR \cdot \frac{\left(V_{IN} - N \cdot V_{OUT}\right) \cdot V_{OUT}}{f_S \cdot V_{IN} \cdot V_{P-P(MAX)}} \quad \text{(EQ. 53)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 54 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 55 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2 \cdot N \cdot C \cdot V_O}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \quad \text{(EQ. 54)}$$

$$L \leq \frac{1.25 \cdot N \cdot C}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \cdot \left(V_{IN} - V_O\right) \quad \text{(EQ. 55)}$$

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper MOSFET loss calculation. These effects are outlined in "MOSFETs" on page 28, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in "Output Filter Design" on page 34. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Switching frequency is determined by the selection of the frequency-setting resistor, R_T. Figure 25 and Equation 56 are provided to assist in selecting the correct value for R_T.

$$R_T = 10^{[10.61 - (1.035 \cdot \log(f_S))]} \quad \text{(EQ. 56)}$$

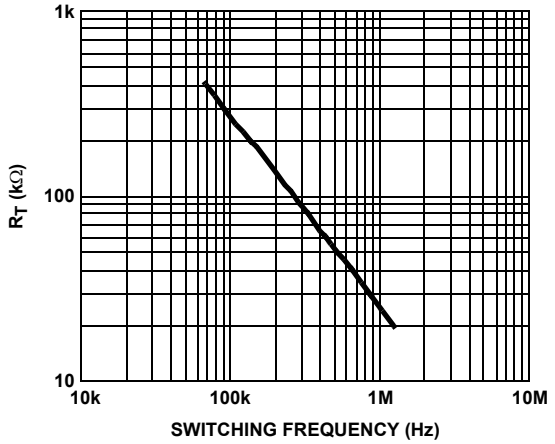


FIGURE 25. R_T vs SWITCHING FREQUENCY

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

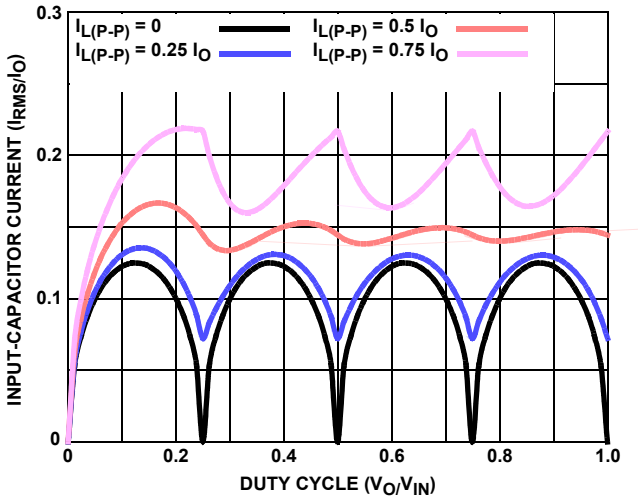


FIGURE 26. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 4-PHASE CONVERTER

For a 4-phase design, use Figure 26 to determine the input-capacitor RMS current requirement set by the duty cycle, maximum sustained output current (I_O), and the ratio of the peak-to-peak inductor current ($I_{L(P-P)}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated.

The voltage rating of the capacitors should also be at least 1.25x greater than the maximum input voltage. Figures 27 and 28 provide the same input RMS current information for 3-phase and two-phase designs respectively. Use the same approach for selecting the bulk capacitor type and number.

Low capacitance, high-frequency ceramic capacitors are needed in addition to the input bulk capacitors to suppress leading and falling edge voltage spikes. The spikes result from the high current slew rate produced by the upper MOSFET turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitics and maximize suppression.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component selection, layout, and placement minimizes these voltage spikes. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET was carrying channel current. During the turn-off, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

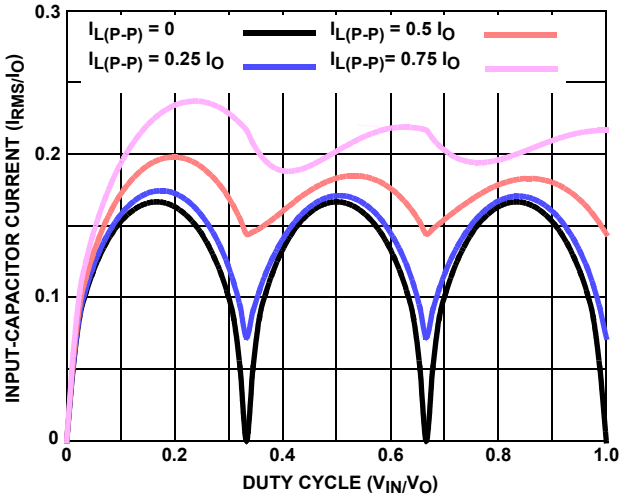


FIGURE 27. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

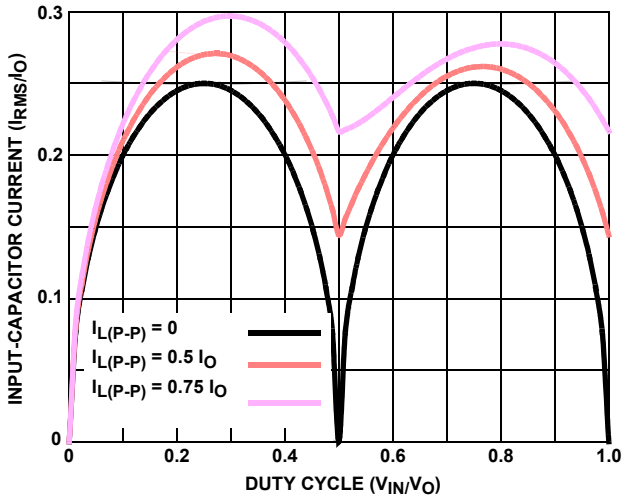


FIGURE 28. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 2-PHASE CONVERTER

There are two sets of critical components in a DC/DC converter using a ISL6324A controller. The power components are the most critical because they switch large amounts of energy. Next are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first, which include the MOSFETs, input and output capacitors, and the inductors. It is important to have a symmetrical layout for each power train, preferably with the controller located equidistant from each. Symmetrical layout allows heat to be dissipated equally across all power trains. Equidistant placement of the controller to the CORE and NB power trains it controls through the integrated drivers helps keep the gate drive traces equally short, resulting in equal trace impedances and similar drive capability of all sets of MOSFETs.

When placing the MOSFETs try to keep the source of the upper FETs and the drain of the lower FETs as close as thermally possible. Input high-frequency capacitors, C_{HF}, should be placed close to the drain of the upper FETs and the source of the lower FETs. Input bulk capacitors, CBULK, case size typically limits following the same rule as the high-frequency input capacitors. Place the input bulk capacitors as close to the drain of the upper FETs as possible and minimize the distance to the source of the lower FETs.

Locate the output inductors and output capacitors between the MOSFETs and the load. The high-frequency output decoupling capacitors (ceramic) should be placed as close as practicable to the decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND next or on the capacitor solder pad.

The critical small components include the bypass capacitors (C_{FILTER}) for VCC and PVCC, and many of the components surrounding the controller including the feedback network and current sense components. Locate the VCC/PVCC bypass capacitors as close to the ISL6324A as possible. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up.

A multi-layer printed circuit board is recommended. Figure 28 shows the connections of the critical components for the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually the one underneath the component side of the board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to output inductors short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring.

Routing UGATE, LGATE, and PHASE Traces

Great attention should be paid to routing the UGATE, LGATE, and PHASE traces since they drive the power train MOSFETs using short, high current pulses. It is important to size them as large and as short as possible to reduce their overall impedance and inductance. They should be sized to carry at least one ampere of current (0.02” to 0.05”). Going between layers with vias should also be avoided, but if so, use two vias for interconnection when possible.

Extra care should be given to the LGATE traces in particular since keeping their impedance and inductance low helps to significantly reduce the possibility of shoot-through. It is also important to route each channels UGATE and PHASE traces in as close proximity as possible to reduce their inductances.

Current Sense Component Placement and Trace Routing

One of the most critical aspects of the ISL6324A regulator layout is the placement of the inductor DCR current sense components and traces. The R-C current sense components must be placed as close to their respective ISEN+ and ISEN- pins on the ISL6324A as possible.

The sense traces that connect the R-C sense components to each side of the output inductors should be routed on the bottom of the board, away from the noisy switching components located on the top of the board. These traces should be routed side by side, and they should be very thin traces. It’s important to route these traces as far away from any other noisy traces or planes as possible. These traces should pick up as little noise as possible.

Thermal Management

For maximum thermal performance in high current, high switching frequency applications, connecting the thermal GND pad of the ISL6324A to the ground plane with multiple vias is recommended. This heat spreading allows the part to achieve its full thermal potential. It is also recommended that the controller be placed in a direct path of airflow if possible to help thermally manage the part.

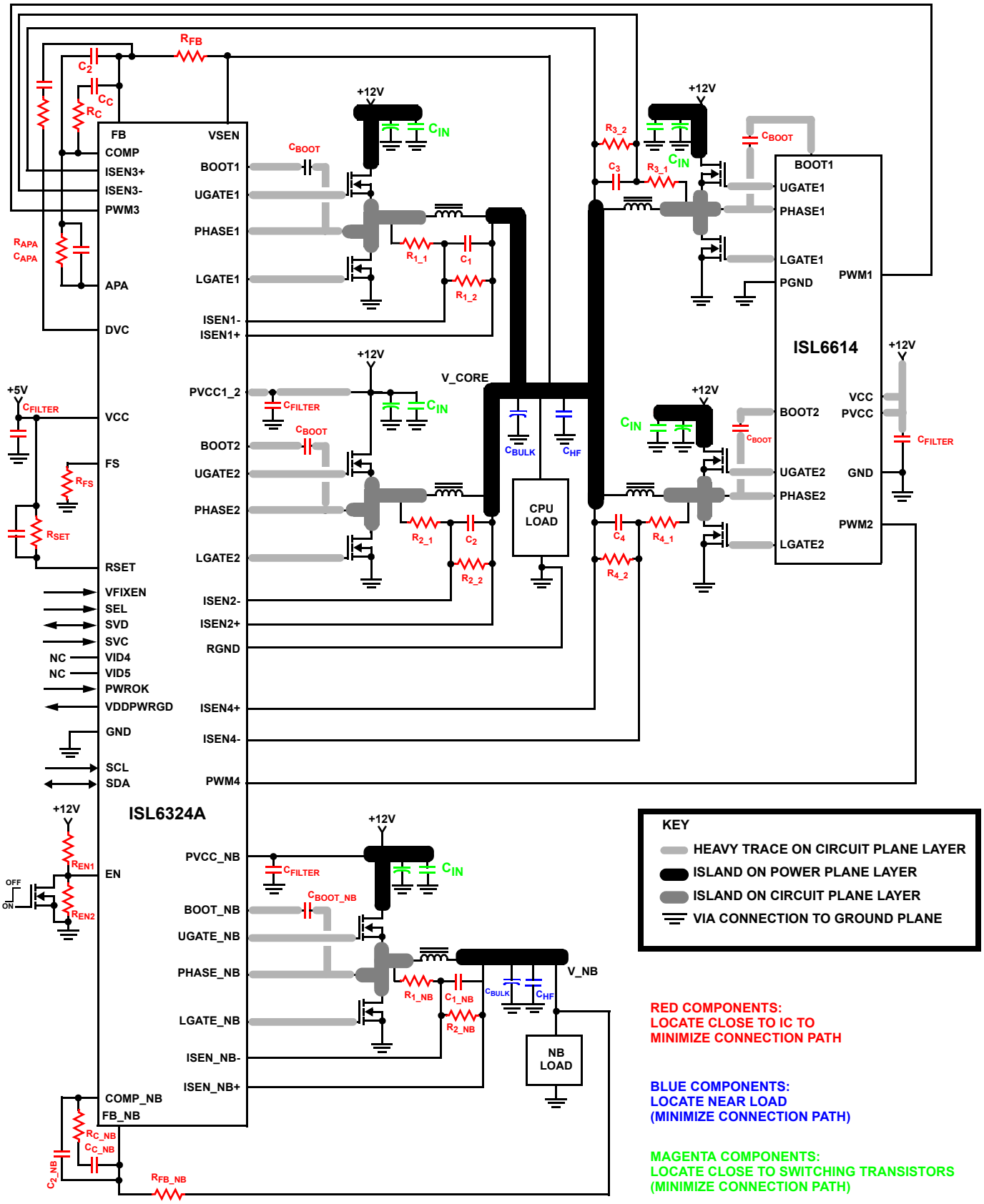
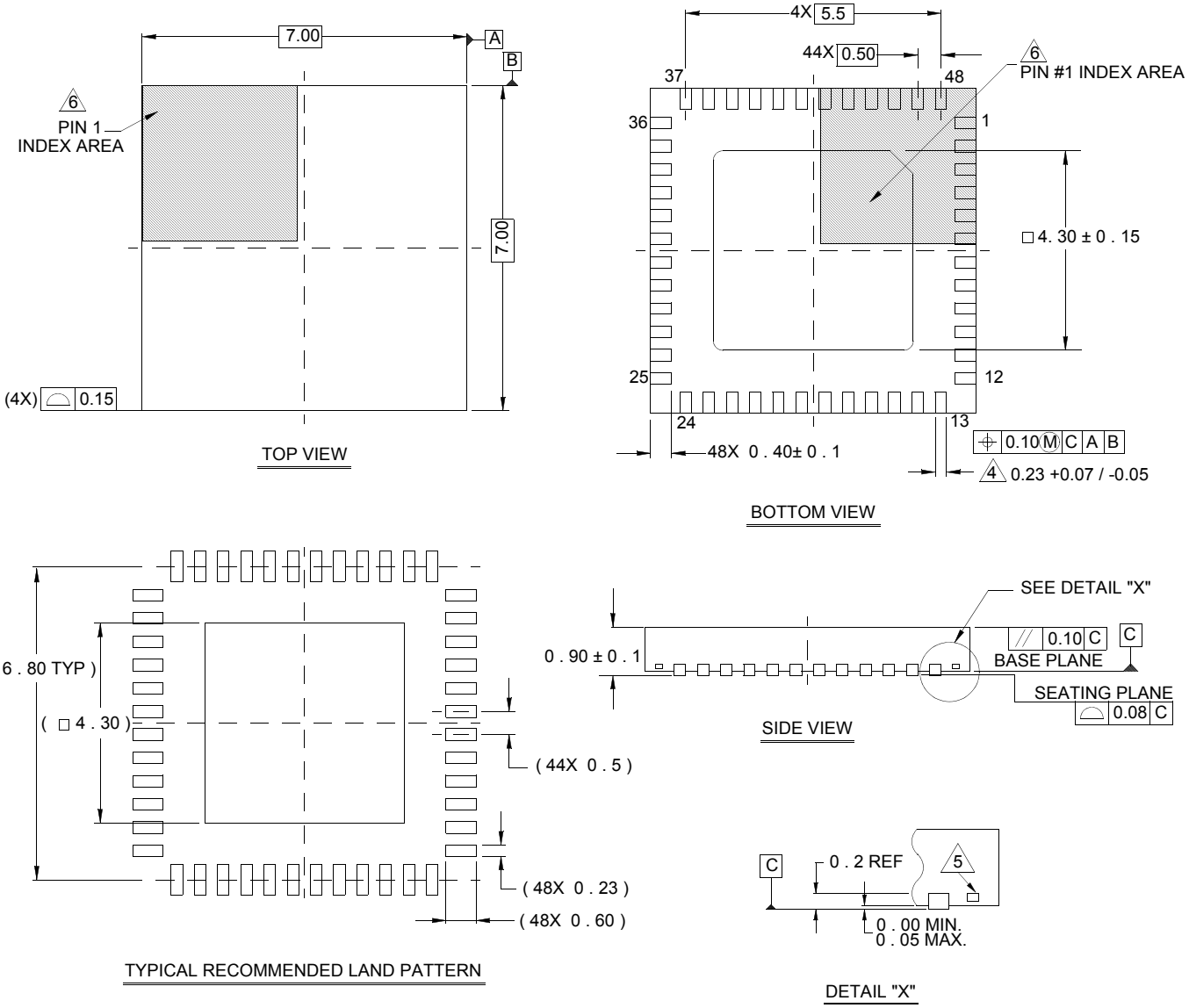


FIGURE 29. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Package Outline Drawing

L48.7x7

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 10/06



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.