ISL8700A, ISL8701A, ISL8702A, ISL8703A, ISL8704A, ISL8705A

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The ISL8700A, ISL8701A, ISL8702A, ISL8703A, ISL8704A, ISL8705A family of ICs provide four delay adjustable sequenced outputs while monitoring an input voltage all with a minimum of external components.

High performance DSP, FPGA, µP and various subsystems require input power sequencing for proper functionality at initial power-up and the ISL870XA provides this function while monitoring the distributed voltage for over and undervoltage compliance.

These ICs operate over the +3.3V to +24V nominal voltage range. All have a user adjustable time from UV and OV voltage compliance to sequencing start via an external capacitor when in auto start mode and adjustable time delay to subsequent ENABLE output signal via external resistors.

Additionally, the ISL8702A, ISL8703A, ISL8704A and ISL8705A provide I/O for sequencing on and off operation (SEQ_EN) and for voltage window compliance reporting (FAULT) over the +3.3V to +24V nominal voltage range.

Easily daisy chained for more than 4 sequenced signals.

Altogether, the ISL870XA provides these adjustable features with a minimum of external BOM. See Figure 1 for typical implementation.

Ordering Information

PART NUMBER (Note 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8700AIBZ*	ISL 8700AIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL8701AIBZ*	ISL 8701AIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL8702AIBZ*	ISL 8702AIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL8703AIBZ*	ISL 8703AIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL8704AIBZ*	ISL 8704AIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL8705AIBZ*	ISL 8705AIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL870XAEVAL1	Evaluation Platform			

*Add “-T” suffix for tape and reel.

NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

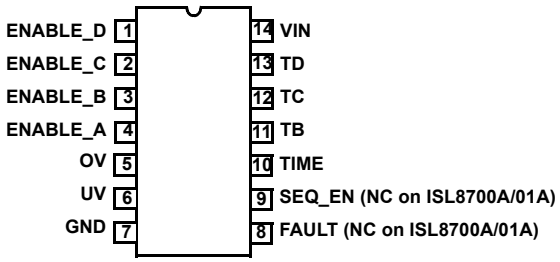
- Adjustable Delay to Subsequent Enable Signal
- Adjustable Delay to Sequence Auto Start
- Adjustable Distributed Voltage Monitoring
- Under and Overvoltage Adjustable Delay to Auto Start Sequence
- I/O Options
  ENABLE (ISL8700A, ISL8702A, ISL8704A) and
  ENABLE# (ISL8701A, ISL8703A, ISL8705A)
  SEQ_EN (ISL8702A, ISL8703A) and
  SEQ_EN# (ISL8704A, ISL8705A)
- Voltage Compliance Fault Output
- Pb-Free (RoHS Compliant)

Applications

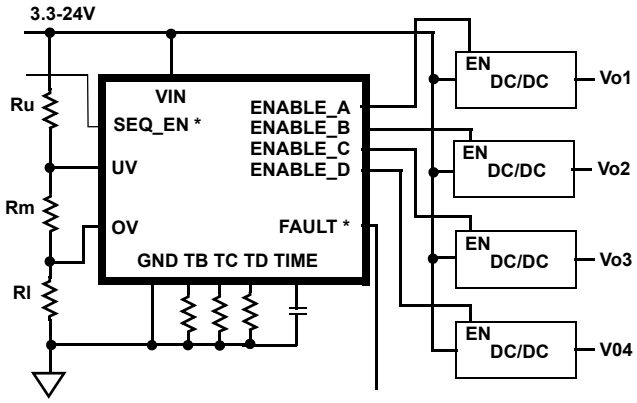
- Power Supply Sequencing
- System Timing Function

Pinout

ISL870XA
(14 LD SOIC)
TOP VIEW



ISL8701A, ISL8703A, ISL8705A PINS 1-4 ARE ENABLE# FUNCTION
ISL8704A, ISL8705A PIN 9 IS SEQ_EN# FUNCTION



*** SEQ_EN and FAULT are not available on ISL8700A and ISL8701A**

FIGURE 1. ISL870XA IMPLEMENTATION

Absolute Maximum Ratings

V_{IN}, ENABLE(#), FAULT . . . . . 27V, to -0.3V
TIME, TB, TC, TD, UV, OV . . . . . +6V, to -0.3V
SEQ_EN(#) . . . . . V_{IN}+0.3V, to -0.3V
ENABLE, ENABLE # Output Current 10mA

Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Supply Voltage Range (Nominal) . . . . . 3.3V to 24V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
14 Ld SOIC	110

Maximum Junction Temperature (Plastic Package) . . . . . +125°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

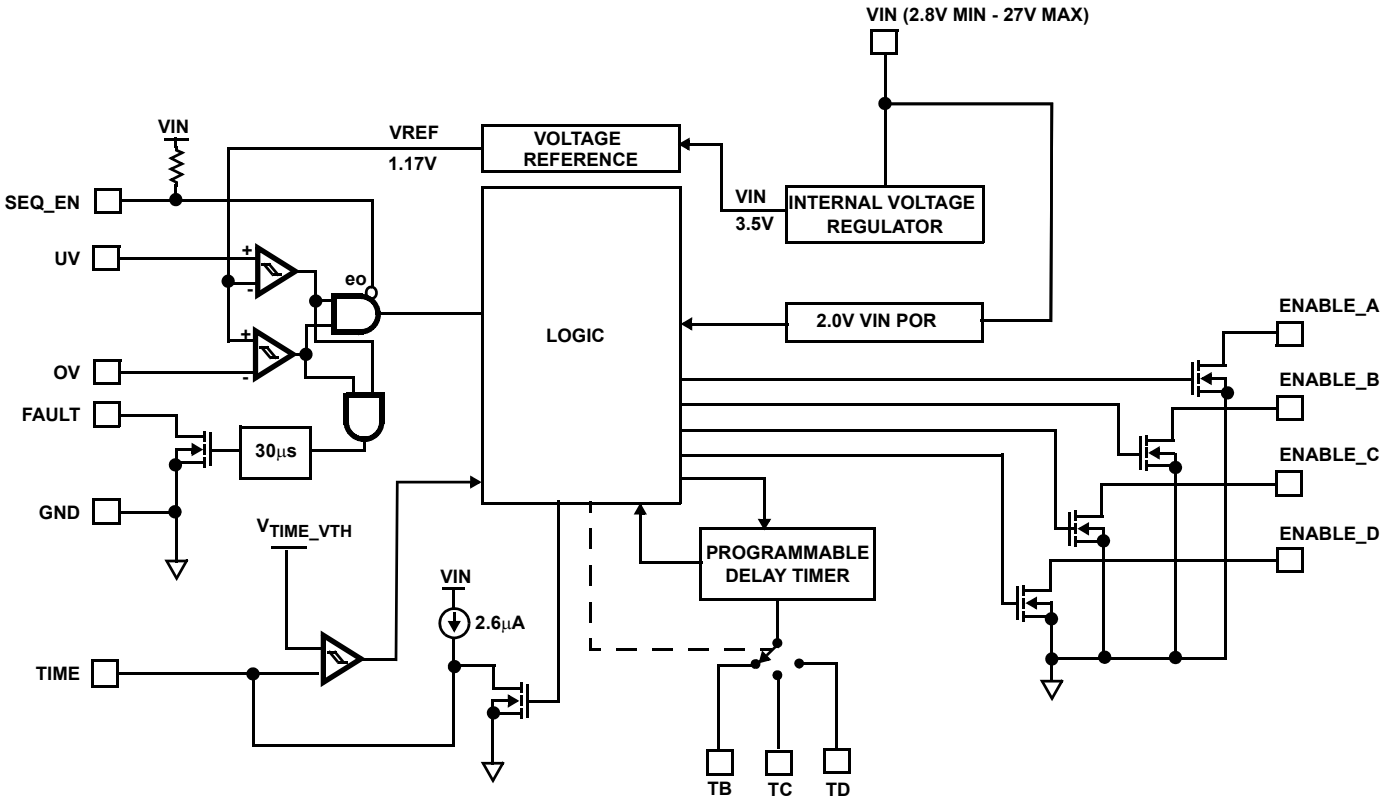
Nominal V_{IN} = 3.3V to +24V, T_A = T_J = -40°C to+85°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UV AND OV INPUTS						
UV/OV Rising Threshold	V_{UVRvth}		1.16	1.21	1.28	V
UV/OV Falling Threshold	V_{UVFvth}		1.06	1.10	1.18	V
UV/OV Hysteresis	V_{UVhys}	V_{UVRvth} - V_{UVFvth}	-	104	-	mV
UV/OV Input Current	I_{UV}		-	10	-	nA
TIME, ENABLE/ENABLE# OUTPUTS						
TIME Pin Charging Current	I_{TIME}		-	2.6	-	µA
TIME Pin Threshold	V_{TIME_VTH}		1.9	2.0	2.25	V
Time from V_{IN} Valid to ENABLE_A	$t_{VINSEQpd}$	SEQ_EN = high, C_{TIME} = open	-	30	-	µs
	$t_{VINSEQpd\_10}$	SEQ_EN = high, C_{TIME} = 10nF	-	7.7	-	ms
	$t_{VINSEQpd500}$	SEQ_EN = high, C_{TIME} = 500nF	-	435	-	ms
Time from V_{IN} Invalid to Shutdown	$t_{shutdown}$	UV or OV to simultaneous shutdown	-	-	1	µs
ENABLE Output Resistance	R_{EN}	I_{ENABLE} = 1mA	-	100	-	Ω
ENABLE Output Low	Vol	I_{ENABLE} = 1mA	-	0.1	-	V
ENABLE Pull-down Current	I_{pulld}	ENABLE = 1V	10	15	-	mA
Delay to Subsequent ENABLE Turn-on/off	t_{del_120}	R_{TX} = 120kΩ	155	195	240	ms
	t_{del_3}	R_{TX} = 3kΩ	3.5	4.7	6	ms
	t_{del_0}	R_{TX} = 0Ω	-	0.5	-	ms
SEQUENCE ENABLE AND FAULT I/O						
V_{IN} Valid to FAULT Low	t_{FLTL}		15	30	50	µs
V_{IN} Invalid to FAULT High	t_{FLTH}		-	0.5	-	µs
FAULT Pull-down Current		FAULT = 1V	10	15	-	mA
SEQ_EN Pull-up Voltage	V_{SEQ}	SEQ_EN open	-	2.4	-	V
SEQ_EN Low Threshold Voltage	Vil_{SEQ_EN}		-	-	0.3	V
SEQ_EN High Threshold Voltage	Vih_{SEQ_EN}		1.2	-	-	V
Delay to ENABLE_A Deasserted	$t_{SEQ\_EN\_ENA}$	SEQ_EN low to ENABLE_A low	-	0.2	1	µs
BIAS						
IC Supply Current	$I_{VIN\_3.3V}$	V_{IN} = 3.3V	-	191	-	µA
	I_{VIN_12V}	V_{IN} = 12V	-	246	400	µA
	I_{VIN_24V}	V_{IN} = 24V	-	286	-	µA
V_{IN} Power On Reset	V_{IN_POR}	V_{IN} low to high	-	2.3	2.8	V

Pin Descriptions

PINS						PIN NAME	FUNCTION DESCRIPTION
8700A	8701A	8702A	8703A	8704A	8705A		
NA	1	NA	1	NA	1	ENABLE#_D	Active low open drain sequenced output. Sequenced on after ENABLE#_C and first output to sequence off for the ISL8701A, ISL8703A, ISL8705A. Tracks V_{IN} upon bias.
1	NA	1	NA	1	NA	ENABLE_D	Active high open drain sequenced output. Sequenced on after ENABLE_C and first output to sequence off for the ISL8700A, ISL8702A, ISL8704A. Pulls low with V_{IN} < 1V.
NA	2	NA	2	NA	2	ENABLE#_C	Active low open drain sequenced output. Sequenced on after ENABLE#_B and sequenced off after ENABLE#_D for the ISL8701A, ISL8703A, ISL8705A. Tracks V_{IN} upon bias.
2	NA	2	NA	2	NA	ENABLE_C	Active high open drain sequenced output. Sequenced on after ENABLE_B and sequenced off after ENABLE_D for the ISL8700A, ISL8702A, ISL8704A. Pulls low with V_{IN} < 1V.
NA	3	NA	3	NA	3	ENABLE#_B	Active low open drain sequenced output. Sequenced on after ENABLE#_A and sequenced off after ENABLE#_C for the ISL8701A, ISL8703A, ISL8705A. Tracks V_{IN} upon bias.
3	NA	3	NA	3	NA	ENABLE_B	Active high open drain sequenced output. Sequenced on after ENABLE_A and sequenced off after ENABLE_C for the ISL8700A, ISL8702A, ISL8704A. Pulls low with V_{IN} < 1V.
NA	4	NA	4	NA	4	ENABLE#_A	Active low open drain sequenced output. Sequenced on after CTIME period and sequenced off after ENABLE#_B for the ISL8701A, ISL8703A, ISL8705A. Tracks V_{IN} upon bias.
4	NA	4	NA	4	NA	ENABLE_A	Active high open drain sequenced output. Sequenced on after CTIME period and sequenced off after ENABLE_B for the ISL8700A, ISL8702A, ISL8704A. Pulls low with V_{IN} < 1V.
5	5	5	5	5	5	OV	The voltage on this pin must be under its 1.22V Vth or the four ENABLE outputs will be immediately pulled down. Conversely the 4 ENABLE# outputs will be released to be pulled high via external pull-ups.
6	6	6	6	6	6	UV	The voltage on this pin must be over its 1.22V Vth or the four ENABLE outputs will be immediately pulled down. Conversely the 4 ENABLE# outputs will be released to be pulled high via external pull-ups.
7	7	7	7	7	7	GND	IC ground.
NA	NA	8	8	8	8	FAULT	The V_{IN} voltage when not within the desired UV to OV window will cause FAULT to be released to be pulled high to a voltage equal to or less than V_{IN} via an external resistor.
NA	NA	9	9	NA	NA	SEQ_EN	This pin provides a sequence on signal input with a high input. Internally pulled high to ~2.4V.
NA	NA	NA	NA	9	9	SEQ_EN#	This pin provides a sequence on signal input with a low input. Internally pulled high to ~2.4V.
10	10	10	10	10	10	TIME	This pin provides a 2.6µA current output so that an adjustable V_{IN} valid to sequencing on and off start delay period is created with a capacitor to ground.
11	11	11	11	11	11	TB	A resistor connected from this pin to ground determines the time delay from ENABLE_A being active to ENABLE _B being active on turn-on and also going inactive on turn-off via the SEQ_IN input.
12	12	12	12	12	12	TC	A resistor connected from this pin to ground determines the time delay from ENABLE_B being active to ENABLE _C being active on turn-on and also going inactive on turn-off via the SEQ_IN input.
13	13	13	13	13	13	TD	A resistor connected from this pin to ground determines the time delay from ENABLE_C being active to ENABLE _D being active on turn-on and also going inactive on turn-off via the SEQ_IN input.
14	14	14	14	14	14	V_{IN}	IC Bias Pin Nominally 3.3V to 24V This pin requires a 1µF decoupling capacitor close to IC pin.

Functional Block Diagram



Functional Description

The ISL870XA family of ICs provides four delay adjustable sequenced outputs while monitoring a single distributed voltage in the nominal range of 3.3V to 24V for both under and overvoltage. Only when the voltage is in compliance will the ISL870XA initiate the pre-programmed A-B-C-D sequence of the ENABLE (ISL8700A, ISL8702A, ISL8704A) or ENABLE# (ISL8701A, ISL8703A, ISL8705A) outputs. Although this IC has a bias range of 3.3V to 24V it can monitor any voltage >1.22V via the external divider if a suitable bias voltage is otherwise provided.

During initial bias voltage (V_{IN}) application the ISL8700A, ISL8702A, ISL8704A ENABLE outputs are held low once V_{IN} = 1V whereas the ISL8701A, ISL8703A, ISL8705A ENABLE# outputs follow the rising V_{IN}. Once V_{IN} > the V bias power on reset threshold (POR) of 2.8V, V_{IN} is constantly monitored for compliance via the input voltage resistor divider and the voltages on the UV and OV pins and reported by the FAULT output. Internally, voltage regulators generate 3.5V and 1.17V ±5% voltage rails for internal usage once V_{IN} > POR. Once UV > 1.22V and with the SEQ_EN pin high or open, (SEQ_EN# must be pulled low on ISL8704A, ISL8705A) the auto sequence of the four ENABLE (ENABLE#) outputs begins as the TIME pin charges its external capacitor with a 2.6µA current source. The voltage on TIME is compared to the internal reference (V_{TIME_VTH}) comparator input and when greater than V_{TIME_VTH} the ISL8700A, ISL8702A, ISL8704A ENABLE_A is released to go high via an external pull-up resistor or a pull-up in a DC/DC convertor enable input, for example. Conversely, ENABLE#_A output will be pulled low at this time on an ISL8701A, ISL8703A, ISL8705A. The time delay generated by the external capacitor is to assure continued voltage compliance within the programmed limits, as during this time any OV or UV condition will halt the start-up process. TIME cap is discharged once V_{TIME_VTH} is met.

Once ENABLE_A is active (either released high on the ISL8700A, ISL8702A, ISL8704A or pulled low, ISL8701A, ISL8703A, ISL8705A) a counter is started and using the resistor on TB as a timing component a delay is generated before ENABLE_B is activated. At this time, the counter is restarted using the resistor on TC as its timing component for a separate timed delay until ENABLE_C is activated. This process is repeated for the resistor on TD to complete the A-B-C-D sequencing order of the ENABLE or ENABLE# outputs. At any time during sequencing if an OV or UV event is registered, all four ENABLE outputs will immediately return to their reset state; low for ISL8700A, ISL8702A, ISL8704A and high for ISL8701A, ISL8703A, ISL8705A. C_{TIME} is immediately discharged after initial ramp up thus waiting for subsequent voltage compliance to restart. Once sequencing is complete, any subsequently registered UV or OV event will trigger an immediate and simultaneous reset of all ENABLE or ENABLE# outputs.

On the ISL8702A, ISL8703A, ISL8704A and ISL8705A, enabling of on or off sequencing can also be signaled via the SEQ_EN or SEQ_EN# input pin once voltage compliance is met. Initially, the SEQ_EN pin should be held low and released when sequence start is desired. The SEQ# is internally pulled high and sequencing is enabled when it is pulled low. The on sequence of the ENABLE outputs is as previously described. The off sequence feature is only available on the variants having the SEQ_EN or the SEQ_EN# inputs, these being the ISL8702A, ISL8703A, ISL8704A, ISL8705A. The sequence is D off, then C off, then B off and finally A off. Once SEQ_EN (SEQ_EN#) is signaled low (high), the TIME cap is charged to 2V once again. Once this Vth is reached, ENABLE_D transitions to its reset state and CTIM is discharged. A delay and subsequent sequence off is then determined by TD resistor to ENABLE_C. Likewise, a delay to ENABLE_B and then ENABLE_A turn-off is determined by TC and TB resistor values respectively.

With the ISL8700A, ISL8701A a quasi down sequencing of the ENABLE outputs can be achieved by loading the ENABLE pins with various value capacitors to ground. When a simultaneous output latch off is invoked, the caps will set the falling ramp of the various ENABLE outputs thus adjusting the time to Vth for various DC/DC convertors or other circuitry.

Regardless of IC variant, the FAULT signal is always valid at operational voltages and can be used as justification for SEQ_EN release or even controlled with an RC timer for sequence on.

Programming the Under and Overvoltage Limits

When choosing resistors for the divider remember to keep the current through the string bounded by power loss at the top end and noise immunity at the bottom end. For most applications, total divider resistance in the 10kΩ to1000kΩ range is advisable with high precision resistors being used to reduce monitoring error. Although for the ISL870XA, two dividers of two resistors each can be employed to separately monitor the OV and UV levels for the V_{IN} voltage. We will discuss using a single three resistor string for monitoring the V_{IN} voltage, referencing Figure 1. In the three resistor divider string with Ru (upper), Rm (middle) and Rl (lower), the ratios of each in combination to the other two is balanced to achieve the desired UV and OV trip levels. Although this IC has a bias range of 3.3V to 24V, it can monitor any voltage >1.22V.

The ratio of the desired overvoltage trip point to the internal reference is equal to the ratio of the two upper resistors to the lowest (gnd connected) resistor.

The ratio of the desired undervoltage trip point to the internal reference voltage is equal to the ratio of the uppermost (voltage connected) resistor to the lower two resistors.

These assumptions are true for both rising (turn-on) or falling (shutdown) voltages.

The following is a practical example worked out. For detailed equations on how to perform this operation for a given supply requirement please see the next section.

1. Determine if turn-on or shutdown limits are preferred. In this example, we will determine the resistor values based on the shutdown limits.
2. Establish lower and upper trip level: 12V ±10% or 13.2V (OV) and 10.8V (UV)
3. Establish total resistor string value: 100kΩ, Ir = divider current, 1.1V is falling 1.2V is rising threshold.
4. (Rm+Rl) x Ir = 1.1V at UV and Rl x Ir = 1.2V at OV
5. Rm+Rl = 1.1V/Ir at UV = Rm+Rl = 1.1V/(10.8V/100kΩ) = 10.185kΩ
6. Rl = 1.2V/Ir at OV = Rl = 1.2V/(13.2V/100kΩ) = 9.09kΩ
7. Rm = 10.185kΩ - 9.09kΩ = 1.095kΩ
8. Ru = 100kΩ - 10.185kΩ = 89.815kΩ
9. Choose standard value resistors that most closely approximate these ideal values. Choosing a different total divider resistance value may yield a more ideal ratio with available resistor's values.

In our example, with the closest standard values of Ru = 90.9kΩ, Rm = 1.13kΩ and Rl = 9.31kΩ, the nominal UV falling and OV rising will be at 10.9V and 13.3V respectively.

Programming the ENABLE Output Delays

The delay timing between the four sequenced ENABLE outputs are programmed with four external passive components. The delay from a valid V_{IN} (ISL8700A and ISL8701A) to ENABLE_A and SEQ_EN being valid (ISL8702A, ISL8703A, ISL8704A, ISL8705A) to ENABLE_A is determined by the value of the capacitor on the TIME pin to GND. The external TIME pin capacitor is charged with a 2.6µA current source. Once the voltage on TIME is charged up to the internal reference voltage, (V_{TIME_VTH}) the ENABLE_A output is released out of its reset state. The capacitor value for a desired delay (±10%) to ENABLE_A once V_{IN} and SEQ_EN where applicable has been satisfied is determined by:

$C_{TIME} = t_{VINSEQpd}/770k\Omega$

Once ENABLE_A reaches V_{TIME_VTH}, the TIME pin is pulled low in preparation for a sequenced off signal via SEQ_EN. At this time, the sequencing of the subsequent outputs is started. ENABLE_B is released out of reset after a programmable time, then ENABLE_C, then ENABLE _D, all with their own programmed delay times.

The subsequent delay times are programmed with a single external resistor for each ENABLE output providing maximum flexibility to the designer through the choice of the resistor value connected from TB, TC and TD pins to GND. The resistor values determine the charge and discharge rate of an internal capacitor comprising an RC time constant for an oscillator whose output is fed into a counter generating the timing delay to ENABLE output sequencing.

The R_{TX} value for a given delay time is defined as:

$R_{TX} = t_{del}/1667nF$

An Advanced Tutorial on Setting UV and OV Levels

This section discusses in additional detail the nuances of setting the UV and OV levels, providing more insight into the ISL870XA than the earlier text.

The following equation set can alternatively be used to work out ideal values for a 3 resistor divider string of Ru, Rm and Rl. These equations assume that V_{REF} is the center point between V_{UVRvth} and V_{UVFvth} (i.e. (V_{UVRvth} + V_{UVFvth})/2 = 1.17V), Iload is the load current in the resistor string (i.e. V_{IN} /(Ru + Rm + Rl)), V_{IN} is the nominal input voltage and Vtol is the acceptable voltage tolerance, such that the UV and OV thresholds are centered at V_{IN} ± Vtol. The actual acceptable voltage window will also be affected by the hysteresis at the UV and OV pins. This hysteresis is amplified by the resistor string such that the hysteresis at the top of the string is:

$Vhys = V_{UVhys} \times V_{OUT}/V_{REF}$

This means that the V_{IN} ± Vtol thresholds will exhibit hysteresis resulting in thresholds of V_{IN} + Vtol ± Vhys/2 and V_{IN} - Vtol ± Vhys/2.

There is a window between the V_{IN} rising UV threshold and the V_{IN} falling OV threshold where the input level is guaranteed not to be detected as a fault. This window exists between the limits V_{IN} ± (Vtol - Vhys/2). There is an extension of this window in each direction up to V_{IN} ± (Vtol + Vhys/2), where the voltage may or may not be detected as a fault, depending on the direction from which it is approached. These two equations may be used to determine the required value of Vtol for a given system. For example, if V_{IN} is 12V, Vhys = (0.1 x 12)/1.17 = 1.03V. If V_{IN} must remain within 12V ± 1.5V, Vtol = 1.5 - 1.03/2 = 0.99V.

This will give a window of 12 ±0.48V where the system is guaranteed not to be in fault and a limit of 12 ±1.5V beyond which the system is guaranteed to be in fault.

It is wise to check both these voltages, for if the latter is made to tight, the former will cease to exist. This point comes when Vtol < Vhys/2 and results from the fact that the acceptable window for the OV pin no longer aligns with the acceptable window for the UV pin. In this case, the application will have to be changed such that UV and OV are provided separate resistor strings. In this case, the UV and OV thresholds can be individually controlled by adjusting the relevant divider.

The previous example will give voltage thresholds of:

with V_{IN} rising
UVr = V_{IN} - Vtol + Vhys/2 = 11.5V and
OVr = V_{IN} + Vtol + Vhys/2 = 13.5V

with V_{IN} falling
Ovf = V_{IN} + Vtol - Vhys/2 = 12.5V and
UVf = V_{IN} - Vtol - Vhys/2 = 10.5V.

So with a single three resistor string, the resistor values can be calculated as:

Rl = (V_{REF}/Iload) (1 - Vtol/V_{IN})
Rm = 2(V_{REF} x Vtol)/(V_{IN} x Iload)
Ru = 1/Iload x (V_{IN} - V_{REF} (1+Vtol/V_{IN}))

For the above example, with Vtol = 0.99V, assuming a 100µA Iload at V_{IN} = 12V:

Rl = 10.7kΩ
Rm = 1.9kΩ
Ru = 107.3kΩ

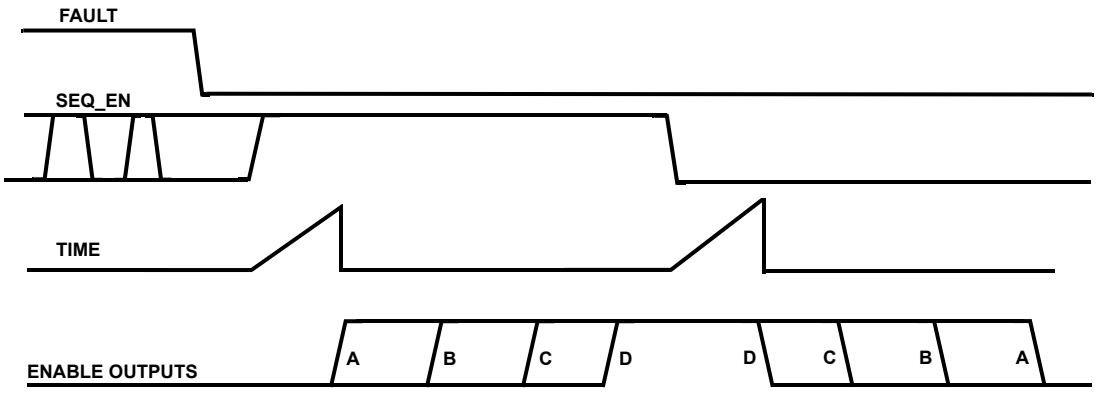


FIGURE 2. ISL8702A OPERATIONAL DIAGRAM

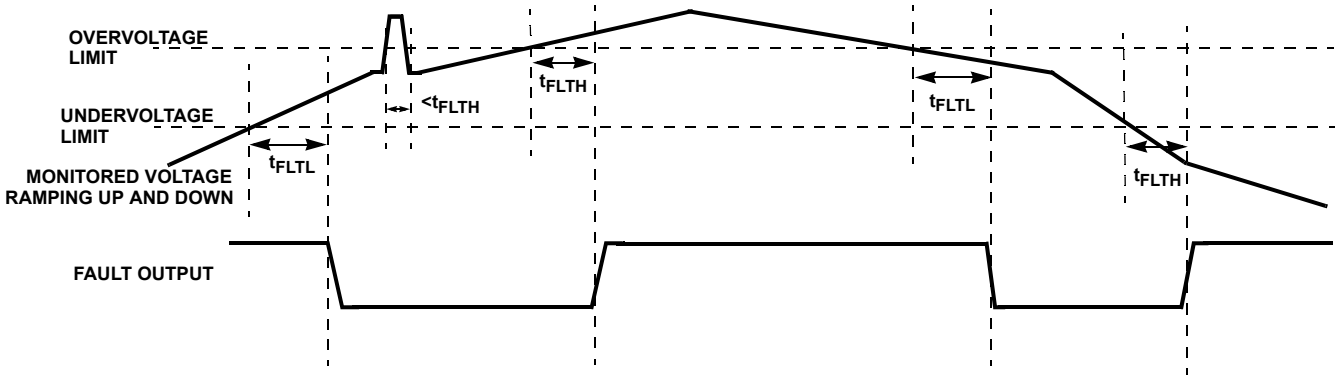


FIGURE 3. ISL8702A, ISL8703A, ISL8704A, ISL8705A FAULT OPERATIONAL DIAGRAM

Typical Performance Curves

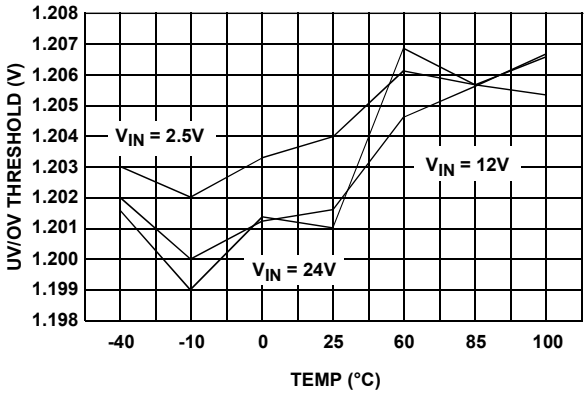


FIGURE 4. UV/OV RISING THRESHOLD

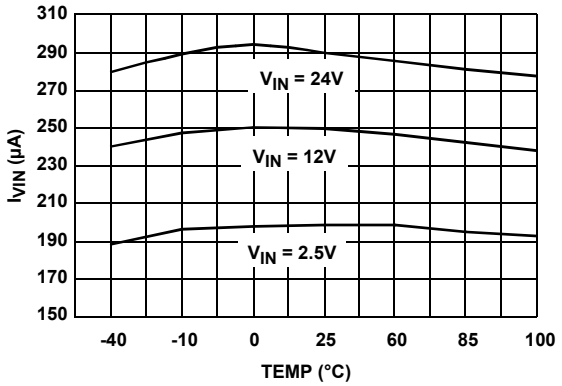


FIGURE 5. V_{IN} CURRENT

Applications Usage

Using the ISL870XAEVAL1 Platform

The ISL870XAEVAL1 platform is the primary evaluation board for this family of sequencers. See Figure 16 for photograph and schematic.The evaluation board is shipped with an **ISL8702A** mounted in the left position and with the other device variants loose packed. In the following discussion, test points names are **bold** on initial occurrence for identification.

The **V_{IN}** test point is the chip bias and can be biased from 3.3V to 24V. The **VHI** test point is for the ENABLE and **FAULT** pull-up voltage which are limited to a maximum of 24V independent of V_{IN}. The UV/OV resistor divider is set so that a nominal 12V on the **VMONITOR** test point is compliant and with a rising OV set at 13.2V and a falling UV set at 10.7V. These three test points (V_{IN},VHI and VMONITOR) are brought out separately for maximum flexibility in evaluation.

VMONITOR ramping up and down through the UV and OV levels will result in the FAULT output signaling the out of bound conditions by being released to pull high to the VHI voltage as shown in Figures 6 and 7.

Once the voltage monitoring FAULT is resolved and where applicable, the **SEQ_EN**(#) is satisfied, sequencing of the ENABLE_X(#) outputs begins. When sequence enabled the **ENABLE_A**, **ENABLE_B**, **ENABLE_C** and lastly **ENABLE_D** are asserted in that order and when SEQ_EN is disabled the order is reversed. See Figures 8 and 9 demonstrating the sequenced enabling and disabling of the ENABLE outputs. The timing between ENABLE outputs is set by the resistor values on the TB, TC, TD pins as shown. Figure 10 illustrates the timing from either SEQ_EN and/or VMONITOR being valid to ENABLE_A being asserted with a 10nF TIME capacitor. Figure 11 shows that ENABLE_X outputs are pulled low even before V_{IN} = 1V. This is critical to ensure that a false enable is not signaled. Figure 12 illustrates the SEQ_EN# input disabling and enabling the ISL8705A ENABLE# outputs. Notice the reversal in order and delay timing from ENABLE_X# to ENABLE_X#. Figure 13 shows the time from SEQ_EN transition with the voltage ramping across the TIME capacitor to TIME Vth being met. This results in the immediate pull down of the TIME pin and simultaneous ENABLE_A enabling.

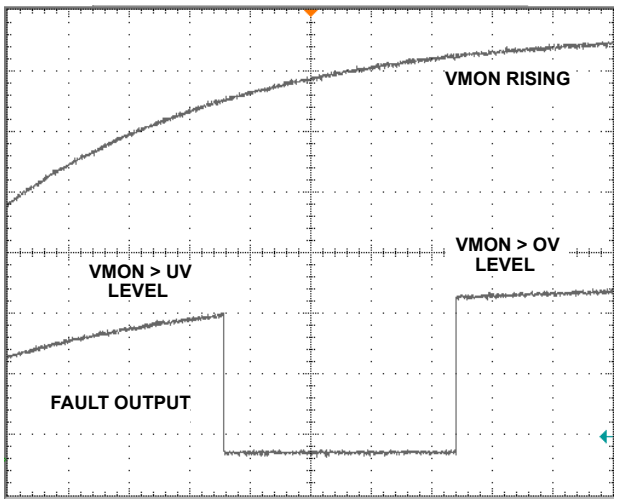


FIGURE 6. VMONITOR RISING TO FAULT

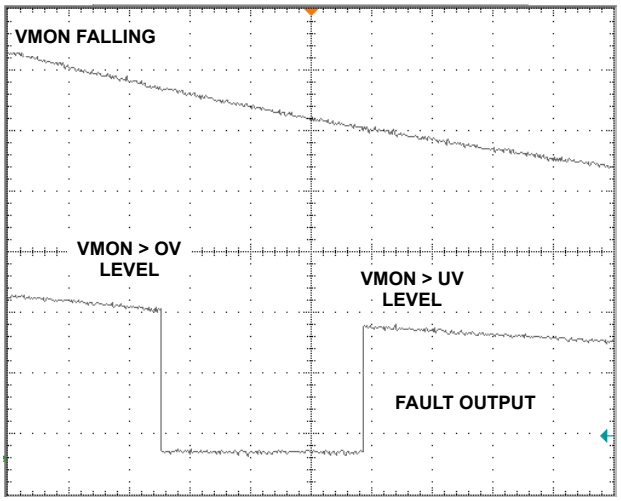


FIGURE 7. VMONITOR FALLING TO FAULT

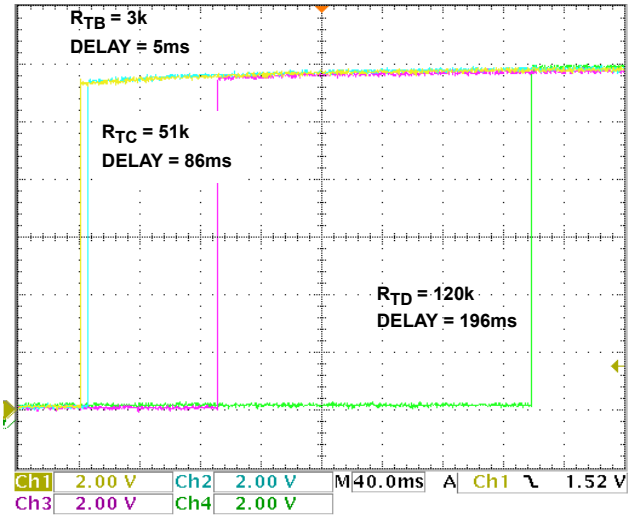


FIGURE 8. ENABLE_X TO ENABLE_X ENABLING

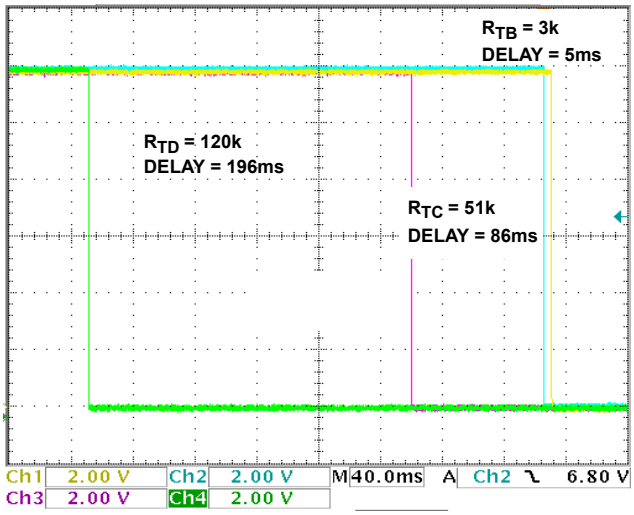


FIGURE 9. ENABLE_X TO ENABLE_X DISABLING

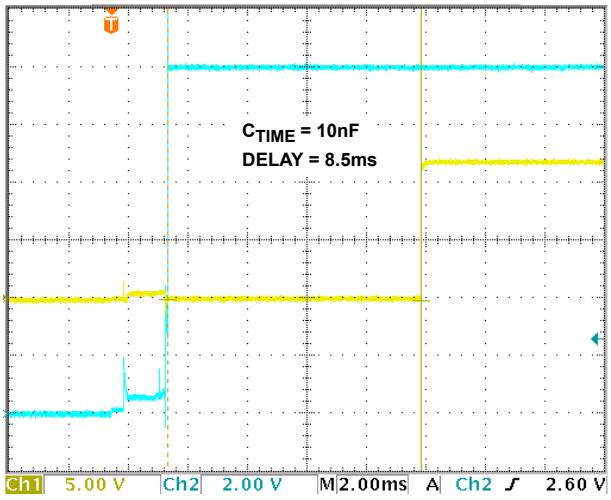


FIGURE 10. V_{IN}/SEQ_EN VALID TO ENABLE_A

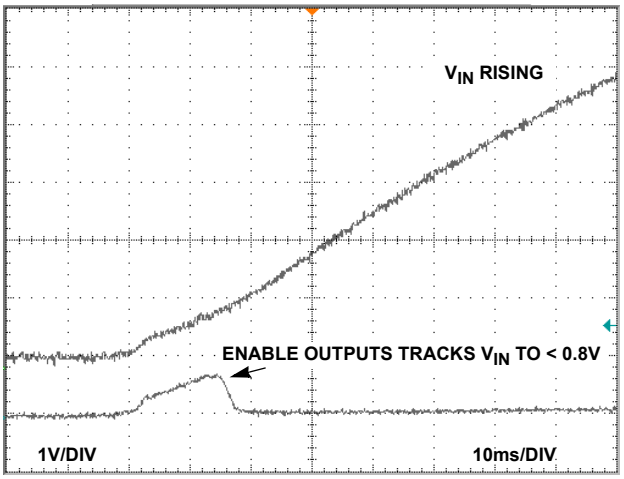


FIGURE 11. ENABLE AS V_{IN} RISES

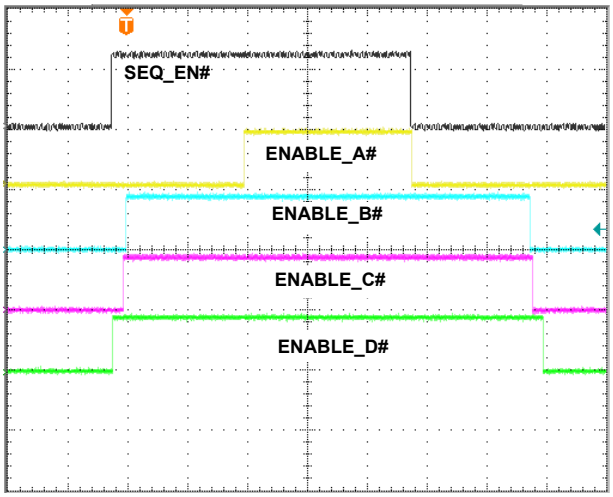


FIGURE 12. ISL8705A ENABLE_X# TO ENABLE_X#

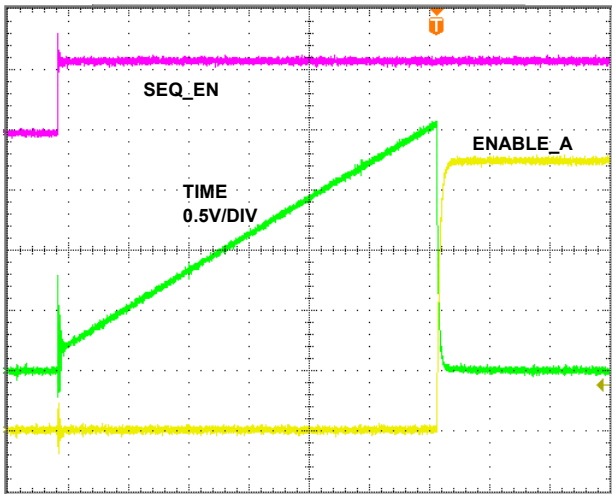


FIGURE 13. SEQ_EN TO ENABLE_A

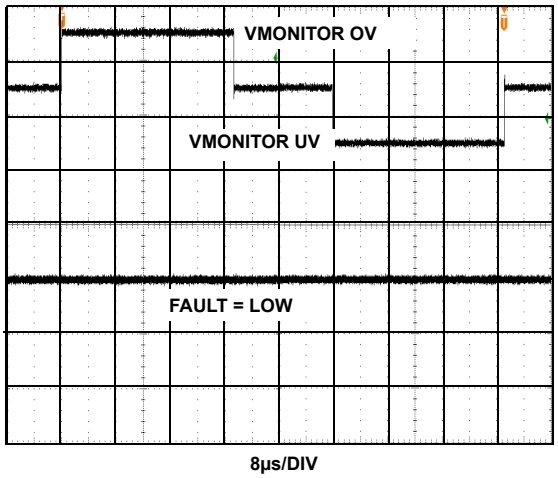


FIGURE 14. OV AND UV TRANSIENT IMMUNITY

Application Recommendations

Best practices V_{IN} decoupling is required, a 1µF capacitor is recommended.

Coupling from the ENABLE_X pins to the sensitive UV and OV pins can cause false OV/UV events to be detected. This is most relevant for ISL8700A, ISL8702A, ISL8704A parts due to the ENABLEA and OV pins being adjacent. This coupling can be reduced by adding a ground trace between UV and the ENABLE/FAULT signals, as shown in Figure 15. The PCB traces on OV and UV should be kept as small as practical and the ENABLE_X and FAULT traces should ideally not be routed under/over the OV/UV traces on different PCB layers unless there is a ground or power plane in between. Other methods that can be used to eliminate this issue are by reducing the value of the resistors in the network connected to UV and OV (R_2, R_3, R_5 in Figure 16) or by adding small decoupling capacitors to OV and UV (C_2 and C_7 in Figure 16). Both these methods act to reduce the AC impedance at the nodes, although the latter method acts to filter the signals which will also cause an increase in the time that a UV/OV fault takes to be detected.

When the ISL870XA is implemented on a hot swappable card that is plugged into an always powered passive back plane an RC filter is required on the V_{IN} pin to prevent a high dv/dt transient. With the already existing 1µF decoupling capacitor the addition of a small series R (>50Ω) to provide a time constant >50µs is all that is necessary.

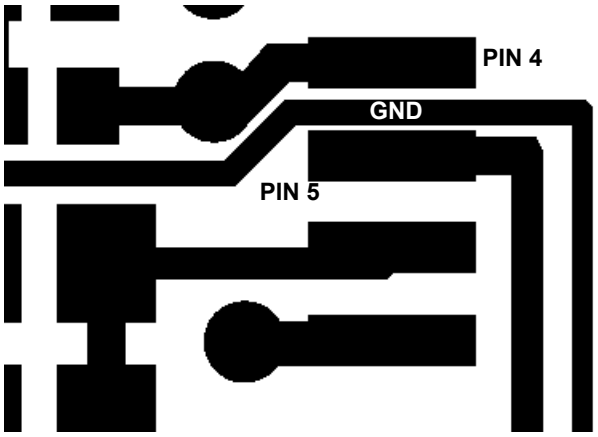
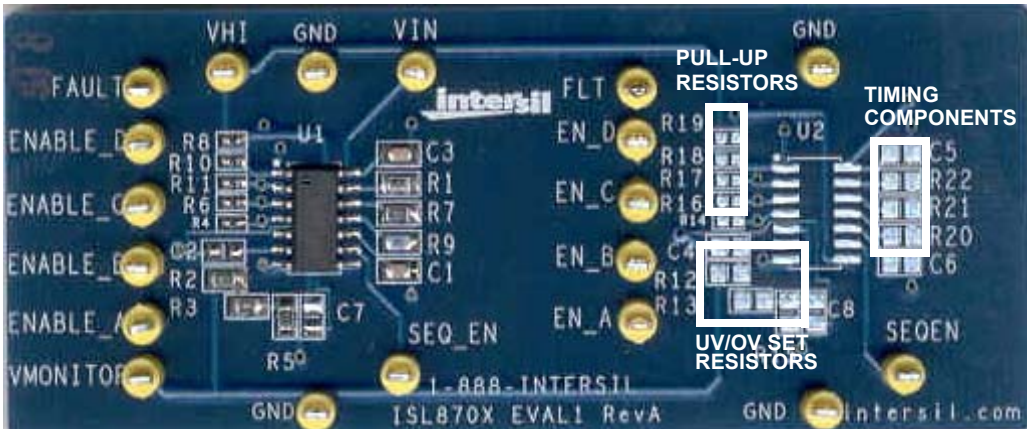


FIGURE 15. LAYOUT DETAIL OF GND BETWEEN PINS 4 AND 5



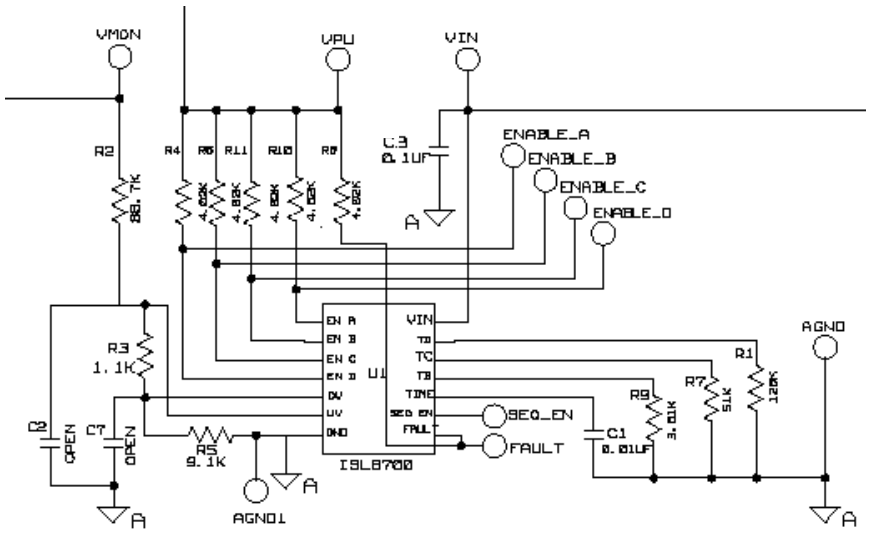


FIGURE 16. ISL870XAEVAL1 PHOTOGRAPH AND SCHEMATIC OF LEFT CHANNEL

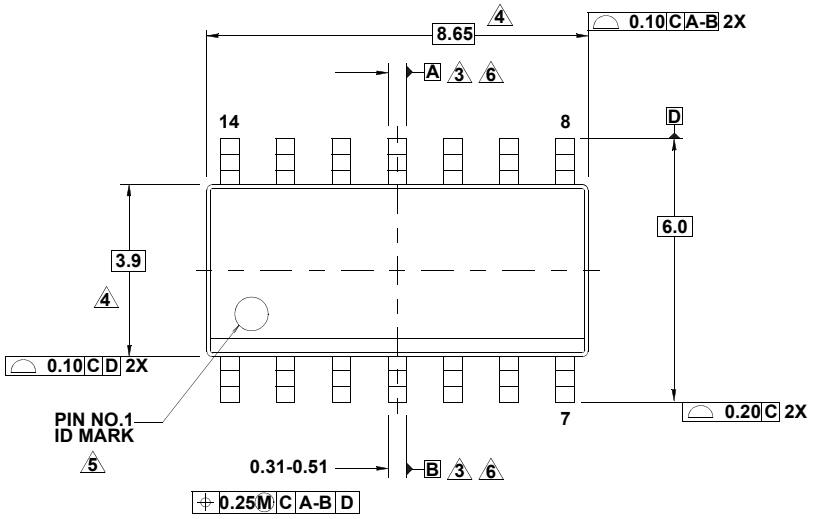
TABLE 1. ISL870XAEVAL1 LEFT CHANNEL COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
U1	**ISL8702A**, Quad Under/Overvoltage Sequencer	Intersil, **ISL8702A**, Quad Under/Overvoltage Sequencer
R3	UV Resistor for Divider String	1.1kΩ 1%, 0603
R2	VMONITOR Resistor for Divider String	88.7kΩ 1%, 0603
R5	OV Resistor for Divider String	9.1kΩ 1%, 0603
C1	C_{TIME} Sets Delay from Sequence Start to First ENABLE	0.01µF, 0603
R1	R_{TD} Sets Delay from Third to Fourth ENABLE	120kΩ 1%, 0603
R9	R_{TB} Sets Delay from First to Second ENABLE	3.01kΩ 1%, 0603
R7	R_{TC} Sets Delay from Second to Third ENABLE	51kΩ 1%, 0603
R4, R6, R8, R10, R11	ENABLE_X(#) and FAULT Pull-up Resistors	4kΩ 10%, 0402
C3	Decoupling Capacitor	1µF, 0603

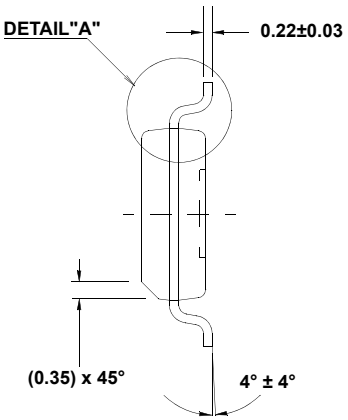
Package Outline Drawing

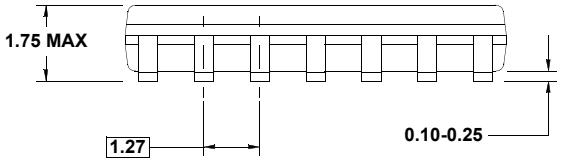
M14.15

14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 1, 10/09

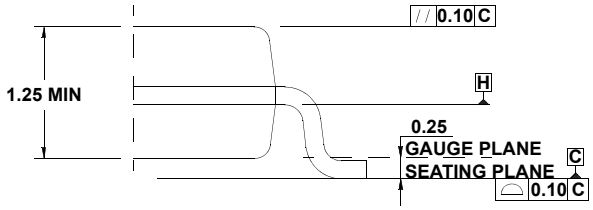


TOP VIEW

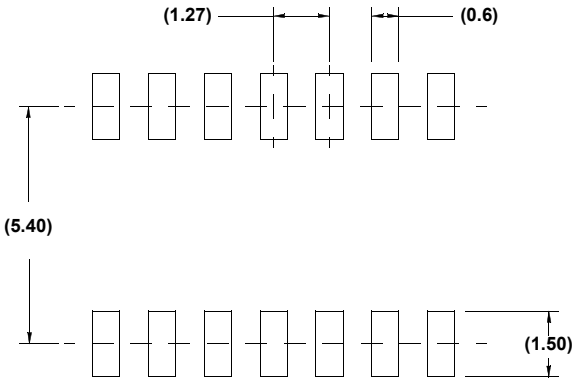




SIDE VIEW



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.