ZL6105-1CH-DEMO1Z Demonstration Board User Guide

Introduction

The ZL6105 is an innovative power conversion and management IC that combines integrated MOSFET drivers with key power and fault management functions in a small package, resulting in a flexible and integrated solution. The ZL6105-1CH-DEMO1Z platform allows quick evaluation of the highly configurable ZL6105's performance and features in either stand-alone mode or via the SMBus™ interface using Intersil's PowerNavigator™ GUI software.

Specifications

This board has been configured and optimized for the following range of operating conditions:

- V_{IN} = 5.5V to 14V
- V_{OUT} = 0.6V to 3.6V
- I_{MAX} = 40A
- f_{SW} = 300kHz to 1333kHz
- Peak efficiency: >90% at 50% load
- Output ripple: <1% at 50% load

Key Features

- Optimized for small circuit footprint
- Onboard enable switch
- Power-good indicator
- SMBus control interface
- Interconnectivity with other Intersil demo boards

References

- ZL6105, Datasheet
- AN2010, "Thermal and Layout Guidelines for Digital-DC™ Products"
- AN2035, "Compensation Using CompZL™"
- AN1779, "Configuring Current Sharing on the ZL6105 and ZL8101"
- TB389, "PCB Land Pattern and Surface Mount Guidelines for QFN Packages"

Ordering Information

PART NUMBER	DESCRIPTION
ZL6105-1CH-DEMO1Z	ZL6105 Evaluation Kit, one channel (EVB, USB adapter, Cable, Software

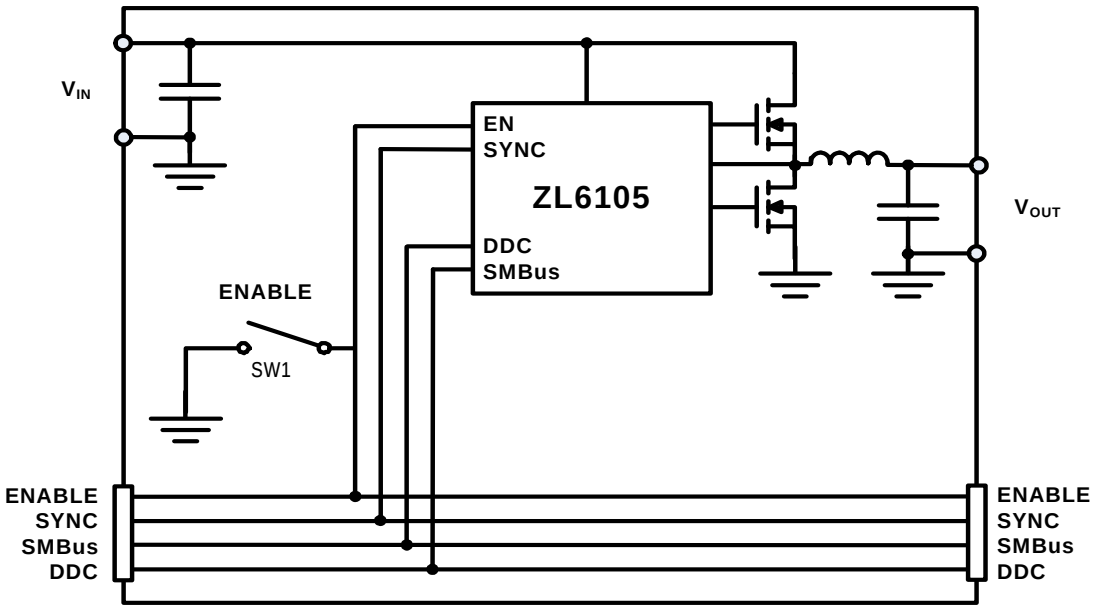


FIGURE 1. ZL6105-1CH-DEMO1Z SIMPLIFIED SCHEMATIC

ZL6105-1CH-DEMO1Z BOARD

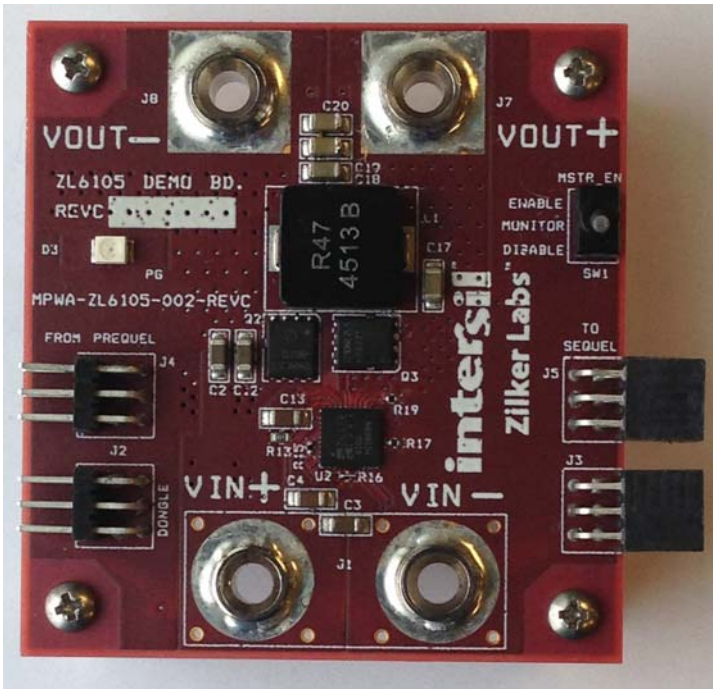


FIGURE 2. TOP SIDE

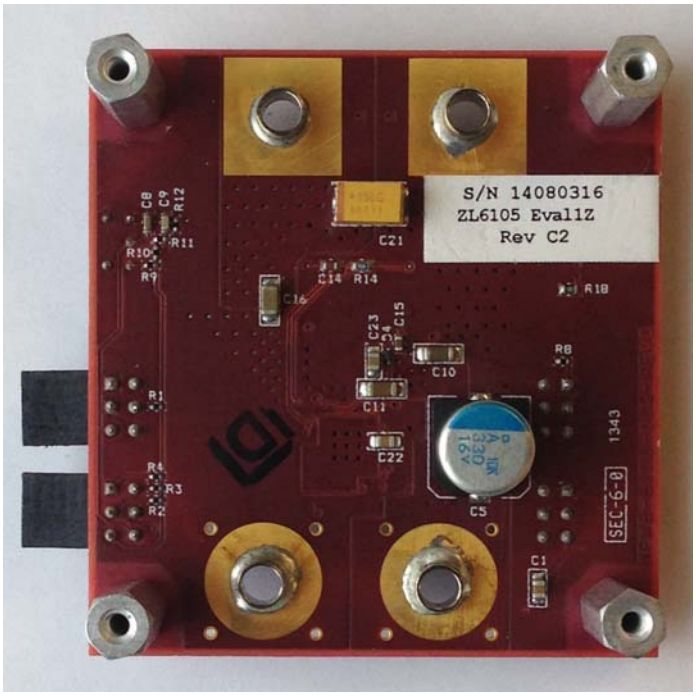


FIGURE 3. BOTTOM SIDE

Functional Description

The ZL6105-1CH-DEMO1Z provides all of the circuitry required to demonstrate features of the ZL6105. The ZL6105-1CH-DEMO1Z has a functionally optimized layout that allows efficient operation up to the maximum output current. Power and load connections are provided through plug-in sockets. Standalone operation is achieved using a combination of pin-strap settings and stored settings. The pin-strap setting details are described in the ZL6105 datasheet. The stored settings are listed on "Default Configuration Settings" on page 14.

The ZL6105-1CH-DEMO1Z Demonstration Board schematics are shown in Figures 4 and 5. The hardware enable function is controlled by a toggle switch. The Power-Good (PG) LED indicates that V_{OUT} is regulating. The right angle headers at opposite ends of the board are for connecting a USB to SMBus control board or for daisy chaining of multiple Intersil evaluation boards.

Connecting multiple Intersil Digital boards allows the user to setup many shared features such as clock synchronization, controlled sequencing, phase spreading and fault spreading within Intersil's PowerNavigator™ software as part of a single power project. This document provides operational instructions, schematics, bill of materials and PCB layers with layout notes for reference. Figures 14 through 19 show performance data taken using this hardware in its optimized configuration. The configuration settings that the hardware ships with are shown on page 14.

Operating Range

By default, the ZL6105-1CH-DEMO1Z is configured to provide 1V at up to 40A at 400kHz f_{SW}. The board can also support a wider operating range and modifying the operating conditions will change the performance results.

The board V_{IN} range is 4.5V to 14V. The board V_{OUT} setting is fixed at 1V by PMBus setting, but the range is programmable from 0.54V to 3.6V (including margin high/low) using the VOUT_COMMAND PMBus command. The maximum value of 3.6V is limited by pin strap. The board I_{OUT} range is 0 to 40A. For continuous operation at 40A, airflow across the board may be needed.

The switching frequency (f_{SW}) is set to 400kHz by PMBus command, but the f_{SW} setting can be changed by using the FREQUENCY_SWITCH PMBus command (while the device is disabled). The f_{SW} range is 300kHz to 1.33MHz.

Quick Start Guide

Stand Alone Operation

1. Ensure that the board is properly connected to the supply and loads before applying any power.
2. Set Enable switch to "DISABLE".
3. Apply Load to V_{OUT+}/V_{OUT-}.
4. Connect the USB adapter cable to the host computer.
5. Connect the USB to SMBus adapter to J2 (Required to provide external power for enable switch).
6. Connect the input power supply to V_{IN+}/V_{IN-}.
7. Turn input supply on.
8. Set Enable switch to "ENABLE".
9. Test ZL6105 operation.

USB (PMBus) Operation

1. Follow steps 1 through 7 of Stand Alone Operation.
2. Download PowerNavigator software from the Intersil website and install.
3. Use the GUI to operate at V_{OUT} up to 3.6V.
4. Set the Enable switch to "ENABLE".
5. Monitor and configure the ZL6105 using the PowerNavigator software.

ZL6105-1CH-DEMO1Z Schematics

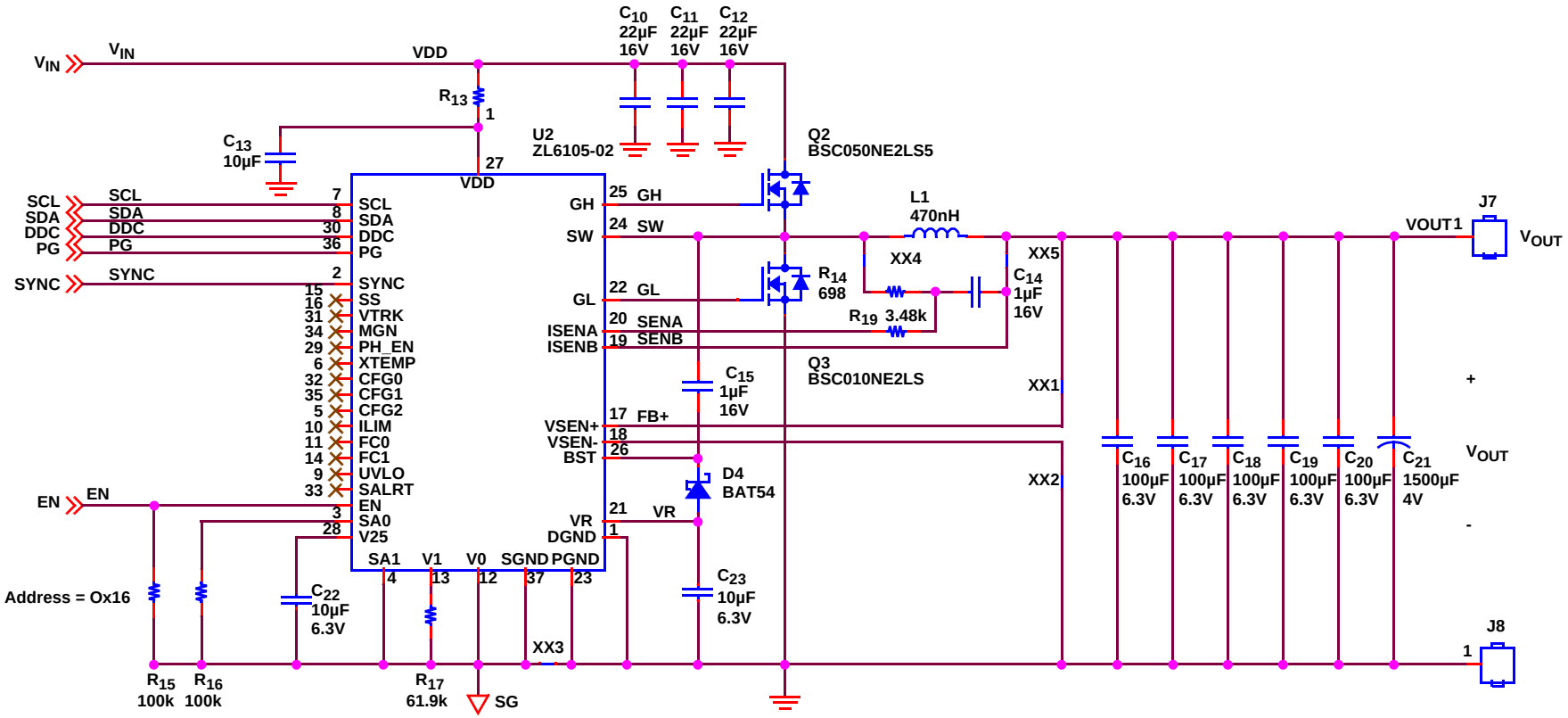


FIGURE 4. ZL6105-1CH-DEMO1Z DEMO BOARD

ZL6105-1CH-DEM01Z Schematics (Continued)

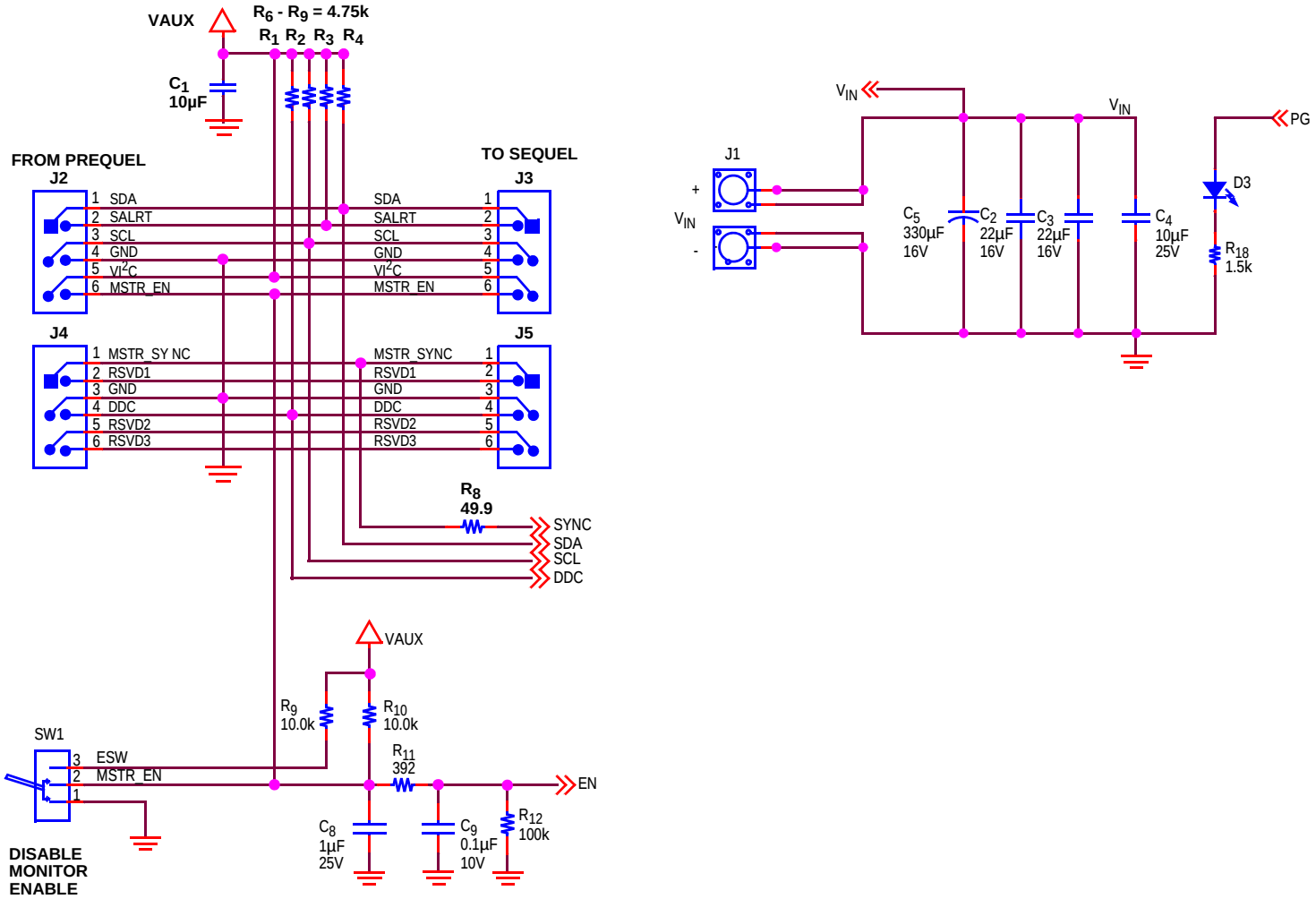


FIGURE 5. ZL6105-1CH-DEM01Z INTERFACE

Bill of Materials

QTY	REFERENCE	VALUE	TOL (%)	RATING	TYPE	PCB FOOTPRINT	MANUFACTURER	PART NUMBER
1	U2	ZL6105				MLF36_6X6BX	Intersil Corporation	
2	C2, C3	22µF	20	16V	X5R	SM1206	Murata	GRM31CR61C226ME15L
1	C4	10µF	10	25V	X5R	SM1206	Panasonic - ECG	ECJ-3YB1E106K
1	C5	330µ	20	16V	AL POLY	SM_CAP_10.5X10.5_PXA_FLD	United Chemi-Con	APXA160ARA331MJC0G
1	C8	1µF	10	25V	X5R	SM0603	Taiyo Yuden	TMK107BJ105KA-T
1	C9	0.1µF	10	10V	X7R	SM0603	Kemet	C0603C104K8RACTU
3	C10, C11, C12	22µF	20	16V	X5R	SM1206	Panasonic - ECG	ECJ-3YB1C226M
1	C13	10µF	10	25V	X7R	SM1206	Taiyo Yuden	TMK316B7106KL-TD
2	C14, C15	1µF	10	16V	X7R	SM0603	AVX Corporation	0603YC105KAT2A
5	C16, C17, C18, C19, C20	100µF	20	6.3V	X5R	SM1206	TDK Corporation	C3216X5R0J107M
1	C21	1500µF	20	4V	AL POLY	SM7343_KEMET_T530_BC	AVX	TPME158K004R0018
2	C22, C23	10µF	10	6.3V	X7R	SM0805	TDK Corporation	CGA4J1X7R0J106K125AC
1	D4	BAT54		30V	Schottky	SOD_523	ON Semiconductor	BAT54XV2T1OS
1	L1	470nH		0.8mΩ	Inductor	IND_HCM1305_XX	Cooper Bussmann	HCM1305-R47-R
1	Q2	BSC050NE2LS5		30V		PG_TDSON_8_LAS	Infineon	
1	Q3	BSC010NE2LS		30V		PG_TDSON_8_LAS	Infineon	
4	R1, R2, R3, R4	4.75k	1		1/16W	SM0402	Panasonic - ECG	ERJ-2RKF4751X
1	R13	1	1		1/16W	SM0603	Panasonic - ECG	ERJ-3RQF1R0V
1	R14	953	1		1/16W	SM0603	Panasonic	ERJ-3EKF9530V
2	R15, R16	100k	1		1/16W	SM0402	Vishay/Dale	CRCW0402100KFKED
1	R17	133k	1		1/16W	SM0402	Panasonic - ECG	ERJ-2RKF1333X
1	R19	3.48k	1		1/16W	SM0402	Panasonic - ECG	ERJ-2RKF3481X
ANCILLARY PARTS SPECIFIC TO DEMO BOARD OPERATION								
1	C1	10µF	10	10V	X7R	SM0805	Taiyo Yuden	LMK212B7106KG-TD
1	D3	GRN		1.8V		DIO_LG_T67K	Osram	LG T67K-H2K1-24-Z
2	J2, J4	HDR_3x2_RA			RA	HDRM3DUALRA100X100	SAMTEC	TSW-103-08-T-D-RA
2	J3, J5	SKT_3x2_RA			RA	HDRF3DUALRA100X100	SAMTEC	SSQ-103-02-T-D-RA
1	R8	49.9	1	100mW	THK FILM	SM0402	PANASONIC-ECG	ERJ-2RKF49R9X
2	R9, R10	10.0k	1	63mW	THK FILM	SM0402	Panasonic - ECG	ERJ-2RKF1002X
1	R11	392	1	100mW	THK FILM	SM0402	Panasonic	ERJ-2RKF3920X
1	R12	100k	1	63mW	THK FILM	SM0402	Panasonic - ECG	ERJ-2RKF1003X
1	R18	1.5K	1	63mW	THK FILM	SM0603	Panasonic - ECG	ERJ-3EKF1501V
1	SW1	SW_SPDT			PCB VERT	SW_TOG_ULTRAMIN_SPDT	NKK	G13AP-RO

Bill of Materials (Continued)

QTY	REFERENCE	VALUE	TOL (%)	RATING	TYPE	PCB FOOTPRINT	MANUFACTURER	PART NUMBER
4	J1A, J1B, J7, J8	JACK_BANANA				JACK_KEYSTONE_575-4	Keystone Electronics	575-4
4		STANDOFF_#4-40.75LG				STANDOFF_4-40_NDH		
4		SCREW_#4-40.25"				SCREW_4-40		

Measured Data

The following data was obtained using a ZL6105-1CH-DEM01Z evaluation board. V_{IN} = 12V for all data.

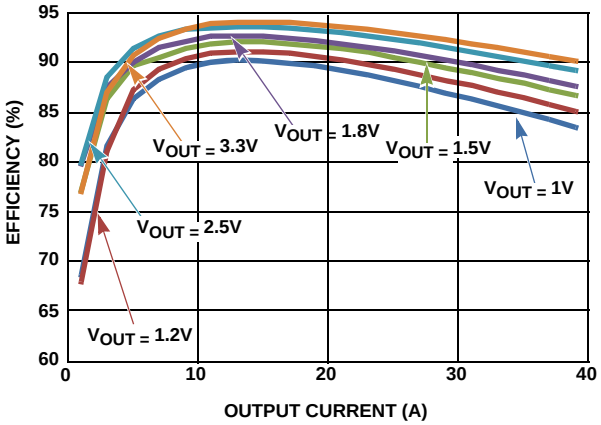


FIGURE 6. EFFICIENCY DATA AT 300kHz

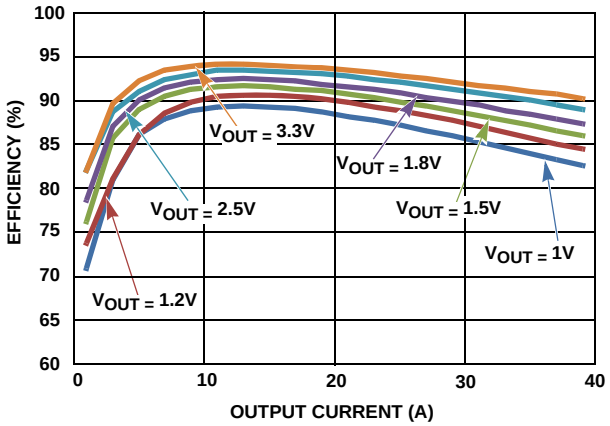


FIGURE 7. EFFICIENCY DATA AT 400kHz

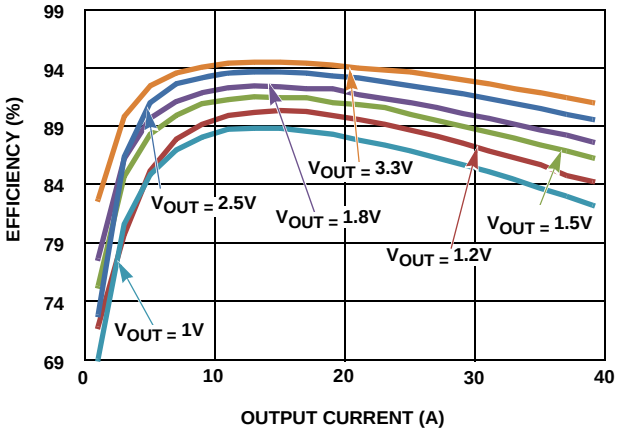


FIGURE 8. EFFICIENCY DATA AT 500kHz

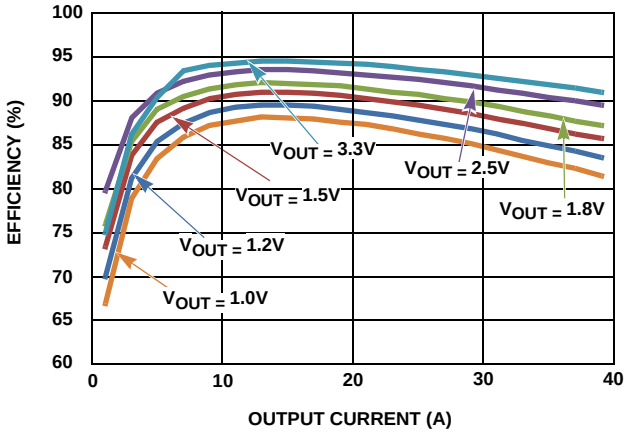


FIGURE 9. EFFICIENCY DATA AT 600kHz

Measured Data

The following data was obtained using a ZL6105-1CH-DEMO1Z evaluation board. V_{IN} = 12V for all data. **(Continued)**

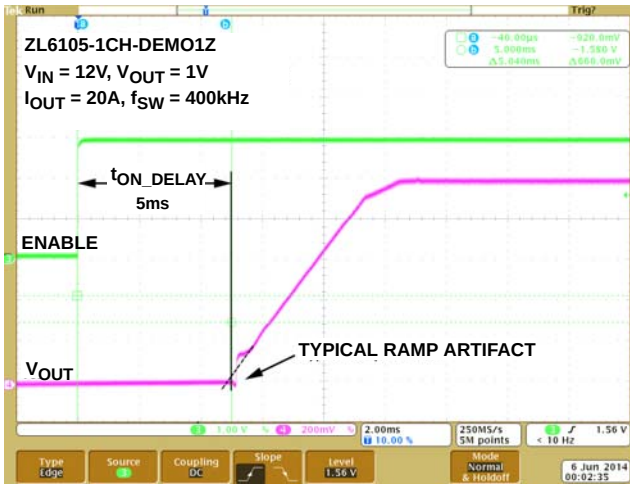


FIGURE 10. TYPICAL TURN-ON RAMP, TRISE = 5ms, t_{ON}_DELAY = 5ms

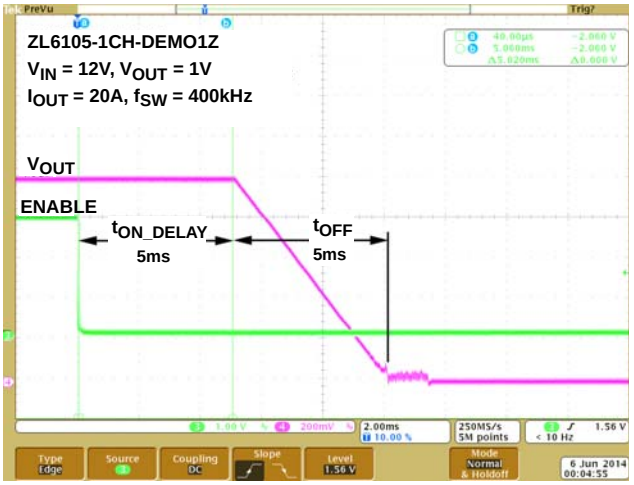


FIGURE 11. TYPICAL TURN-OFF RAMP, t_{FALL} = 5ms, t_{OFF}_DELAY = 5ms

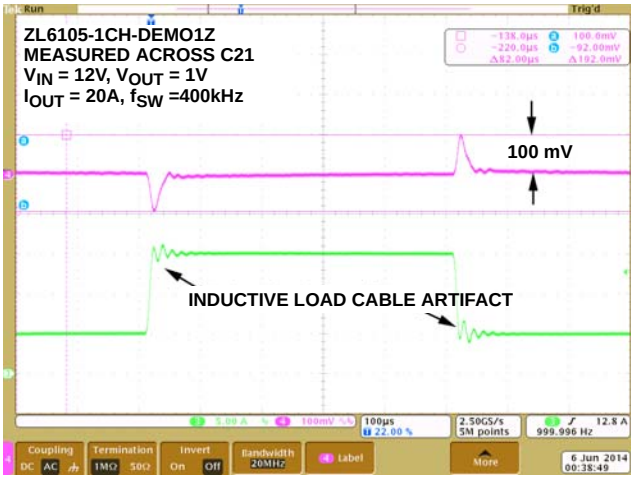


FIGURE 12. TRANSIENT RESPONSE 5 TO 15A, 5A/µ

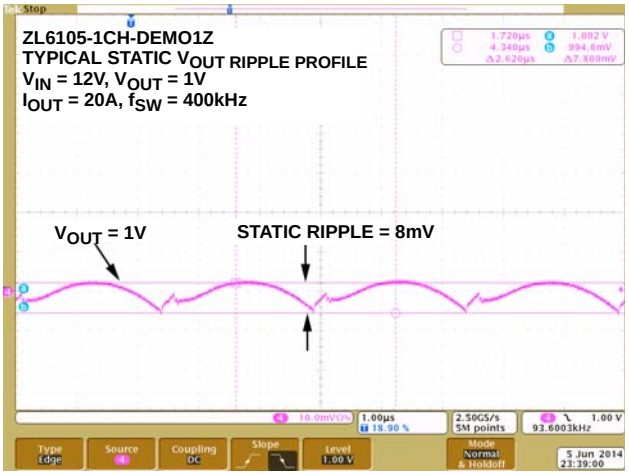


FIGURE 13. STATIC RIPPLE

ZL6105 PCB Layout Guidelines

Device Ground Pins

- SGND is the analog reference for VDD, VR, V25, XTEMP and the pin straps. Very little current passes through this path normally.
- DGND is the high current digital GND return path for the controller. It is isolated internally from SGND to avoid noise coupling.
- PGND is the high current GND return for the MOSFET drivers and the bootstrap circuit. It is isolated internally from SGND to avoid noise coupling.

Ground Pin Usage

- The pins are isolated within the device only to avoid noise coupling through the package and bond wires. They should be tied together on the PCB with a very low impedance connection for best operation. If the DGND pin is not closely coupled to SGND, the SGND pin will become a current path for digital circuits and will get noisy.

Device Power Supply Pins

- VDD is the input supply pin. It provides power to the internal VR regulator.
- VR is the internal 5V regulator used to power the MOSFET drivers and the V25 regulator.
- V25 is the internal 2.5V regulator used to power the digital circuits.

Power Supply Pin Usage

- VDD, VR and V25 are all referenced to SGND and all need to have capacitors placed closely to the pins.

ZL6105 Voltage, Current and Temperature Sense Connections

- Ensure that the current sense signals are routed differentially and that the averaging circuit is Kelvin connected to the sensing element for most accurate current sense.
- Ensure that the voltage sense signals are routed differentially and are Kelvin connected to the final capacitor away from the inductor for best noise performance.
- Ensure that the XTEMP and SGND traces are routed differentially to the temperature sensing transistor.

ZL6105-1CH-DEM01Z Board Layout - 6 Layers

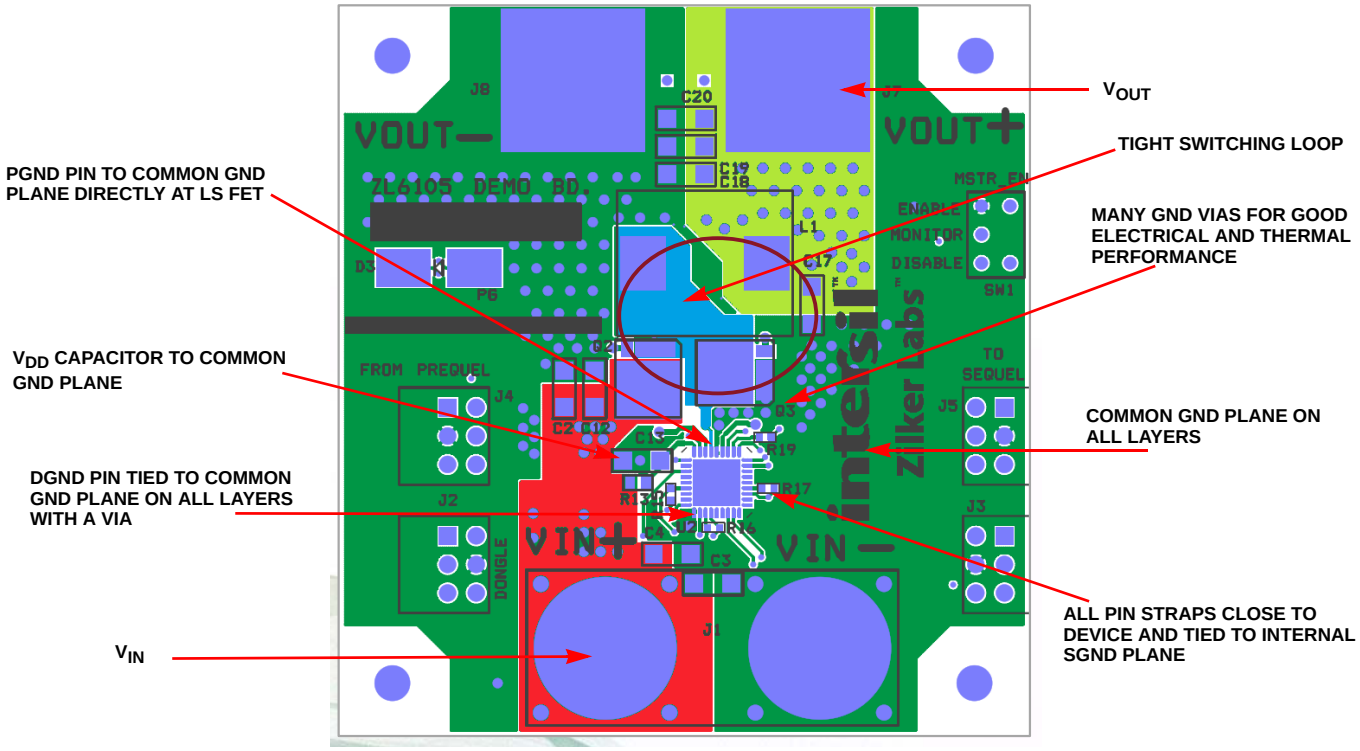


FIGURE 14. PCB TOP LAYER

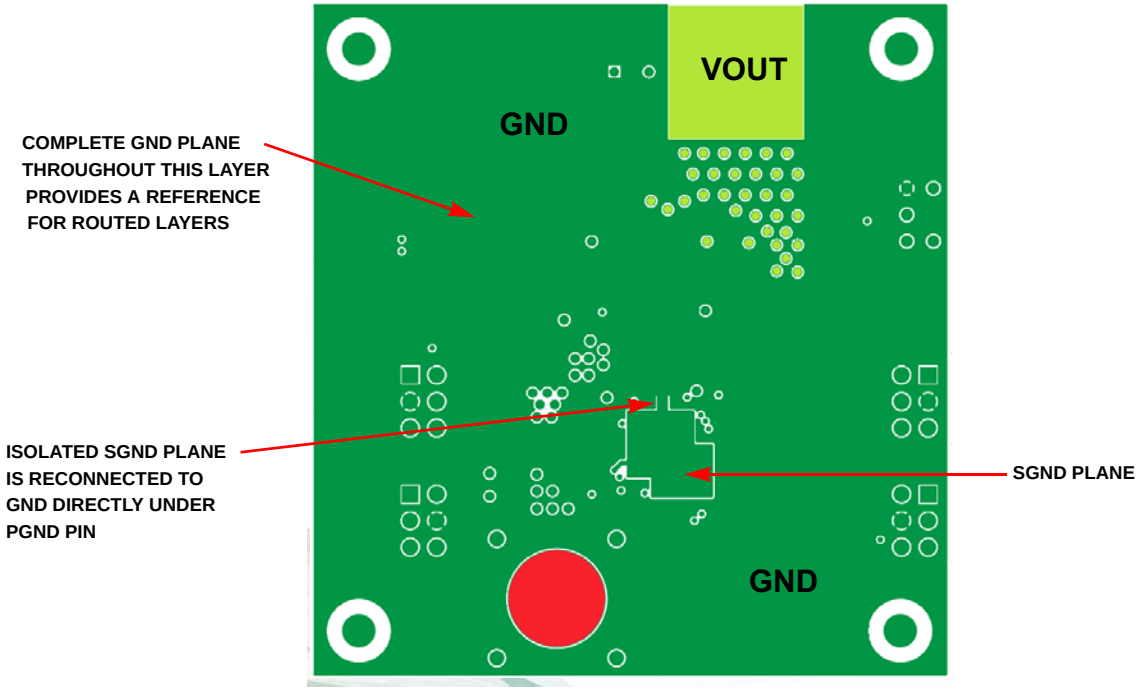


FIGURE 15. INNER LAYER 1

ZL6105-1CH-DEMO1Z Board Layout - 6 Layers

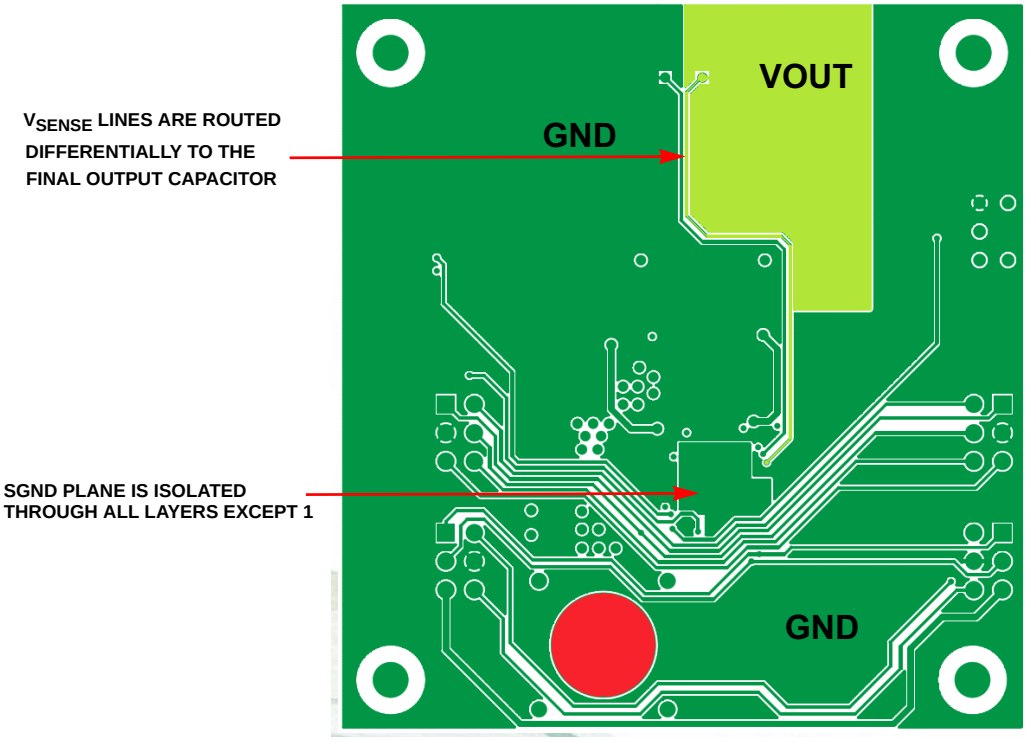


FIGURE 16. INNER LAYER 2

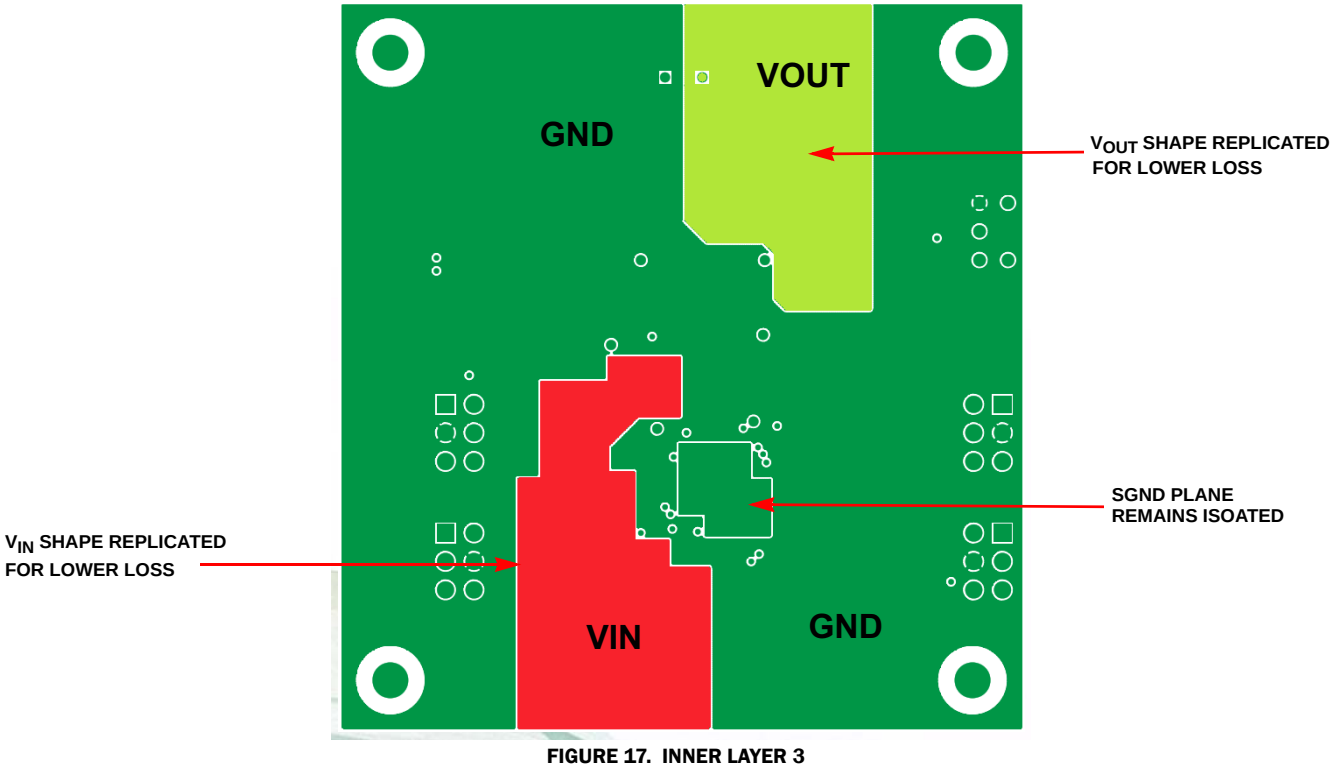


FIGURE 17. INNER LAYER 3

ZL6105-1CH-DEMO1Z Board Layout - 6 Layers

REPLICATION OF INNER LAYER 3 FOR LOWER LOSS

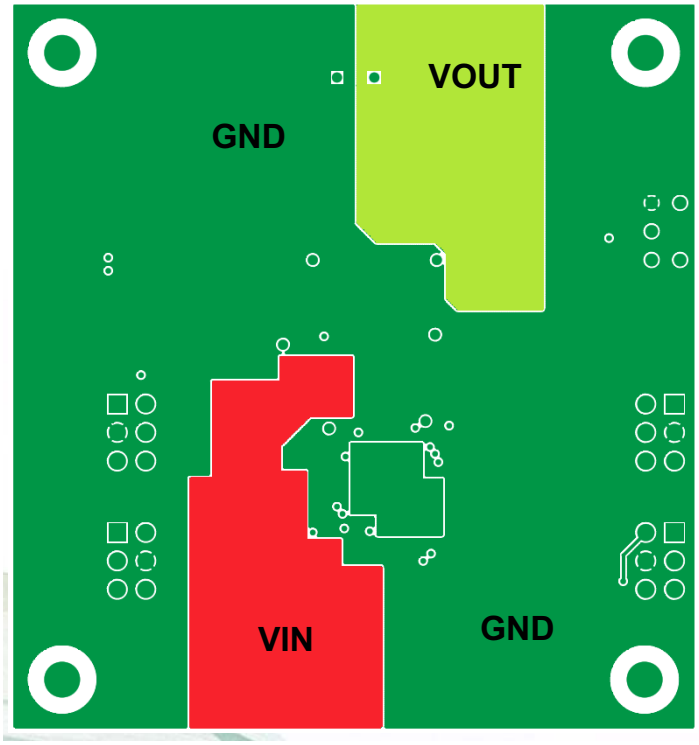
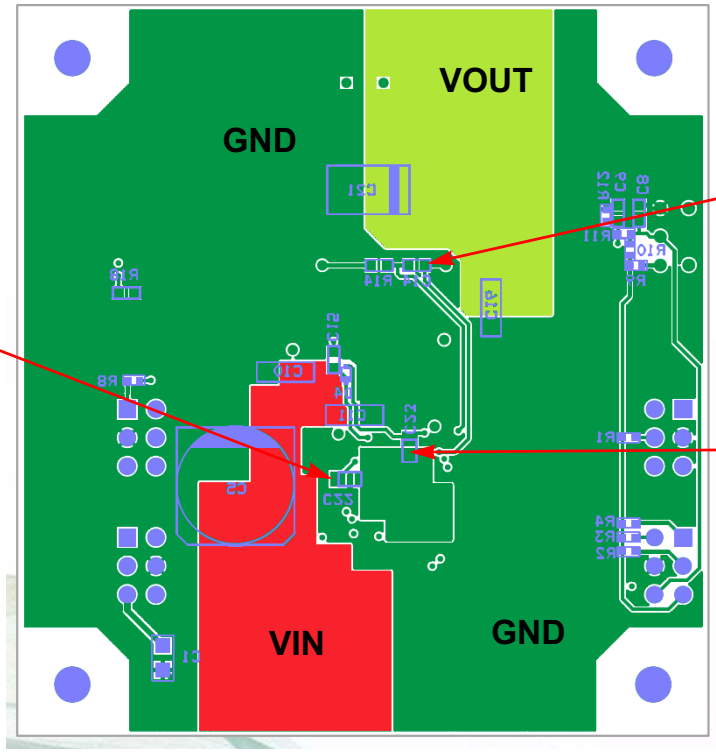


FIGURE 18. INNER LAYER 4



I_{SENSE} LINES ARE ROUTED DIFFERENTIALLY AND KELVIN CONNECTED TO THE INDUCTOR

V25 CAPACITOR CLOSE TO THE DEVICE AND TIED TO SGND PLANE

VR CAPACITOR CLOSE TO THE DEVICE AND TIED TO SGND PLANE NEAR THE SGND/GND RECONNECTION POINT

FIGURE 19. BOTTOM LAYER

Default Configuration Settings

The following configuration file is loaded into the ZL6105 on the ZL6105-1CH-DEM01Z in the Default Store. The # symbol is used to denote comments. Anything following the # symbol is ignored.

PMBus COMMAND	VALUE	NOTES
ON_OFF_CONFIG	0x17	#Pin Enable, immediate off
MFR_ID	Intersil	
MFR_MODEL	ZL6105-1CH-DEM01Z	
MFR_LOCATION	Austin, TX	
MFR_REVISION	Rev 1.0	
VOUT_COMMAND	1	#V
VOUT_UV_FAULT_RESPONSE	0x80	#Immediate shutdown
OVUV_CONFIG	0x00	#Disabled
IOUT_CAL_GAIN	0.84	#mΩ
IOUT_OC_FAULT_LIMIT	50	#A
IOUT_AVG_OC_FAULT_LIMIT	50	#A
IOUT_UC_FAULT_LIMIT	-30	#A
IOUT_AVG_UC_FAULT_LIMIT	-30	#A
FREQUENCY_SWITCH	400	#kHz
DEADTIME	0x2020	#32ns
DEADTIME_CONFIG	0x0606	#2ns Min, Dynamic
DEADTIME_MAX	0x2020	#32,56ns Max
INDUCTOR	0.47	#µH
MFR_CONFIG	0x8412	
USER_CONFIG	0x0011	
TEMPCO_CONFIG	0x28	
MISC_CONFIG	0x2000	
AUTO_COMP_CONFIG	0x79	#Enabled, 80% Gain
STORE_DEFAULT_ALL		
RESTORE_DEFAULT_ALL		
RESTORE_USER_ALL		