ZL8801-2PH-DEMO1Z Demonstration Board User Guide

The ZL8801 is a digital power conversion and management IC that combines an efficient step-down DC/DC converter with key power and thermal management functions in a single package. The ZL8801 incorporates a fully digital, compensation-free, ChargeMode™ control to achieve single-cycle transient response.

The ZL8801-2PH-DEMO1Z demonstration board is a 6-layer board demonstrating a 2-phase 80A synchronous buck converter. Sequencing, margining, plus other features can be evaluated using this demonstration board.

An USB-to-PMBus™ adapter board (ZLUSBEVAL3Z, included with the demonstration kit) is used to connect the demonstration board to a PC. Intersil's PowerNavigator™ evaluation software can then be used to evaluate the full PMBus functionality of the part using a PC running Microsoft Windows XP, 7 or 8.

Key Features

- 2-phase 80A synchronous buck converter with compensation-free ChargeMode control
- Designed to be easy to use and modify. Optimized for small circuit footprint and dynamic response
- Configurable through PMBus
- V_{IN} range of 4.5V to 14V, V_{OUT} adjustable from 0.54 to 2.0V (Device can be adjusted to 5.5V with 6.3V output capacitors)
- Enable switch and power-good indicator

Specifications

- V_{IN} = 12V
- V_{OUT} = 1.2V/80A max
- f_{SW} = 500kHz
- Efficiency: 91% at 40A
- Output ripple: ±1%
- Dynamic response: ±1% (50% to 100% to 50% load step, di/dt = 10A/µs)
- Board temperature: +25°C

References

ZL8801 datasheet

ISL99140 datasheet

Digital Power Design Center

AN1900, "USB to PMBus™ Adapter"

Ordering Information

PART NUMBER	DESCRIPTION
ZL8801-2PH-DEMO1Z	ZL8801 Demonstration Kit (Evaluation Board, USB Adapter, Cable)

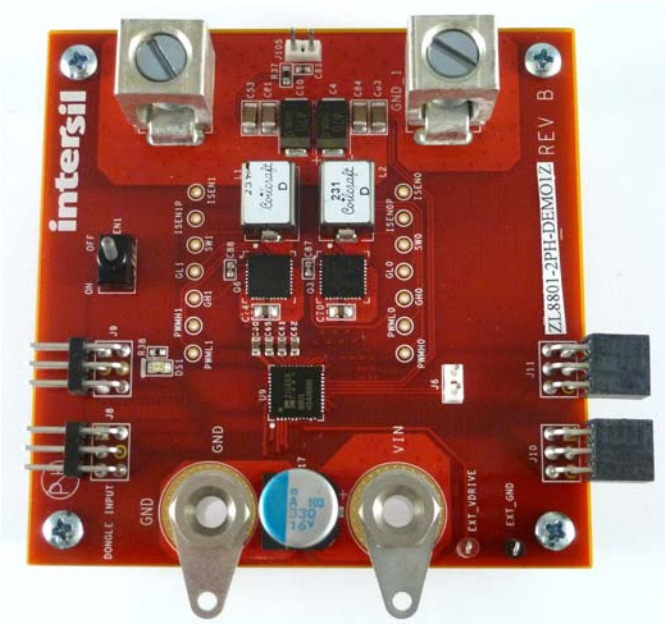


FIGURE 1. TOP VIEW

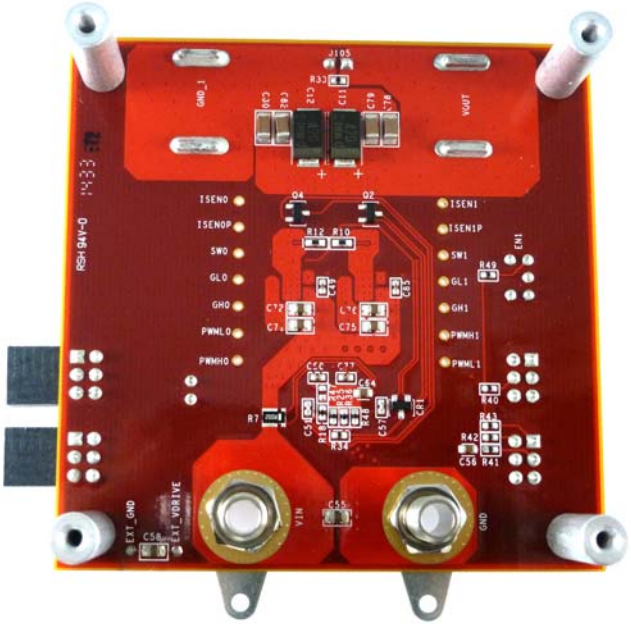


FIGURE 2. BOTTOM VIEW

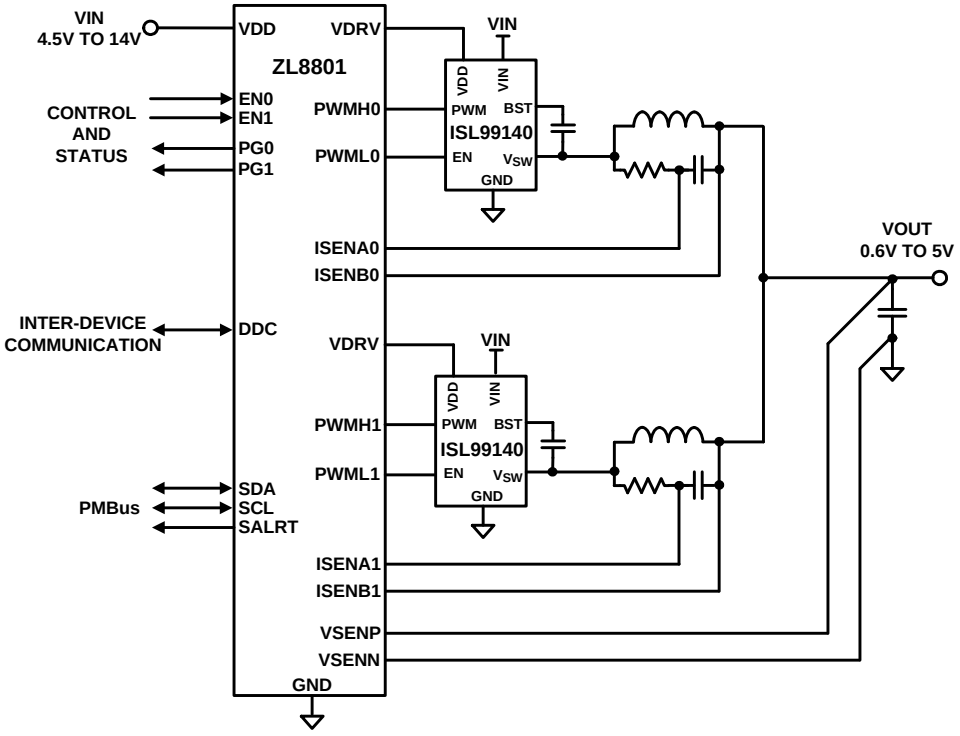


FIGURE 3. ZL8801-2PH-DEM01Z SIMPLIFIED SCHEMATIC

Functional Description

The ZL8801-2PH-DEM01Z provides all circuitry required to demonstrate the features of the ZL8801. The ZL8801-2PH-DEM01Z has a functionally-optimized ZL8801 circuit layout that allows efficient operation up to the maximum output current.

A majority of the features of the ZL8801, such as compensation-free ChargeMode control, soft-start delay and ramp times, supply sequencing, voltage tracking and voltage margining are available on this demonstration board. For voltage tracking and sequencing demonstration, the board can be connected to any other Intersil demonstration board that supports the Digital-DC™ (DDC) bus.

Figure 3 shows a simplified schematic diagram of the ZL8801-2PH-DEM01Z board.

The hardware enable function is controlled by a toggle switch on the ZL8801-2PH-DEM01Z board. The power-good (PG) LEDs indicate the correct state of PG when external power is applied to the ZL8801-2PH-DEM01Z board. The right angle headers at opposite ends of the board are for connecting a USB to PMBus adapter board or for daisy chaining multiple demonstration boards together to build multi-output configurations.

"ZL8801-2PH-DEM01Z Schematic" on page 4 shows the detailed demonstration circuit. Figures 5 through 11 show typical performance data and Figures 16 through 23 show the PCB board layout. The default configuration file is given on page 6, and the Bill of Materials (BOM) is included for reference beginning on page 5.

Operation

PMBus Operation

The ZL8801 utilizes the PMBus protocol. The PMBus functionality can be controlled via USB from a PC running the PowerNavigator evaluation software in Windows XP, 7 or 8 operating systems.

Install the evaluation software from the following Intersil website:
http://www.intersil.com/powernavigator

For board operation, connect the included USB-to-PMBus adapter board to J8 of the ZL8801-2PH-DEM01Z board labeled "DONGLE". Connect the desired load and an appropriate power supply to the input and connect the included USB cable to the PC running the PowerNavigator evaluation software. Place the ENABLE switches in "DISABLE" and turn on the power.

The evaluation software allows modification of all ZL8801 PMBus parameters. The ZL8801 device on the board has been pre-configured as described in this document, but the user may modify the operating parameters through the evaluation software or by loading a predefined set-up from a configuration file.

The ENABLE switch can then be moved to "ENABLE" and the ZL8801-2PH-DEM01Z board can be tested. Alternately, the PMBus ON_OFF_CONFIG and OPERATION commands may be used from the PowerNavigator GUI.

Quick Start Guide

Stand Alone Operation

1. Set ENABLE switch to “DISABLE”.
2. Apply load to VOUT0 and/or VOUT1.
3. Connect the USB to PMBus adapter board to J8 (labeled “DONGLE”) of ZL8801-2PH-DEMO1Z.
4. Connect supplied USB cable from computer to USB to PMBus adapter board.
5. Connect power supply to VIN (supply turned off).
6. Turn power supply on.
7. Set ENABLE switch to “ENABLE”.
8. Monitor ZL8801-2PH-DEMO1Z board operation using an oscilloscope.

USB (PMBus) Operation

1. Set ENABLE switch to “DISABLE”.
2. Apply load to VOUT and/or VOUT1.
3. Connect power supply to VIN (supply turned off).
4. Turn power supply on.
5. Connect USB to PMBus adapter board to J8 of ZL8801-2PH-DEMO1Z.
6. Connect supplied USB cable from computer to USB to PMBus adapter board.

Install the PowerNavigator evaluation software from the following Intersil website:
http://www.intersil.com/powernavigator

7. Set ENABLE switch to “ENABLE”.
8. Monitor and configure the ZL8801-2PH-DEMO1Z board using PMBus commands in the evaluation software.
9. Test the ZL8801-2PH-DEMO1Z operation using an oscilloscope and the evaluation software.

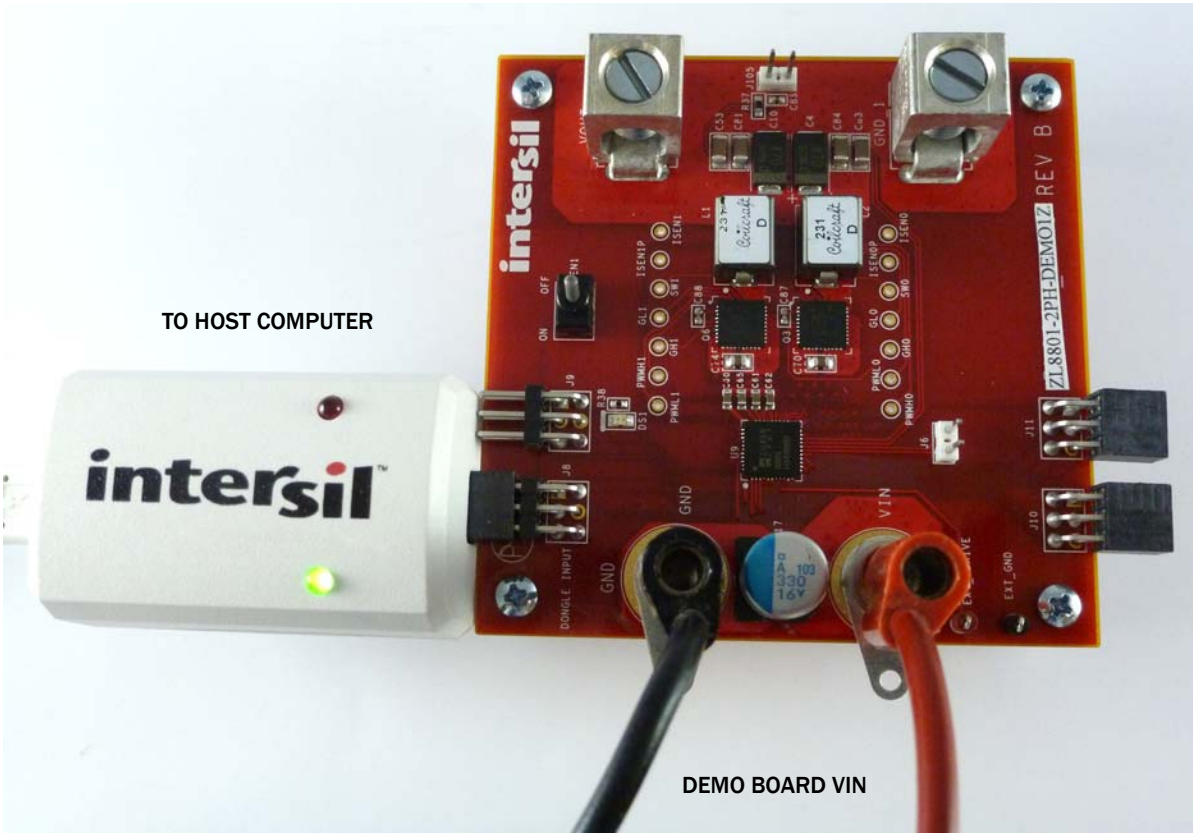
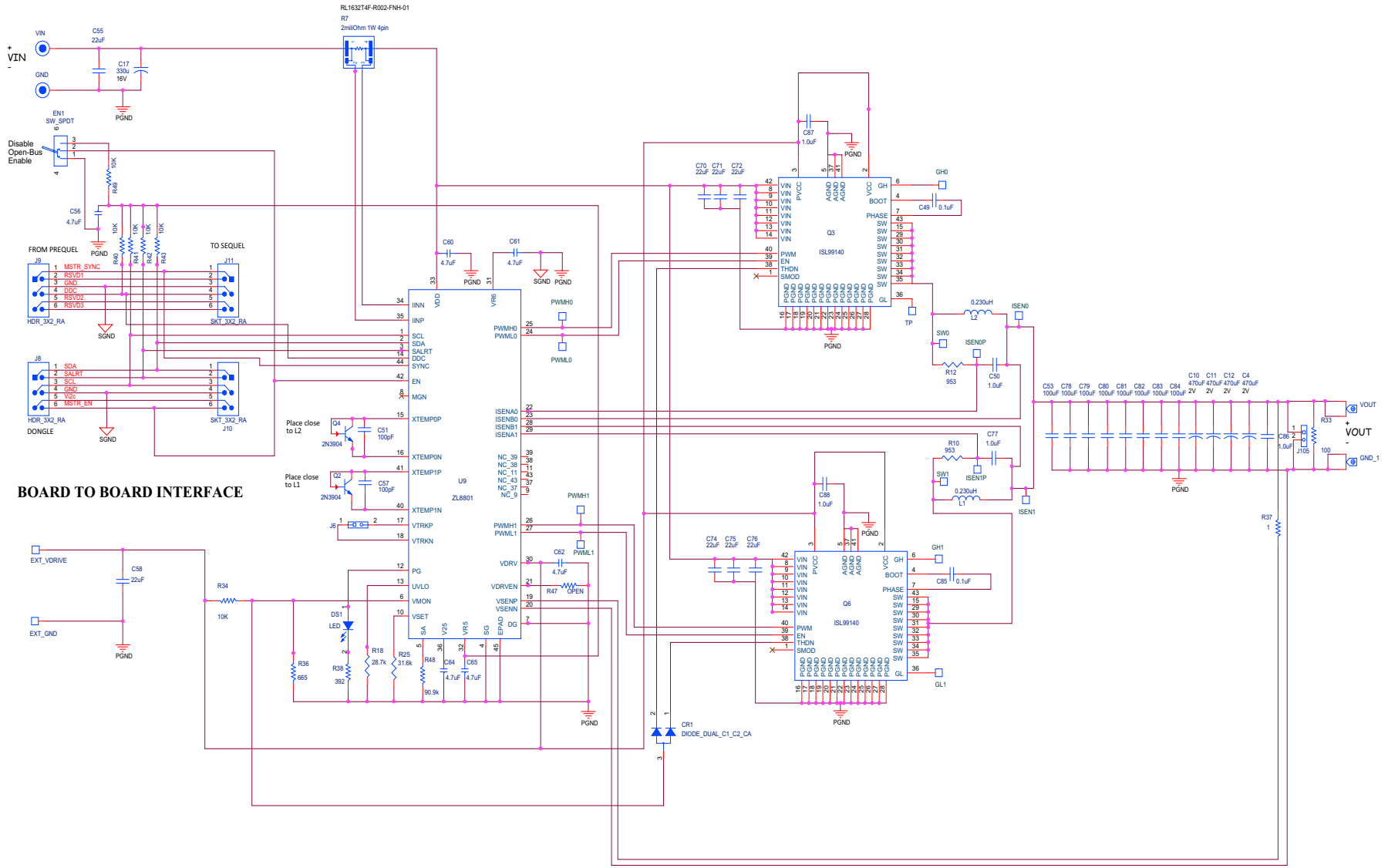


FIGURE 4. ZL8801 DEMONSTRATION KIT SET-UP

ZL8801-2PH-DEMO1Z Schematic



Bill of Materials

QTY	REFERENCE DESIGNATOR	DESCRIPTION	PCB FOOTPRINT	MANUFACTURER	PART NUMBER
1	U9	ZL8801	QFN44_275X275	Intersil	ZL8801
2	Q3, Q6	ISL99140	QFN40_236X236	Intersil	ISL99140
1	CR1	BAT54A-T	SOT23	NXP Semiconductor	BAT54A, 215
4	C4, C10, C11, C12	470µF/2V	CAP_7343	Panasonic	EEF-SX0D471E4
1	C17	330µF	CAPAE_315X244	United Chemi-Con	APXA160ARA331MJC0G
2	C49, C85	0.1µF/16V/X7R	sm0402	TDK	C1005X7R1C104K050BC
5	C50, C77, C86, C87, C88	1.0µF/6.3V/X5R	sm0402	TDK	C1005X7S1A105K050BC
2	C51, C57	100pF/50V/COG-NPO	sm0402	TDK	C1005C0G1H101K050BA
8	C53, C78, C79, C80, C81, C82, C83, C84	100µF/6.3V/X5R	sm1206	TDK	C3216X5R0J107M160AB
8	C55, C58, C70, C71, C72, C74, C75, C76	22µF/16V/X5R	sm0805	TDK	C2012X5R1C226M085AC
6	C56, C60, C61, C62, C64, C65	4.7µF/16V/X5R	CAP_0603	TDK	C1608X5R1C475K080AC
2	L1, L2	0.230µH	IND_PA0511	Coil Craft	SLC1175-231ME_
2	Q2, Q4	2N3904	SOT23	On Semiconductor	MMBT3904LT1G
1	R7	2mΩ 1W 4pin	RL1632T4F	Cyntec	RL1632T4F-R002-F NH-01
2	R10, R12	953	SM0603	Panasonic	ERJ-3EKF9530V
1	R18	28.7k	SM0402	Panasonic	ERJ-2RKF2872X
1	R25	31.6k	SM0402	Panasonic	ERJ-2RKF3162X
1	R33	100	SM0402	Panasonic	ERJ-2RKF1000X
1	R36	665	SM0402	Panasonic	ERJ-2RKF6650X
1	R37	1	sm0603	Panasonic	ERJ-3RQF1R0V
1	R38	392	SM0402	Panasonic	ERJ-2RKF3920X
6	R40, R41, R42, R43, R49, R34	10k	SM0402	Panasonic	ERJ-2RKF1002X
0	R47	OPEN	SM0402	-	-
1	R48	90.9k	SM0402	Panasonic	ERJ-2RKF9092X
DEMONSTRATION BOARD SPECIFIC AUXILIARY PARTS BILL OF MATERIALS					
1	DS1	LED	sm0805	Chicago Miniature	CMD17-21VGC/TR8
1	EN1	SW_SPDT (3 position)	SW_GT13MCBE	C&K Components	GT13MCBE
1	EXT_VDRIVE	T POINT S RED	TP_41C60P	Keystone Electronics	5000
1	EXT_GND	T POINT S BLACK	TP_41C60P	Keystone Electronics	5001
2	VIN, GND	Banana_J	BAN-JACK	Emerson	108-0740-00
2	GND_1, VOUT	LUG	B2C-PCB	Lugs Direct	B2C-PCB
2	J6, J105	2 POS	CONN2	Samtec	TSW-102-07-L-S
2	J8, J9	HDR_3X2_RA	CONN6	Samtec	TSW-103-08-T-D-RA
2	J10, J11	SKT_3X2_RA	CONN6	Samtec	SSQ-103-02-T-D-RA

Configuration File

The following text is loaded into the ZL8801 device on the ZL8801-2PH-DEMO1Z as default settings. Each PMBus command is loaded via the PowerNavigator software. The # symbol is used for a comment line.

```
# Initialize device to factory settings

RESTORE_FACTORY
STORE_DEFAULT_ALL
STORE_USER_ALL

### Begin Default Store
RESTORE_DEFAULT_ALL

ON_OFF_CONFIG                0x17
VOUT_MAX                     0x4000          # 2 V
VOUT_COMMAND                 0x2000          # 1 V
VOUT_MARGIN_HIGH             0x219a          # 1.05 V
VOUT_MARGIN_LOW              0x1e66          # 0.95 V
FREQUENCY_SWITCH             0xfbe8          # 500 kHz
VOUT_OV_FAULT_LIMIT          0x235c          # 1.105 V
VOUT_UV_FAULT_LIMIT          0x1ca4          # 0.895 V
IOUT_OC_FAULT_LIMIT          0xe320          # 50 A
IOUT_UC_FAULT_LIMIT          0xe4e0          # -50 A
POWER_GOOD_ON                0x1ccd          # 0.9 V
IOUT0_CAL_GAIN               0xb11e          # 0.279 mV/A
IOUT1_CAL_GAIN               0xb11e          # 0.279 mV/A
USER_CONFIG                  0x2686
IIN_CAL_GAIN                 0xc300          # 3 mV/A
DDC_CONFIG                   0xa01
POWER_GOOD_DELAY             0xca00          # 4 ms
INDUCTOR                     0xb0eb          # 0.229 uH
TEMPCO_CONFIG                0xa7
DEADTIME_CONFIG              0x8888
ASCR_CONFIG                  0x015a0190
SEQUENCE                     0x0
DDC_GROUP                    0x2fc00000
IOUT_AVG_OC_FAULT_LIMIT      0xe230          # 35 A
IOUT_AVG_UC_FAULT_LIMIT      0xe5d0          # -35 A
MFR_VMON_OV_FAULT_LIMIT      0xcb00          # 6 V

STORE_DEFAULT_ALL
### End Default Store
```

PCB Layout Guidelines

For best performance with the ZL8801, please use the following layout guidelines:

- SGND is the analog reference for VDD, VR6, VR5 and V25 and all pin-strap pins. It should connect to the system ground on internal PCB layers. The ZL8801 paddle should then connect to SGND with multiple vias for electrical and thermal relief.
- DGND is the digital GND return path for the controller. It should connect to the SGND shape using a single point, low impedance connection.
- The VDD pin is the input supply pin for the ZL8801, and is also used for V_{IN} telemetry. The VR6, VR5 and V25 pins are outputs of regulators used to bias internal circuitry. Ceramic decoupling capacitors on these pins should be placed close to their respective pin with a tight connection to SGND.
- The voltage sense lines should be routed differentially from the regulation point back to the ZL8801. Be sure to avoid any noisy areas when routing (such as the switch node) for best performance.
- The current sense traces used for DCR sensing need to connect to the inductor pads using a kelvin connection. This minimizes stray PCB resistance in the current sense network, maximizing current sense accuracy. The resistor in the RC current sense network can be placed by the output inductor, but the capacitor should be placed by the controller.
- The XTEMPxP and XTEMPxN signals should be routed as a differential pair from the external NPN sensor back to the controller, avoiding any noisy areas on the PCB. Up to a 100pF capacitor can be placed across these pins for noise filtering.
- Ceramic input caps for the power stage need to be placed close to the ISL99140 input pins, with a tight loop between the ISL99140 VIN and PGND connections. The ceramic decoupling capacitor for the ISL99140 VCC and PVCC pins should be placed close to those pins.
- Please see the ZL8801 datasheet for guidance on component selection, including input capacitors, output capacitors, and the output inductor.

Measured Data

The following data was acquired using a ZL8801-2PH-DEM01Z demonstration board.

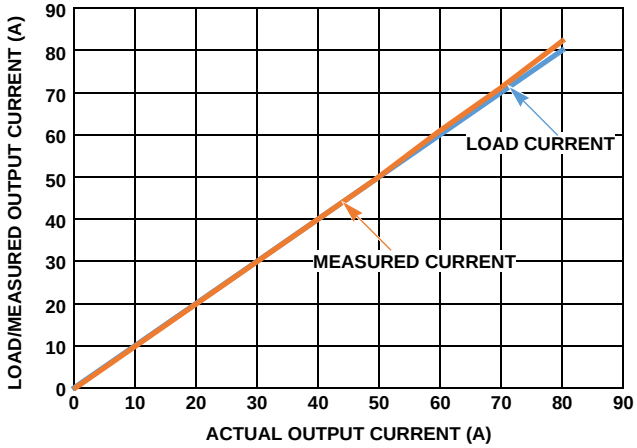


FIGURE 5. OUTPUT CURRENT MEASUREMENT ACCURACY (SINGLE-PHASE)

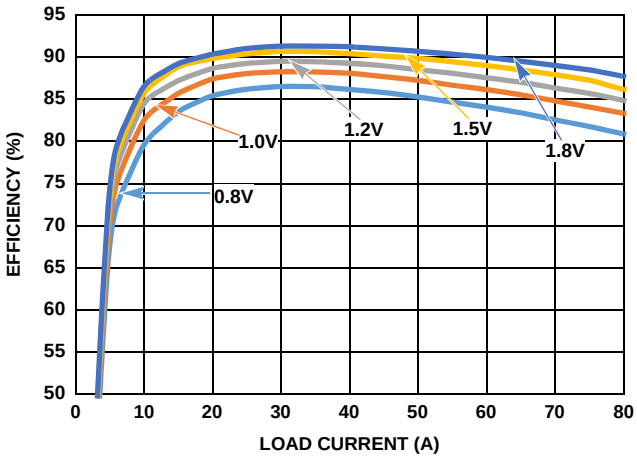


FIGURE 6. EFFICIENCY, V_{IN} = 12V, f_{SW} = 300kHz

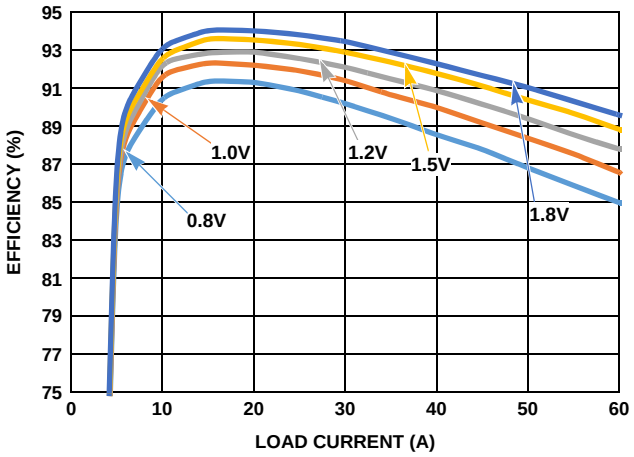


FIGURE 7. EFFICIENCY, V_{IN} = 5V, f_{SW} = 300kHz

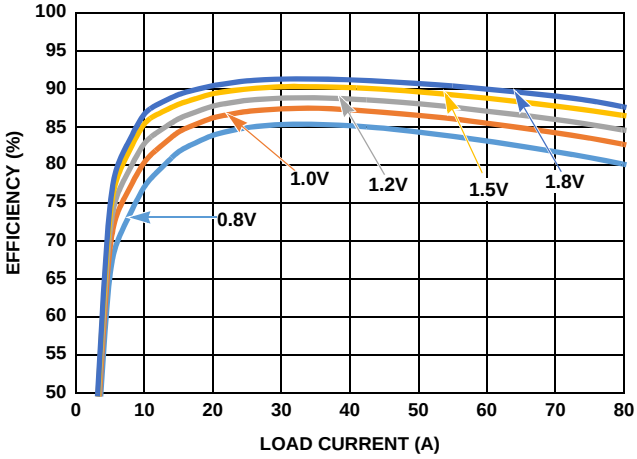


FIGURE 8. EFFICIENCY, V_{IN} = 12V, f_{SW} = 400kHz

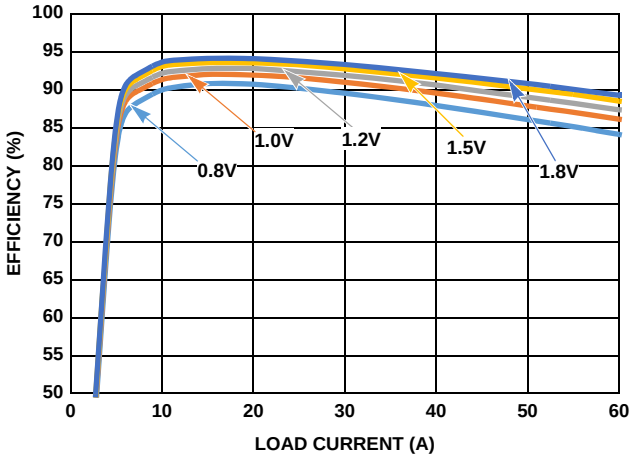


FIGURE 9. EFFICIENCY, V_{IN} = 5V, f_{SW} = 400kHz

Measured Data

The following data was acquired using a ZL8801-2PH-DEMO1Z demonstration board. **(Continued)**

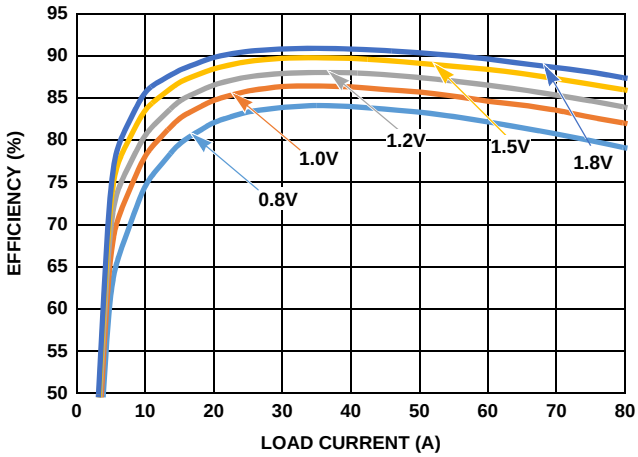


FIGURE 10. EFFICIENCY, V_{IN} = 12V, f_{SW} = 516kHz

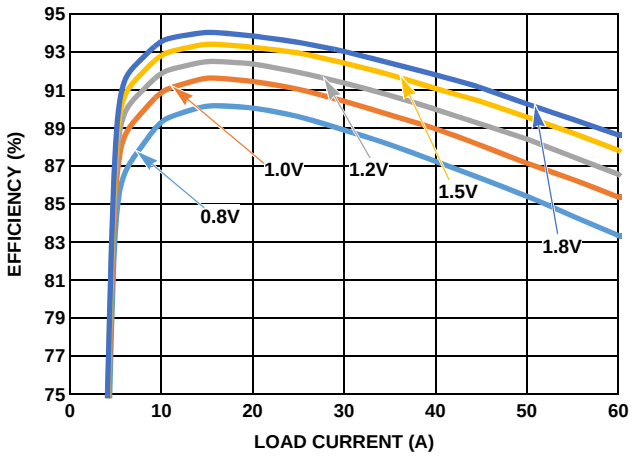


FIGURE 11. EFFICIENCY, V_{IN} = 5V, f_{SW} = 516kHz

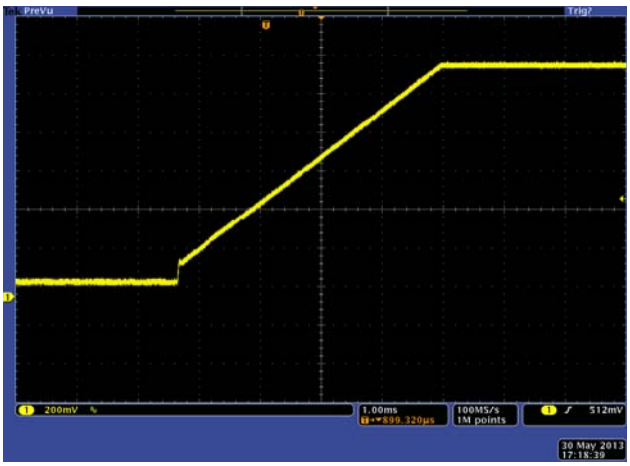


FIGURE 12. RAMP UP

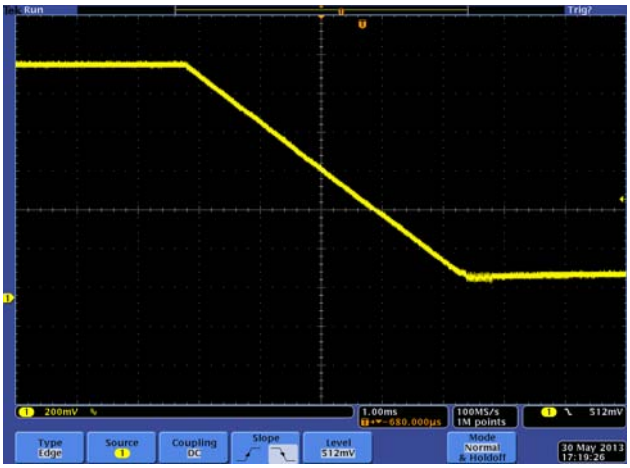


FIGURE 13. RAMP DOWN

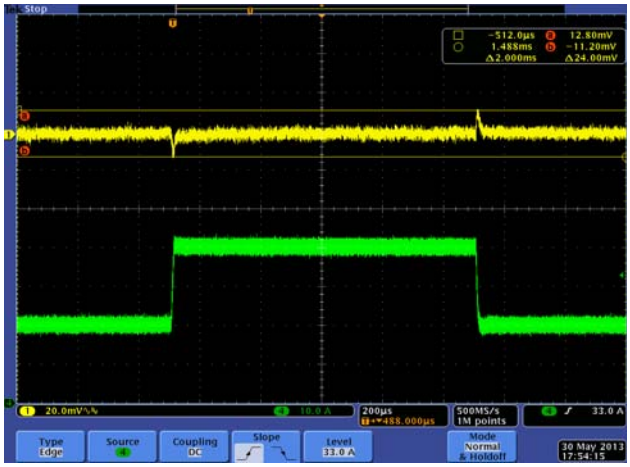


FIGURE 14. STEP RESPONSE, 20A TO 40A AT 5A/µs, ASCR = 1200
TOTAL DEVIATION WINDOW 25mV = 2.5%

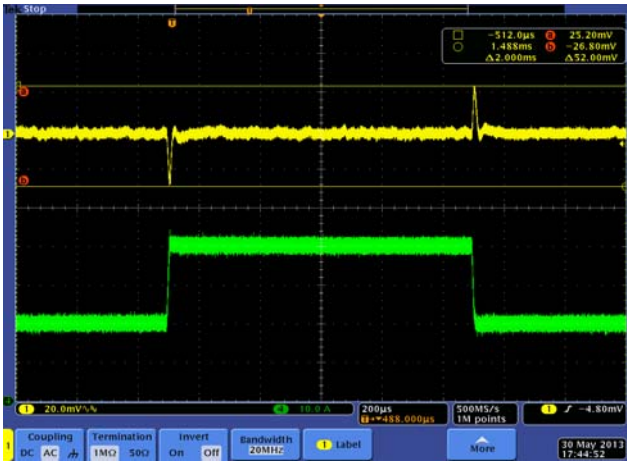


FIGURE 15. STEP RESPONSE, 20A TO 40A AT 5A/µs, ASCR = 400
TOTAL DEVIATION WINDOW 50mV = 5%

ZL8801-2PH-DEM01Z Board Layout

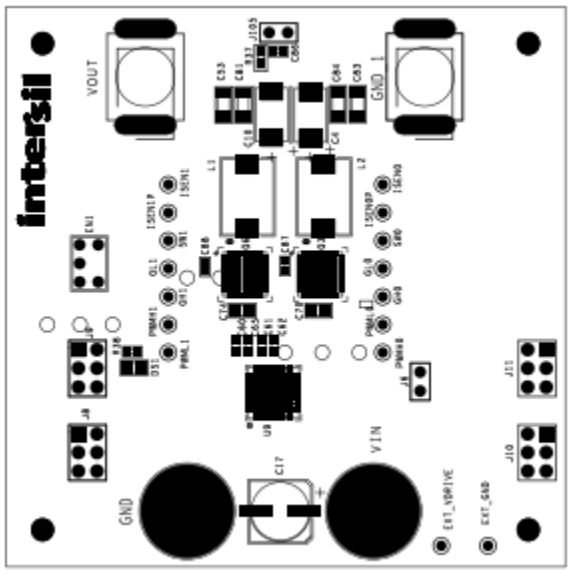


FIGURE 16. PCB - TOP ASSEMBLY

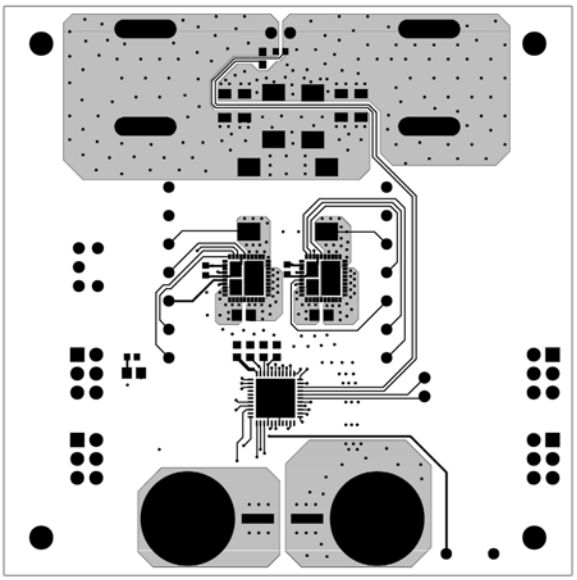


FIGURE 17. PCB - TOP LAYER

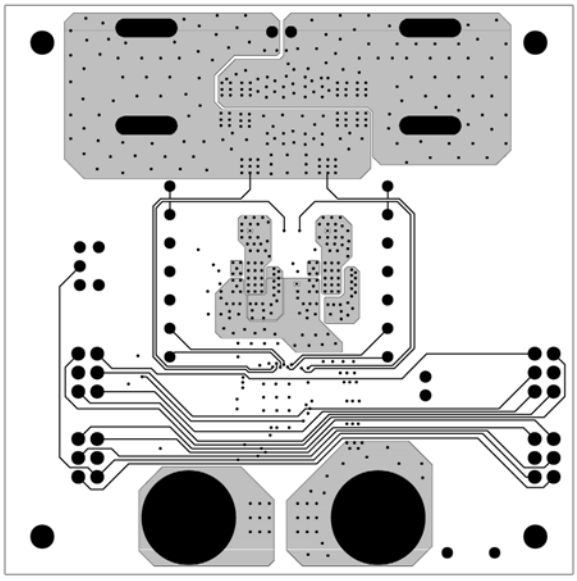


FIGURE 18. PCB - INNER LAYER 1 (TOP VIEW)

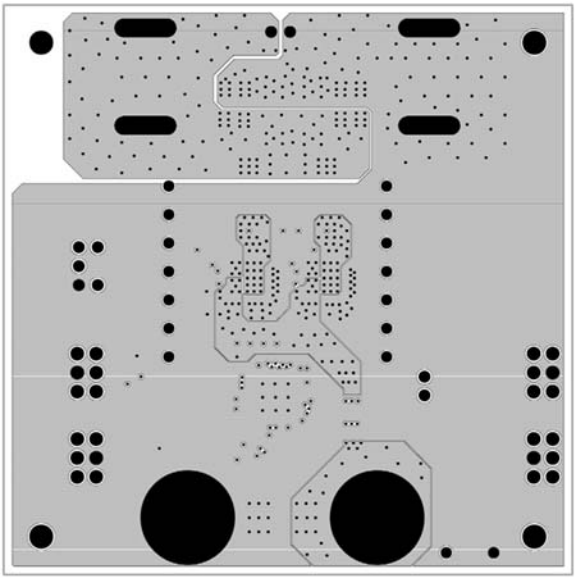


FIGURE 19. PCB - INNER LAYER 2 (TOP VIEW)

ZL8801-2PH-DEMO1Z Board Layout (Continued)

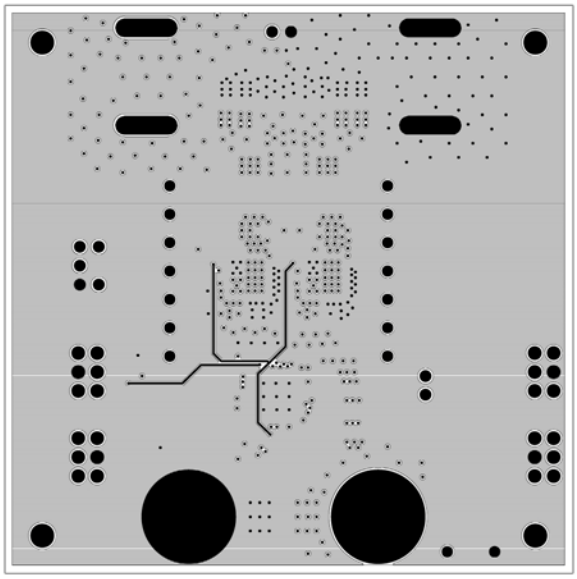


FIGURE 20. PCB - INNER LAYER 3 (TOP VIEW)

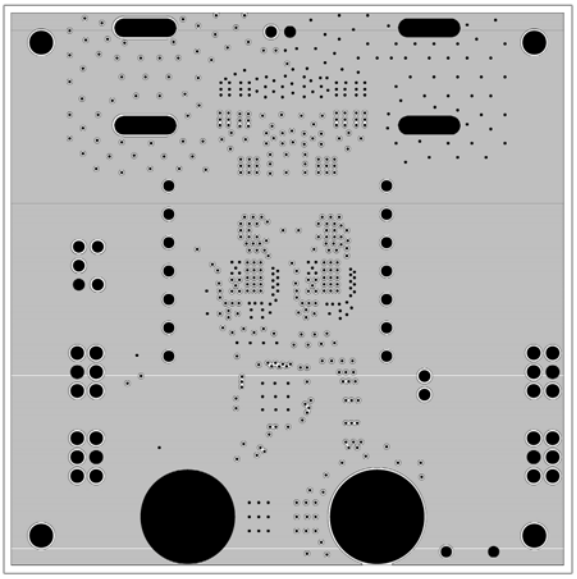


FIGURE 21. PCB - INNER LAYER 4 (TOP VIEW)

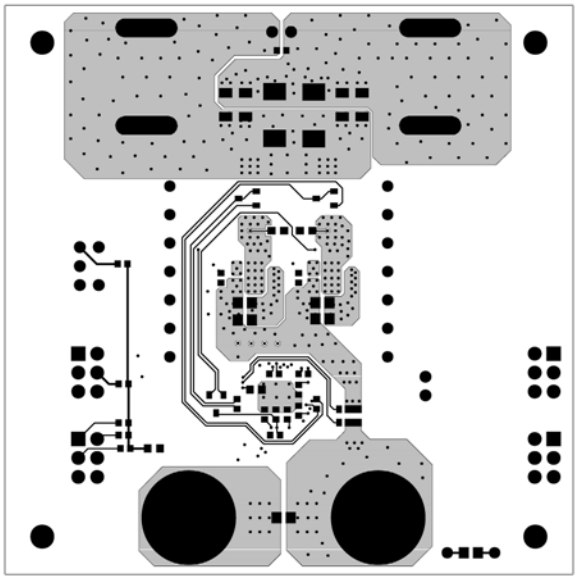


FIGURE 22. PCB - BOTTOM LAYER (TOP VIEW)

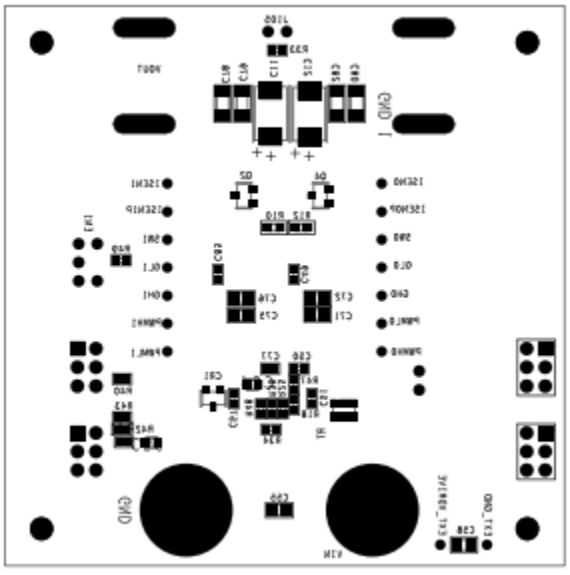


FIGURE 23. PCB - BOTTOM ASSEMBLY (TOP VIEW)