

FEATURES

- **50MHz Gain Bandwidth**
- **800V/μs Slew Rate**
- **5mA Maximum Supply Current**
- **9nV/√Hz Input Noise Voltage**
- **Unity-Gain Stable**
- **C-Load™ Op Amp Drives All Capacitive Loads**
- **1mV Maximum Input Offset Voltage**
- **1μA Maximum Input Bias Current**
- **250nA Maximum Input Offset Current**
- **±13V Minimum Output Swing into 500Ω**
- **±3.2V Minimum Output Swing into 150Ω**
- **4.5V/mV Minimum DC Gain, $R_L=1k$**
- **60ns Settling Time to 0.1%, 10V Step**
- **0.2% Differential Gain, $A_V=2$, $R_L=150\Omega$**
- **0.3° Differential Phase, $A_V=2$, $R_L=150\Omega$**
- **Specified at ±2.5V, ±5V, and ±15V**

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

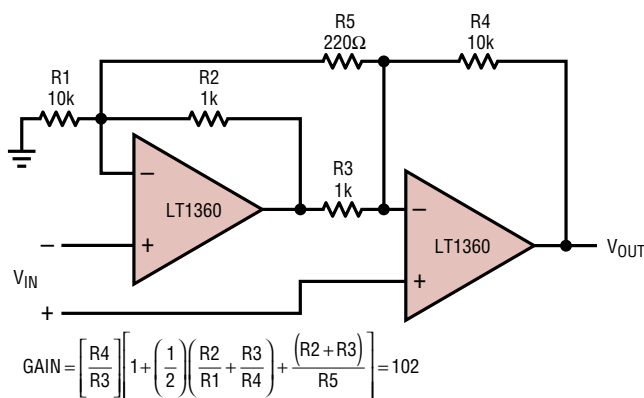
The LT1360 is a high speed, very high slew rate operational amplifier with excellent DC performance. The LT1360 features reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier. The amplifier is a single gain stage with outstanding settling characteristics which makes the circuit an ideal choice for data acquisition systems. The output drives a 500Ω load to ±13V with ±15V supplies and a 150Ω load to ±3.2V on ±5V supplies. The amplifier is also capable of driving any capacitive load which makes it useful in buffer or cable driver applications.

The LT1360 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For dual and quad amplifier versions of the LT1360 see the LT1361/LT1362 data sheet. For 70MHz amplifiers with 6mA of supply current per amplifier see the LT1363 and LT1364/LT1365 data sheets. For lower supply current amplifiers with bandwidths of 12MHz and 25MHz see the LT1354 through LT1359 data sheets. Singles, duals and quads of each amplifier are available.

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C-Load is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

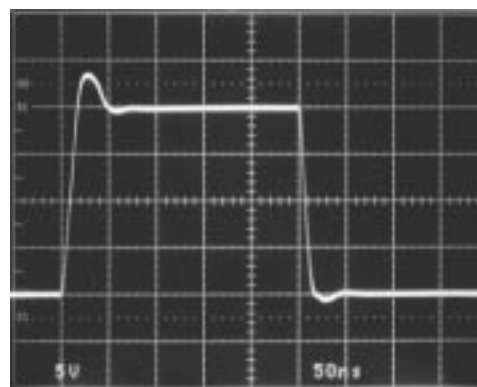
Two Op Amp Instrumentation Amplifier



TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 500kHz

1360 TAO1

$A_V = -1$ Large-Signal Response



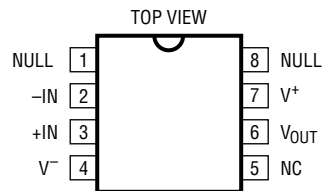
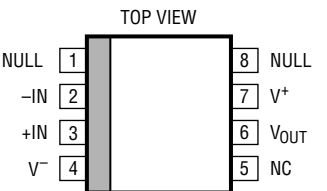
1360 TAO2

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 36V
 Differential Input Voltage
 (Transient Only) (Note 2) $\pm 10V$
 Input Voltage $\pm V_S$
 Output Short Circuit Duration (Note 3) Indefinite

Operating Temperature Range (Note 8) ... -40°C to 85°C
 Specified Temperature Range (Note 9) -40°C to 85°C
 Maximum Junction Temperature (See Below)
 Plastic Package 150°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p>  <p>N8 PACKAGE, 8-LEAD PDIP</p> <p>$T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 130^{\circ}\text{C/W}$</p>	<p>ORDER PART NUMBER</p> <p>LT1360CN8</p>	<p>TOP VIEW</p>  <p>S8 PACKAGE, 8-LEAD PLASTIC SO</p> <p>$T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 190^{\circ}\text{C/W}$</p>	<p>ORDER PART NUMBER</p> <p>LT1360CS8</p> <p>S8 PART MARKING</p> <p>1360</p>
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Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	$\pm 15V$		0.3	1.0	mV
			$\pm 5V$		0.3	1.0	mV
			$\pm 2.5V$		0.4	1.2	mV
I_{OS}	Input Offset Current		$\pm 2.5V$ to $\pm 15V$		80	250	nA
I_B	Input Bias Current		$\pm 2.5V$ to $\pm 15V$		0.3	1.0	μA
e_n	Input Noise Voltage	$f = 10\text{kHz}$	$\pm 2.5V$ to $\pm 15V$		9		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current	$f = 10\text{kHz}$	$\pm 2.5V$ to $\pm 15V$		0.9		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{CM} = \pm 12V$	$\pm 15V$	20	50		$\text{M}\Omega$
	Input Resistance	Differential	$\pm 15V$		5		$\text{M}\Omega$
C_{IN}	Input Capacitance		$\pm 15V$		3		pF
	Input Voltage Range $^+$		$\pm 15V$	12.0	13.4		V
			$\pm 5V$	2.5	3.4		V
			$\pm 2.5V$	0.5	1.1		V
	Input Voltage Range $^-$		$\pm 15V$	-13.2	-12.0		V
			$\pm 5V$	-3.2	-2.5		V
			$\pm 2.5V$	-0.9	-0.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12V$	$\pm 15V$	86	92		dB
		$V_{CM} = \pm 2.5V$	$\pm 5V$	79	84		dB
		$V_{CM} = \pm 0.5V$	$\pm 2.5V$	68	74		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 15V$		93	105		dB

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V _{SUPPLY}	MIN	TYP	MAX	UNITS
A _{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 1\text{k}$	$\pm 15\text{V}$	4.5	9.0		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 500\Omega$	$\pm 15\text{V}$	3.0	6.5		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 500\Omega$	$\pm 5\text{V}$	3.0	6.4		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 150\Omega$	$\pm 5\text{V}$	1.5	4.2		V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 500\Omega$	$\pm 2.5\text{V}$	2.5	5.2		V/mV
V _{OUT}	Output Swing	$R_L = 1\text{k}$, $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	13.5	13.9		$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	13.0	13.6		$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	3.5	4.0		$\pm\text{V}$
		$R_L = 150\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	3.2	3.8		$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 2.5\text{V}$	1.3	1.7		$\pm\text{V}$
I _{OUT}	Output Current	$V_{OUT} = \pm 13\text{V}$	$\pm 15\text{V}$	26	34		mA
		$V_{OUT} = \pm 3.2\text{V}$	$\pm 5\text{V}$	21	29		mA
I _{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	40	54		mA
SR	Slew Rate	$A_V = -2$, (Note 5)	$\pm 15\text{V}$	600	800		V/ μs
			$\pm 5\text{V}$	250	350		V/ μs
	Full Power Bandwidth	10V Peak, (Note 6) 3V Peak, (Note 6)	$\pm 15\text{V}$		12.7		MHz
			$\pm 5\text{V}$		18.6		MHz
GBW	Gain Bandwidth	$f = 1\text{MHz}$	$\pm 15\text{V}$		50		MHz
			$\pm 5\text{V}$		37		MHz
			$\pm 2.5\text{V}$		32		MHz
t _r , t _f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	$\pm 15\text{V}$		3.1		ns
			$\pm 5\text{V}$		4.3		ns
	Overshoot	$A_V = 1$, 0.1V	$\pm 15\text{V}$		35		%
			$\pm 5\text{V}$		27		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT} , 0.1V	$\pm 15\text{V}$		5.2		ns
			$\pm 5\text{V}$		6.4		ns
t _s	Settling Time	10V Step, 0.1%, $A_V = -1$	$\pm 15\text{V}$		60		ns
		10V Step, 0.01%, $A_V = -1$	$\pm 15\text{V}$		90		ns
		5V Step, 0.1%, $A_V = -1$	$\pm 5\text{V}$		65		ns
	Differential Gain	$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 150\Omega$	$\pm 15\text{V}$		0.20		%
			$\pm 5\text{V}$		0.20		%
		$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 1\text{k}$	$\pm 15\text{V}$		0.04		%
			$\pm 5\text{V}$		0.02		%
	Differential Phase	$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 150\Omega$	$\pm 15\text{V}$		0.40		Deg
			$\pm 5\text{V}$		0.30		Deg
		$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 1\text{k}$	$\pm 15\text{V}$		0.07		Deg
			$\pm 5\text{V}$		0.26		Deg
R _O	Output Resistance	$A_V = 1$, $f = 1\text{MHz}$	$\pm 15\text{V}$		1.4		Ω
I _S	Supply Current		$\pm 15\text{V}$		4.0	5.0	mA
			$\pm 5\text{V}$		3.8	4.8	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	$\pm 15\text{V}$	●			1.5	mV
			$\pm 5\text{V}$	●			1.5	mV
			$\pm 2.5\text{V}$	●			1.7	mV
	Input V_{OS} Drift	(Note 7)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		9	12	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●			350	nA
I_B	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●			1.5	μA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	●	84			dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	77			dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	●	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		●	91			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 1\text{k}$	$\pm 15\text{V}$	●	3.6			V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 500\Omega$	$\pm 15\text{V}$	●	2.4			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 500\Omega$	$\pm 5\text{V}$	●	2.4			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 150\Omega$	$\pm 5\text{V}$	●	1.0			V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 500\Omega$	$\pm 2.5\text{V}$	●	2.0			V/mV
				●				
V_{OUT}	Output Swing	$R_L = 1\text{k}$, $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	13.4			$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	12.8			$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	3.4			$\pm\text{V}$
		$R_L = 150\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	3.1			$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 2.5\text{V}$	●	1.2			$\pm\text{V}$
				●				
I_{OUT}	Output Current	$V_{OUT} = \pm 12.8\text{V}$	$\pm 15\text{V}$	●	25			mA
		$V_{OUT} = \pm 3.1\text{V}$	$\pm 5\text{V}$	●	20			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	●	32			mA
SR	Slew Rate	$A_V = -2$, (Note 5)	$\pm 15\text{V}$	●	475			V/ μs
			$\pm 5\text{V}$	●	185			V/ μs
I_S	Supply Current		$\pm 15\text{V}$	●			5.8	mA
			$\pm 5\text{V}$	●			5.6	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	$\pm 15\text{V}$	●			2.0	mV
			$\pm 5\text{V}$	●			2.0	mV
			$\pm 2.5\text{V}$	●			2.2	mV
	Input V_{OS} Drift	(Note 7)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		9	12	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●			400	nA
I_B	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●			1.8	μA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	●	84			dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	77			dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	●	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 1\text{k}$	$\pm 15\text{V}$	●	2.5			V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 500\Omega$	$\pm 15\text{V}$	●	1.5			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 500\Omega$	$\pm 5\text{V}$	●	1.5			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 150\Omega$	$\pm 5\text{V}$	●	0.6			V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 500\Omega$	$\pm 2.5\text{V}$	●	1.3			V/mV
V_{OUT}	Output Swing	$R_L = 1\text{k}\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	13.4			$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	12.0			$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	3.4			$\pm\text{V}$
		$R_L = 150\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	3.0			$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 2.5\text{V}$	●	1.2			$\pm\text{V}$
I_{OUT}	Output Current	$V_{OUT} = \pm 12.0\text{V}$	$\pm 15\text{V}$	●	24			mA
		$V_{OUT} = \pm 3.0\text{V}$	$\pm 5\text{V}$	●	20			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	●	30			mA
SR	Slew Rate	$A_V = -2$, (Note 5)	$\pm 15\text{V}$	●	450			V/ μs
			$\pm 5\text{V}$	●	175			V/ μs
I_S	Supply Current		$\pm 15\text{V}$	●			6.0	mA
			$\pm 5\text{V}$	●			5.8	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Differential inputs of $\pm 10\text{V}$ are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 5: Slew rate is measured between $\pm 10\text{V}$ on the output with $\pm 6\text{V}$ input for $\pm 15\text{V}$ supplies and $\pm 2\text{V}$ on the output with $\pm 1.75\text{V}$ input for $\pm 5\text{V}$ supplies.

Note 6: Full power bandwidth is calculated from the slew rate measurement: $\text{FPBW} = \text{SR}/2\pi V_P$.

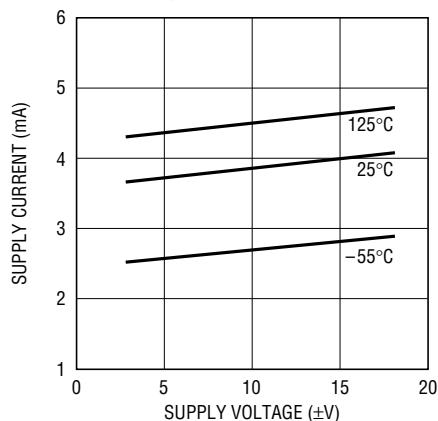
Note 7: This parameter is not 100% tested.

Note 8: The LT1360C is guaranteed functional over the operating temperature range of -40°C to 85°C .

Note 9: The LT1360C is guaranteed to meet specified performance from 0°C to 70°C . The LT1360C is designed, characterized and expected to meet specified performance from -40°C to 85°C , but is not tested or QA sampled at these temperatures. For guaranteed I-grade parts, consult the factory.

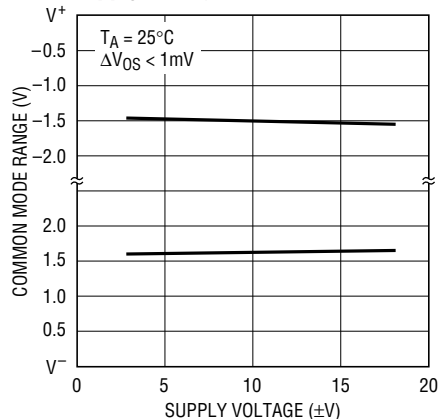
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage and Temperature



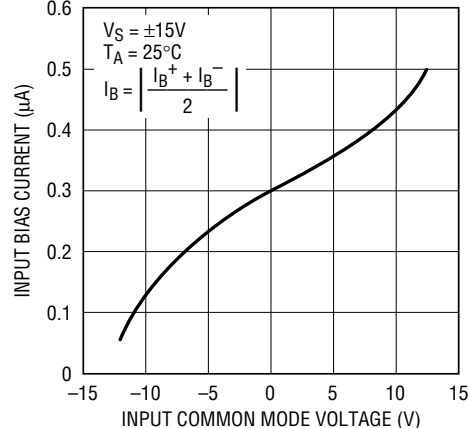
1360 G01

Input Common Mode Range vs Supply Voltage



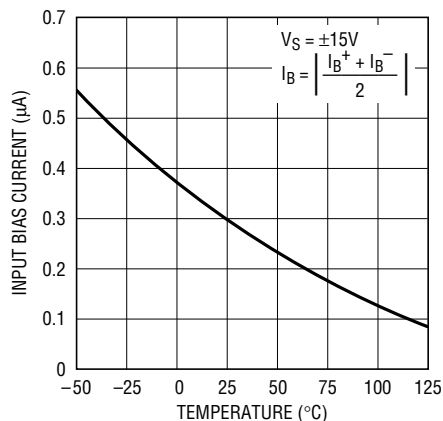
1360 G02

Input Bias Current vs Input Common Mode Voltage



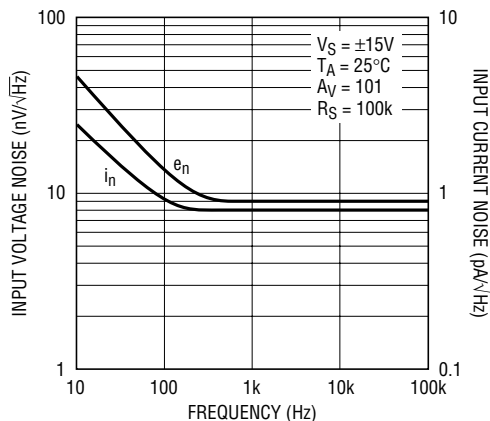
1360 G03

Input Bias Current vs Temperature



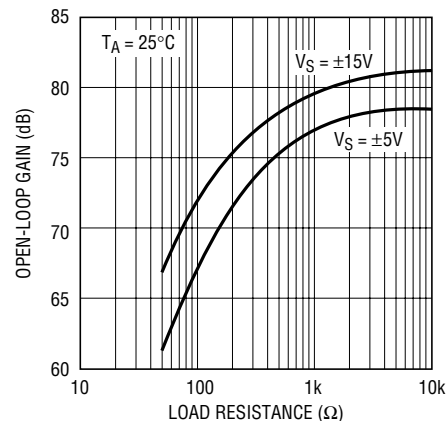
1360 G04

Input Noise Spectral Density



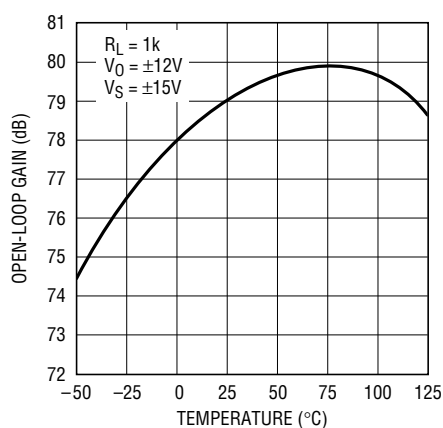
1360 G05

Open-Loop Gain vs Resistive Load



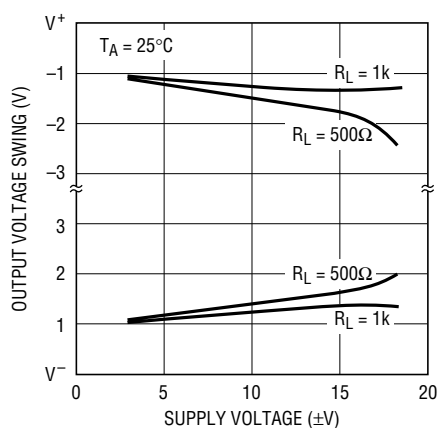
1360 G06

Open-Loop Gain vs Temperature



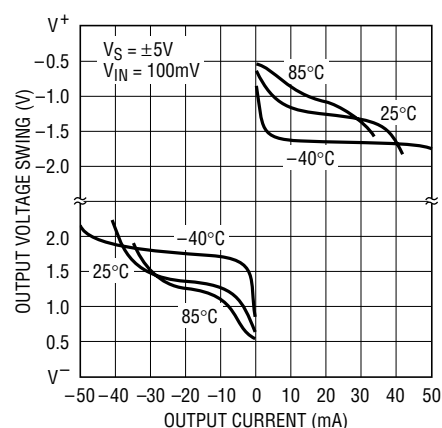
1360 G07

Output Voltage Swing vs Supply Voltage



1360 G08

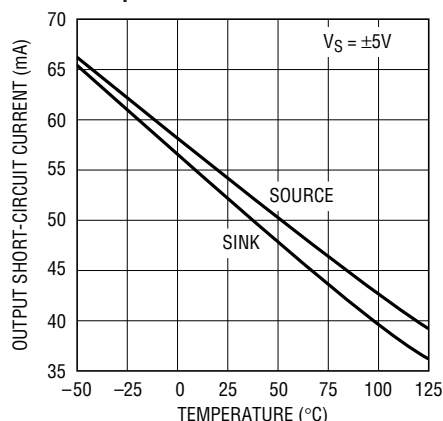
Output Voltage Swing vs Load Current



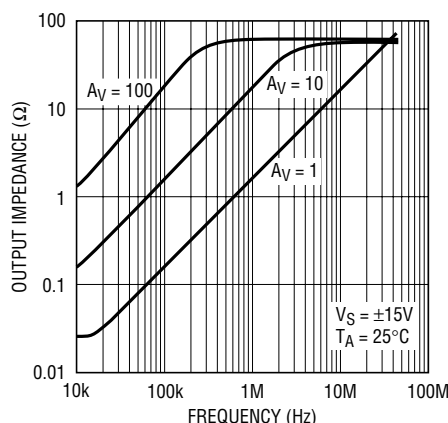
1360 G09

TYPICAL PERFORMANCE CHARACTERISTICS

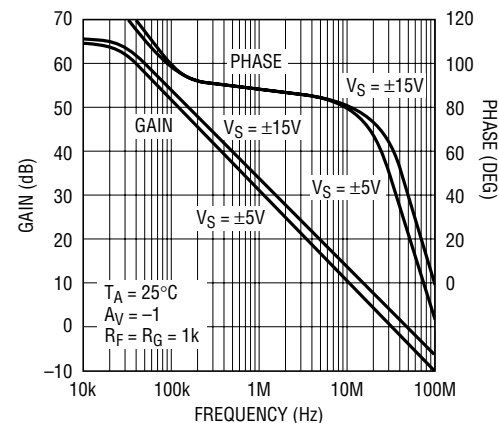
Output Short-Circuit Current vs Temperature



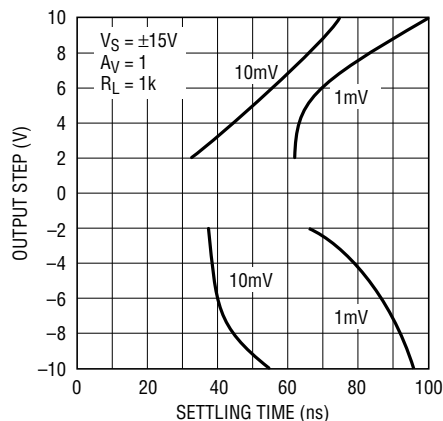
Output Impedance vs Frequency



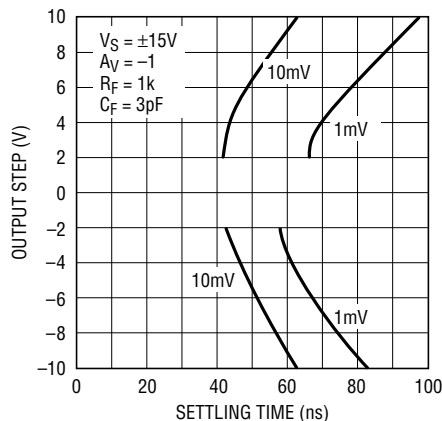
Gain and Phase vs Frequency



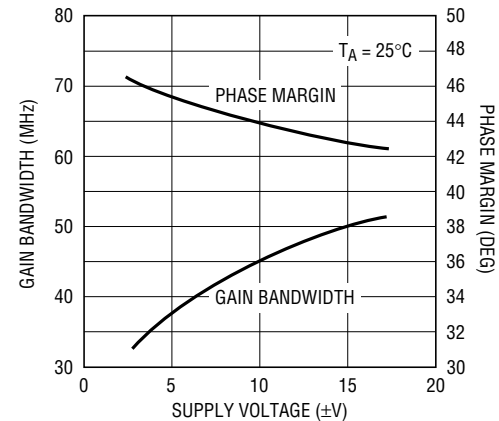
Settling Time vs Output Step (Noninverting)



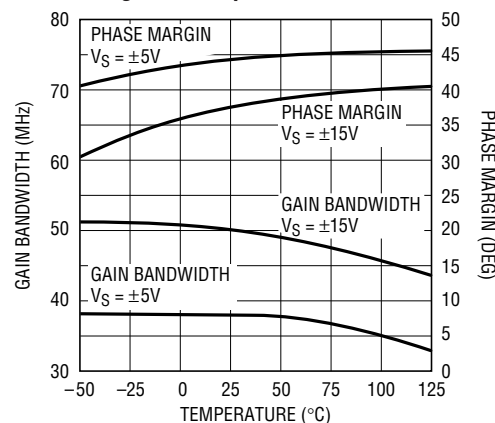
Settling Time vs Output Step (Inverting)



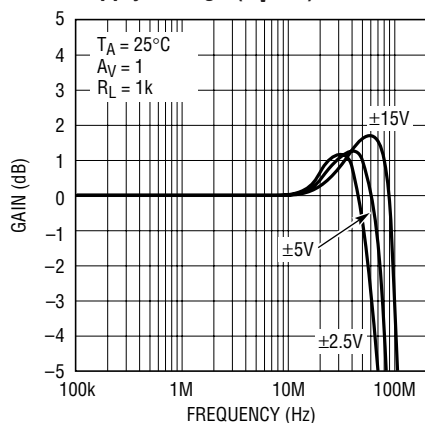
Gain Bandwidth and Phase Margin vs Supply Voltage



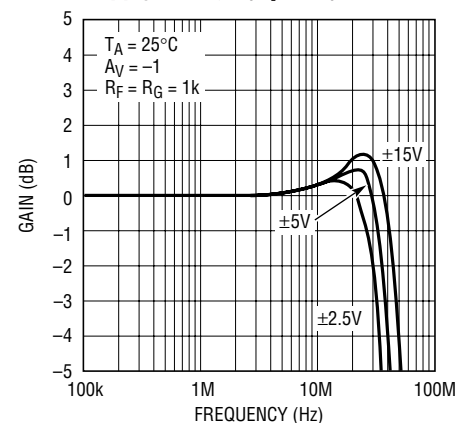
Gain Bandwidth and Phase Margin vs Temperature



Frequency Response vs Supply Voltage (A_V = 1)

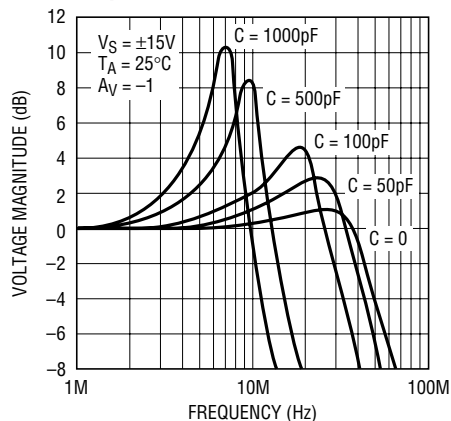


Frequency Response vs Supply Voltage (A_V = -1)



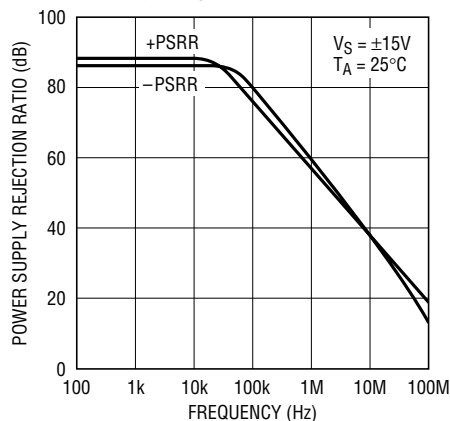
TYPICAL PERFORMANCE CHARACTERISTICS

Frequency Response vs Capacitive Load



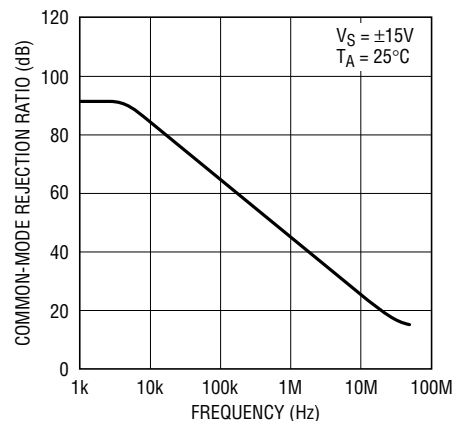
1360 G19

Power Supply Rejection Ratio vs Frequency



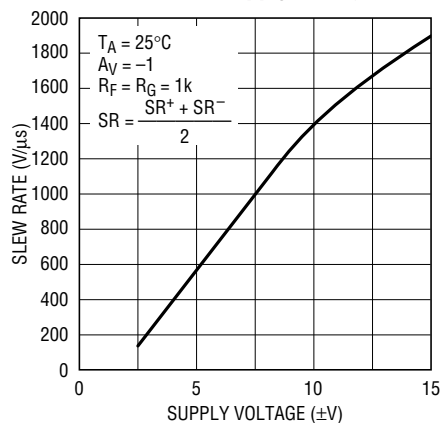
1360 G20

Common Mode Rejection Ratio vs Frequency



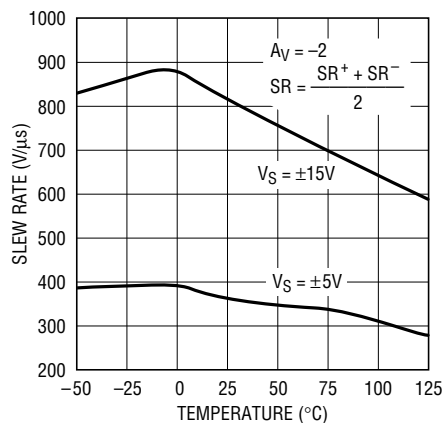
1360 G21

Slew Rate vs Supply Voltage



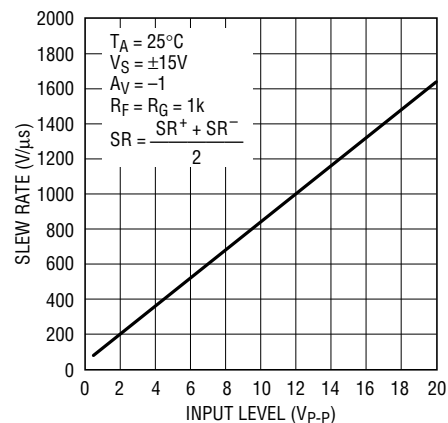
1360 G22

Slew Rate vs Temperature



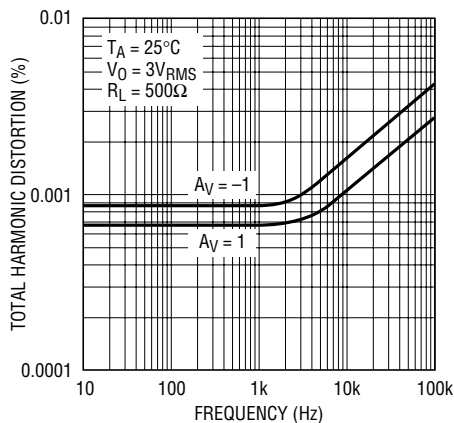
1360 G23

Slew Rate vs Input Level

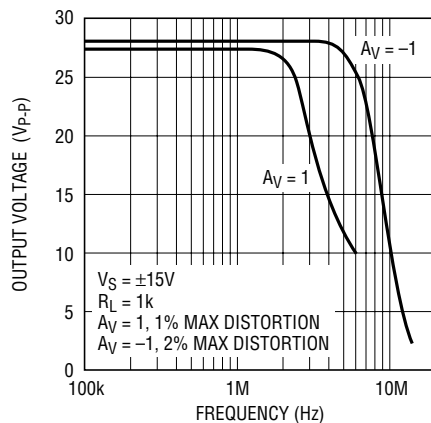


1360 G24

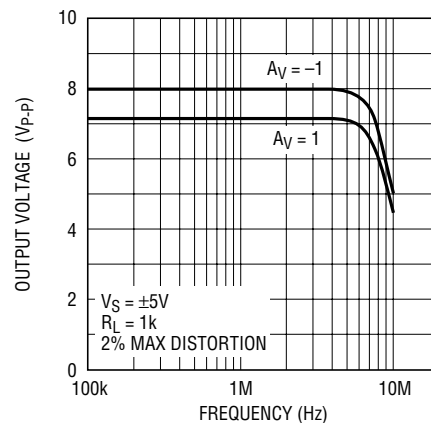
Total Harmonic Distortion vs Frequency



1360 G25

Undistorted Output Swing vs Frequency ($\pm 15V$)

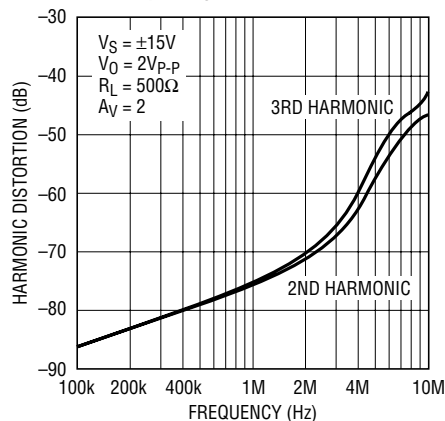
1360 G26

Undistorted Output Swing vs Frequency ($\pm 5V$)

1360 G27

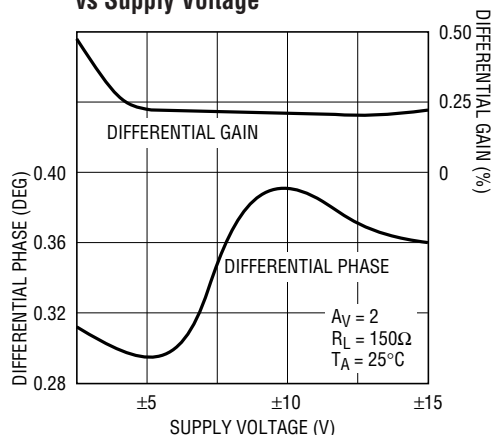
TYPICAL PERFORMANCE CHARACTERISTICS

2nd and 3rd Harmonic Distortion vs Frequency



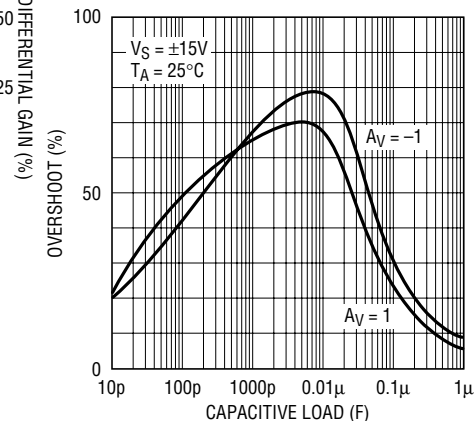
1360 G28

Differential Gain and Phase vs Supply Voltage



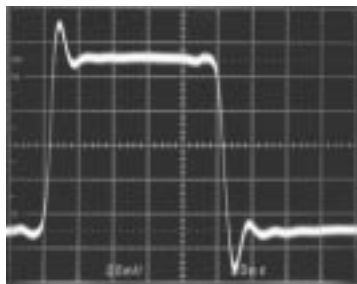
1360 G29

Capacitive Load Handling



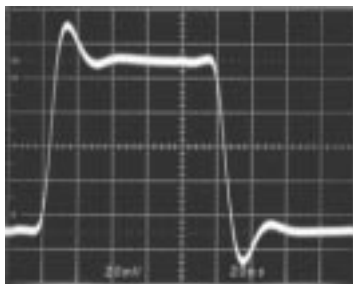
1360 G30

Small-Signal Transient ($A_V = 1$)



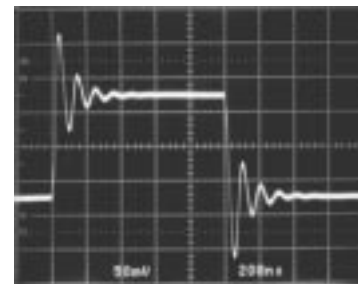
1360 TA31

Small-Signal Transient ($A_V = -1$)



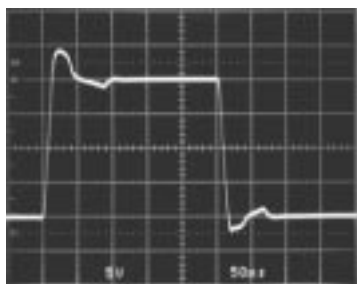
1360 TA32

Small-Signal Transient ($A_V = -1$, $C_L = 500pF$)



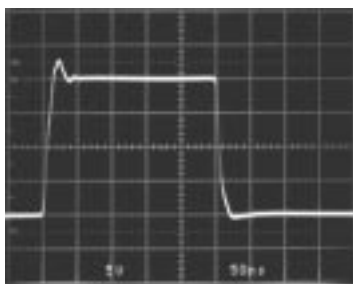
1360 TA33

Large-Signal Transient ($A_V = 1$)



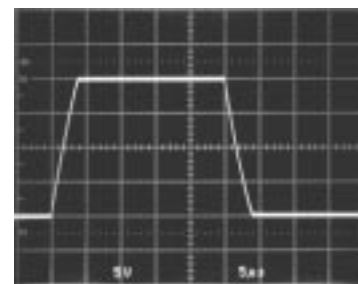
1360 TA34

Large-Signal Transient ($A_V = -1$)



1360 TA35

Large-Signal Transient ($A_V = 1$, $C_L = 10,000pF$)

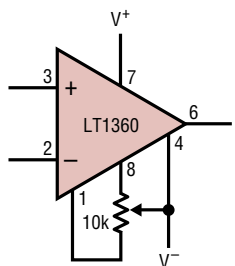


1360 TA36

APPLICATIONS INFORMATION

The LT1360 may be inserted directly into AD817, AD847, EL2020, EL2044, and LM6361 applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1360 is shown below.

Offset Nulling



1360 AI01

Layout and Passive Components

The LT1360 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01μF to 0.1μF). For high drive current applications use low ESR bypass capacitors (1μF to 10μF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or oscillations. For feedback resistors greater than 5kΩ, a parallel capacitor of value

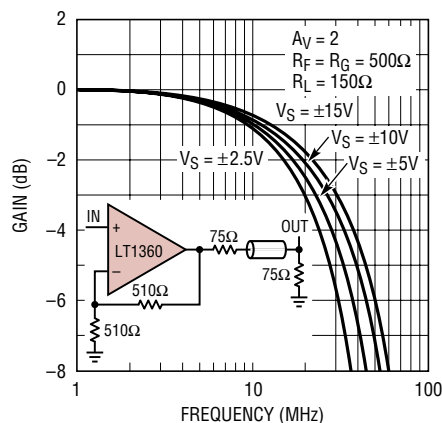
$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN} .

Capacitive Loading

The LT1360 is stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves. The photo of the small-signal response with 500pF load shows 60% peaking. The large-signal response with a 10,000pF load shows the output slew rate being limited to 5V/μs by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Cable Driver Frequency Response



1360 AI02

APPLICATIONS INFORMATION

Input Considerations

Each of the LT1360 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. **The part should not be used as a comparator, peak detector or other open-loop application with large, sustained differential inputs.** Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of the time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

Power Dissipation

The LT1360 combines high speed and large output drive in a small package. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

$$\text{LT1360CN8: } T_J = T_A + (P_D \times 130^\circ\text{C/W})$$

$$\text{LT1360CS8: } T_J = T_A + (P_D \times 190^\circ\text{C/W})$$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore $P_{D\text{MAX}}$ is:

$$P_{D\text{MAX}} = (V^+ - V^-)(I_{S\text{MAX}}) + (V^+/2)^2/R_L$$

Example: LT1360CS8 at 70°C , $V_S = \pm 15\text{V}$, $R_L = 250\Omega$

$$P_{D\text{MAX}} = (30\text{V})(5.8\text{mA}) + (7.5\text{V})^2/250\Omega = 399\text{mW}$$

$$T_{J\text{MAX}} = 70^\circ\text{C} + (399\text{mW})(190^\circ\text{C/W}) = 146^\circ\text{C}$$

APPLICATIONS INFORMATION

Circuit Operation

The LT1360 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R_1 , so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1360 is tested for slew rate in a gain of -2 so higher slew rates can be expected in gains of 1 and -1 , and lower slew rates in higher gain configurations.

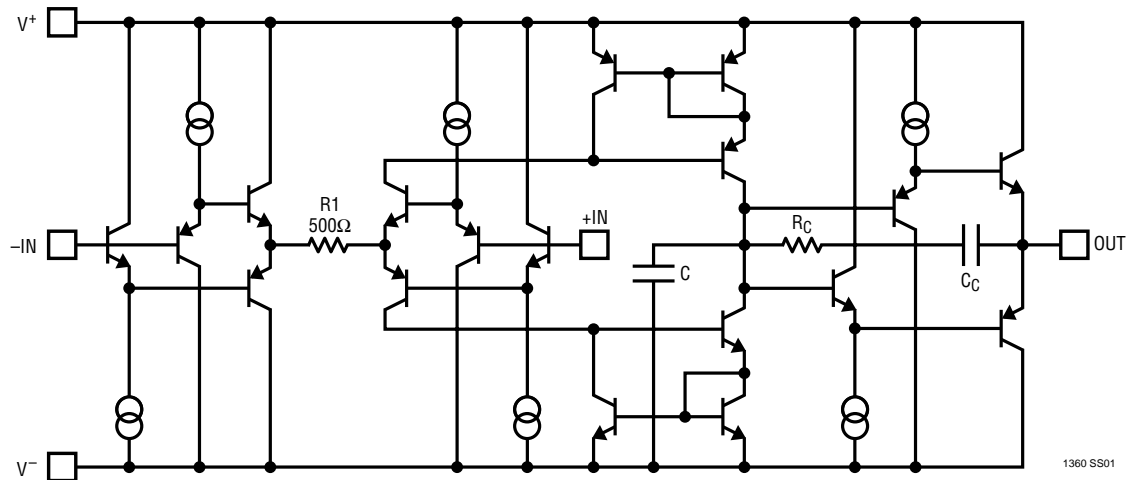
The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network

is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity-gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Comparison to Current Feedback Amplifiers

The LT1360 enjoys the high slew rates of Current Feedback Amplifiers (CFAs) while maintaining the characteristics of a true voltage feedback amplifier. The primary differences are that the LT1360 has two high impedance inputs and its closed loop bandwidth decreases as the gain increases. CFAs have a low impedance inverting input and maintain relatively constant bandwidth with increasing gain. The LT1360 can be used in all traditional op amp configurations including integrators and applications such as photodiode amplifiers and I-to-V converters where there may be significant capacitance on the inverting input. The frequency compensation is internal and not dependent on the value of the feedback resistor. For CFAs, the feedback resistance is fixed for a given bandwidth and capacitance on the inverting input can cause peaking or oscillations. The slew rate of the LT1360 in noninverting gain configurations is also superior in most cases.

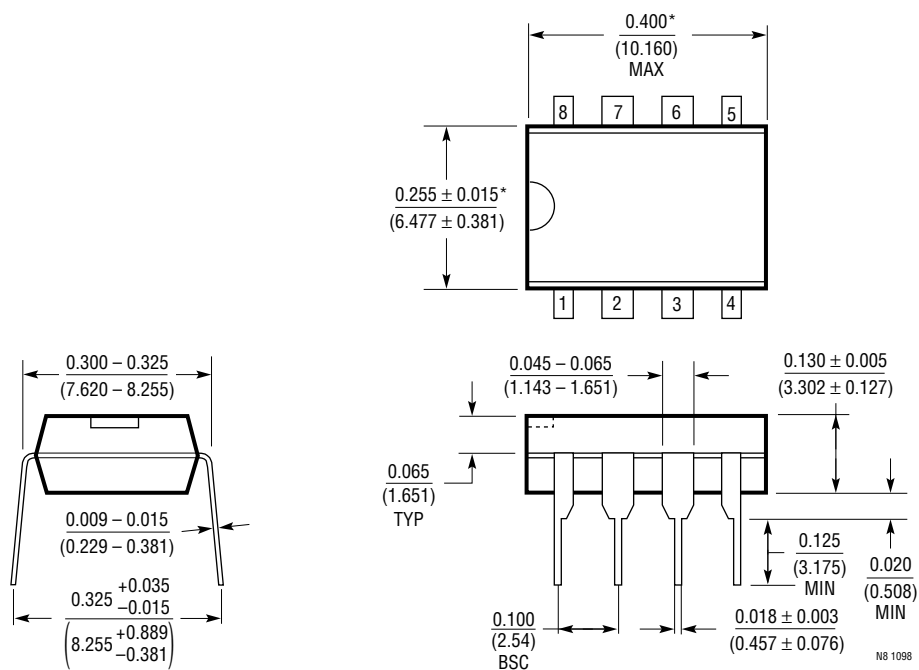
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
 (LTC DWG # 05-08-1510)

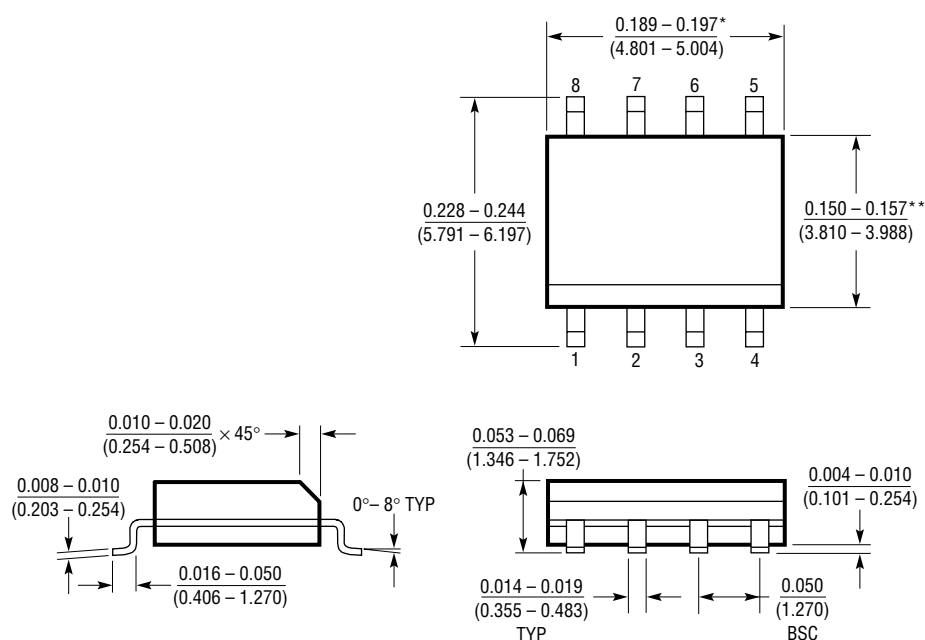


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 1298

The circuit diagram shows a two-stage active filter. The first stage is an inverting amplifier with a gain of -10. It uses an LT1360 op-amp with a feedback capacitor of 47 pF and a feedback resistor of 909 Ω. The input signal V_{IN} is connected to the inverting input through a 909 Ω resistor. The non-inverting input is connected to ground through a 220 pF capacitor. The output of the first stage is connected to the second stage through a 1.1 kΩ resistor. The second stage is a non-inverting amplifier with a gain of 1.1. It also uses an LT1360 op-amp with a feedback capacitor of 22 pF and a feedback resistor of 1.1 kΩ. The input to the second stage is connected to the non-inverting input through a 2.21 kΩ resistor. The output of the second stage is V_{OUT} . The op-amp is labeled LT1360.

PART NUMBER	DESCRIPTION	COMMENTS
LT1361/LT1362	Dual and Quad 50MHz, 800V/μs Op Amps	Dual and Quad Versions of LT1360
LT1363	70MHz, 1000V/μs Op Amp	Faster Version of LT1360, $V_{OS} = 1.5\text{mV}$, $I_S = 6.3\text{mA}$
LT1357	25MHz, 600V/μs Op Amp	Lower Power Version of LT1360, $V_{OS} = 0.6\text{mV}$, $I_S = 2\text{mA}$
LT1812	100MHz, 750V/μs Op Amp	Low Voltage, Low Power LT1360, $V_{OS} = 1\text{mV}$, $I_S = 3\text{mA}$