

Isolated Flyback Converter with Synchronous Rectification

DESCRIPTION

Demonstration circuit 1143 is a 20 Watt Isolated Flyback Converter with Synchronous Rectification and Primary-Side Regulation featuring the LT3825.

This circuit was designed to demonstrate the high levels of performance, efficiency, and small solution size attainable using this part in a flyback power supply. It operates at 250kHz and produces a regulated 3.3V, 6A output from an input voltage range of 36 to 72V: suitable for telecom and other applications. It has a footprint area that is 1.0 inch square. Synchronous rectifi-

cation helps to attain efficiency exceeding 88%. Isolation voltage is 1500VDC.

Design files for this circuit board are available. Call the LTC factory.

ΔT, LTC, LTM, LT, Burst Mode, OPTI-LOOP, Over-The-Top and PolyPhase are registered trademarks of Linear Technology Corporation. Adaptive Power, C-Load, DirectSense, Easy Drive, FilterCAD, Hot Swap, LinearView, μModule, Micropower SwitcherCAD, Multimode Dimming, No Latency ΔΣ, No Latency Delta-Sigma, No R_{SENSE}, Operational Filter, PanelProtect, PowerPath, PowerSOT, SmartStart, SoftSpan, Stage Shedding, SwitcherCAD, ThinSOT, UltraFast and VLDO are trademarks of Linear Technology Corporation. Other product names may be trademarks of the companies that manufacture the products.

PERFORMANCE SUMMARY Specifications are at TA = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IN}	Input Supply Range		36		72	V
V _{OUT}	Output Voltage			3.3		V
I _{OUT}	Output Current Range	V _{IN} = 36–72V	0		6	A
F _{SW}	Switching (Clock) Frequency			250		kHz
V _{OUT P-P}	Output Ripple	V _{IN} = 48V, I _{OUT} = 6A (20MHz BW)		20		mV _{P-P}
I _{REG}	Output Regulation	Line and Load (36–72V, 0–6A)		±1.2		%
P _{OUT/PIN}	Efficiency (see Figure 2)	V _{IN} = 48V, I _{OUT} = 6A		88.5		%

OPERATING PRINCIPLES

The LT3825 Synchronous Flyback PWM Controller is used on the primary and drives a secondary-side MOSFET through a pulse transformer to provide a synchronous rectified output.

When an input voltage is applied, an undervoltage circuit keeps the LT3825 in its quiescent state while a resistor charges C_{vcc} (C10) to 15V. The controller is then enabled, and start-up commences. The primary circuit operates from the charge stored in C_{vcc} until the housekeeping winding of T1 starts to support V_{cc}. When a heavy overload or short-circuit prevents T1

supporting V_{cc}, the converter operates in 'burp-mode', cutting off when V_{cc} declines to 10V, maintaining low power dissipation in the circuit. The LT3825 provides a synchronous rectifier gate drive signal which is passed to the secondary through T2 and subsequently buffered.

Regulation is attained by observing the voltage on the housekeeping winding of T1 during the Flyback time, and Pulse Width Modulating (PWM) the Primary Gate drive (PG) and Synchronous Gate drive (SG). The

LT3825 is programmed to compensate for circuit resistance that is outside of the control loop.

Optional LC filter stages on the input and output facilitate low noise.

QUICK START PROCEDURE

Demonstration circuit 1143 is easy to set up to evaluate the performance of the LT3825. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

NOTE. When measuring the output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the output voltage ripple by touching the probe tip and ground ring directly across the last output capacitor (C29) as shown in Figure 1.

1. Set an input power supply that is capable of 36V to 72V to 48V. Then turn off the supply.
2. With power off, connect the supply to the input terminals +Vin and –Vin.
 - a. Input voltages lower than 36V can keep the converter from turning on due to the undervoltage lockout feature of the LT3825.
 - b. If efficiency measurements are desired, an ammeter capable of measuring 1Adc or a resistor shunt can be put in series with the input supply in order to measure the DC1143A's input current.
 - c. A voltmeter with a capability of measuring at least 72V can be placed across the input terminals in order to get an accurate input voltage measurement.
3. Turn on the power at the input.

NOTE. Make sure that the input voltage never exceeds 72V.

4. Check for the proper output voltage of 3.3V. Turn off the power at the input.
5. Once the proper output voltages are established, connect a variable load capable of sinking 6A at 3.3V to the output terminals +Vout and –Vout. Set the current for 0A.
 - a. If efficiency measurements are desired, an ammeter or a resistor shunt that is capable of handling 6Adc can be put in series with the output load in order to measure the DC1143A's output current.
 - b. A voltmeter with a capability of measuring at least 3.3V can be placed across the output terminals in order to get an accurate output voltage measurement.
6. Turn on the power at the input.

NOTE. If there is no output, temporarily disconnect the load to make sure that the load is not set too high.
7. Once the proper output voltage is again established, adjust the load within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other desired parameters.

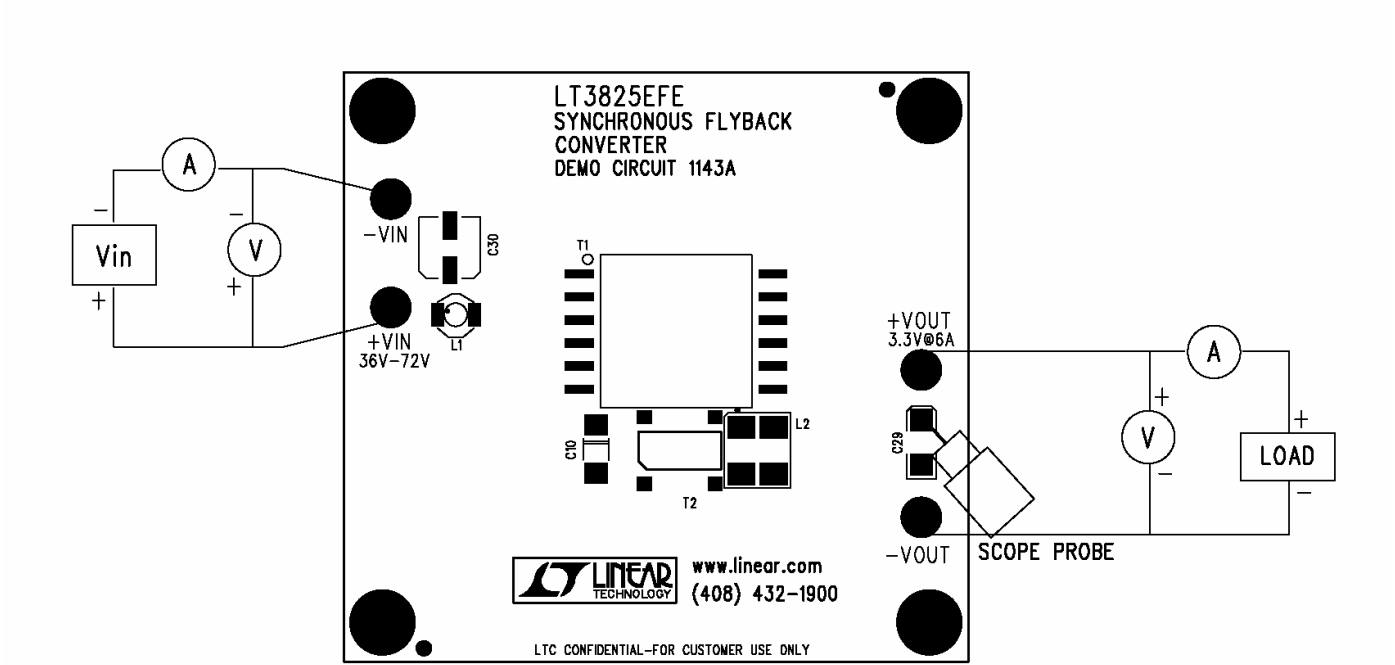


Figure 1. Proper Measurement Equipment Setup

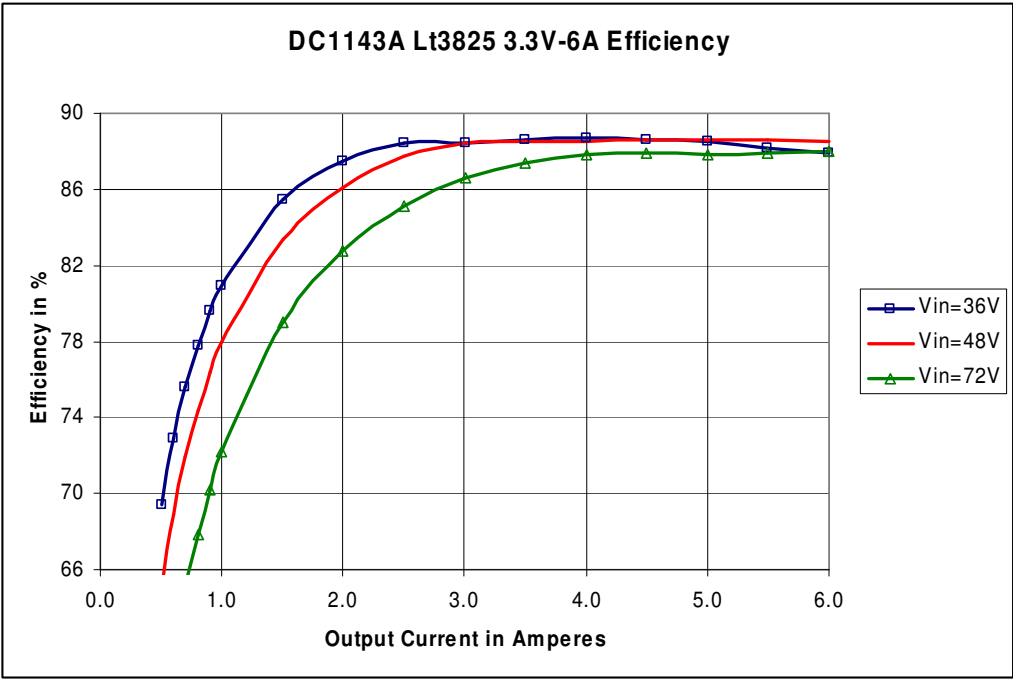


Figure 2. Efficiency – Note 88% efficiency over a wide current range.

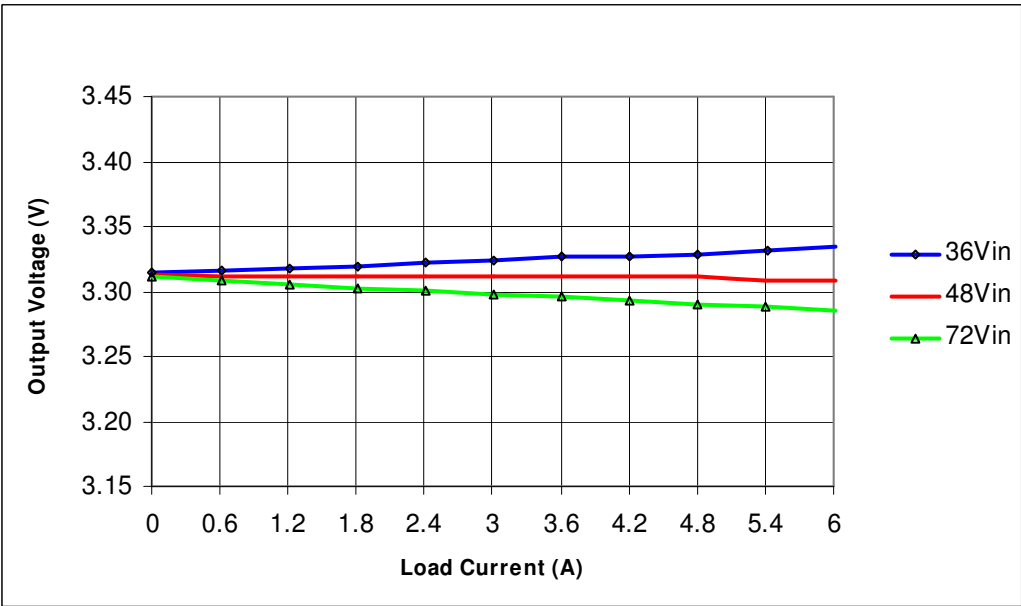


Figure 3. Regulation – Note regulation band of 1.5%

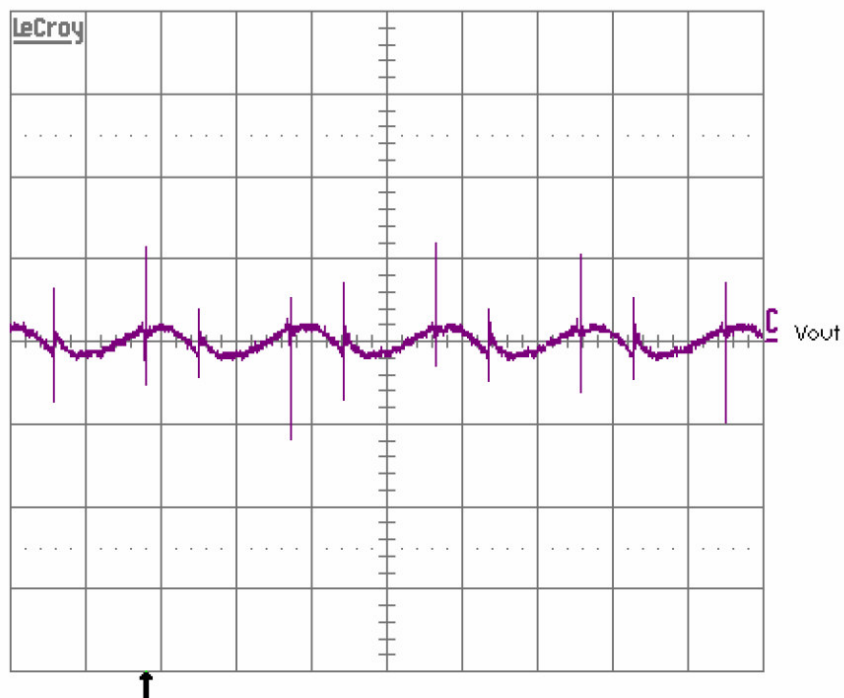


Figure 4. Output Ripple at 48Vin and 6Aout (20MHz) - 2uS and 20mV / div

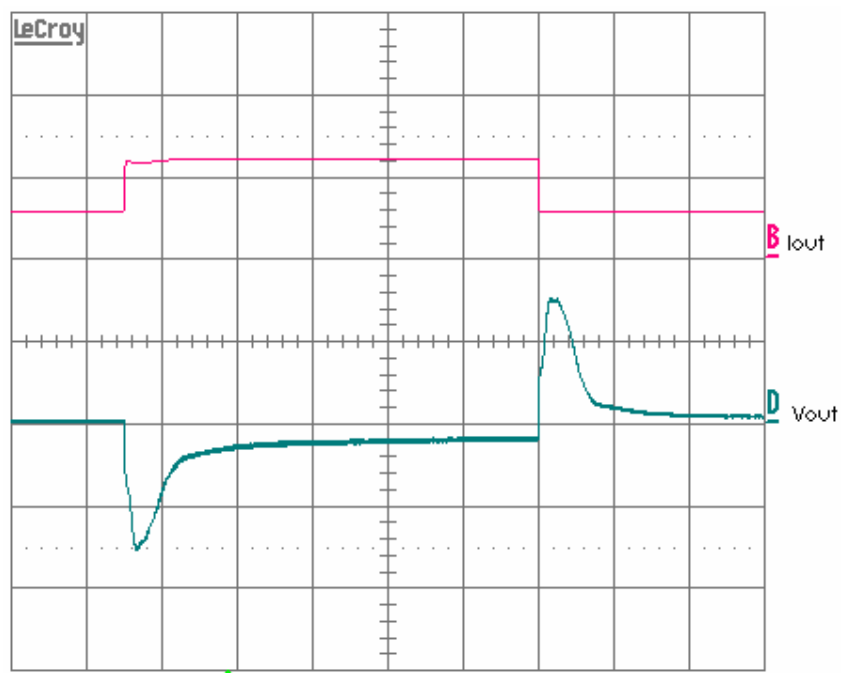
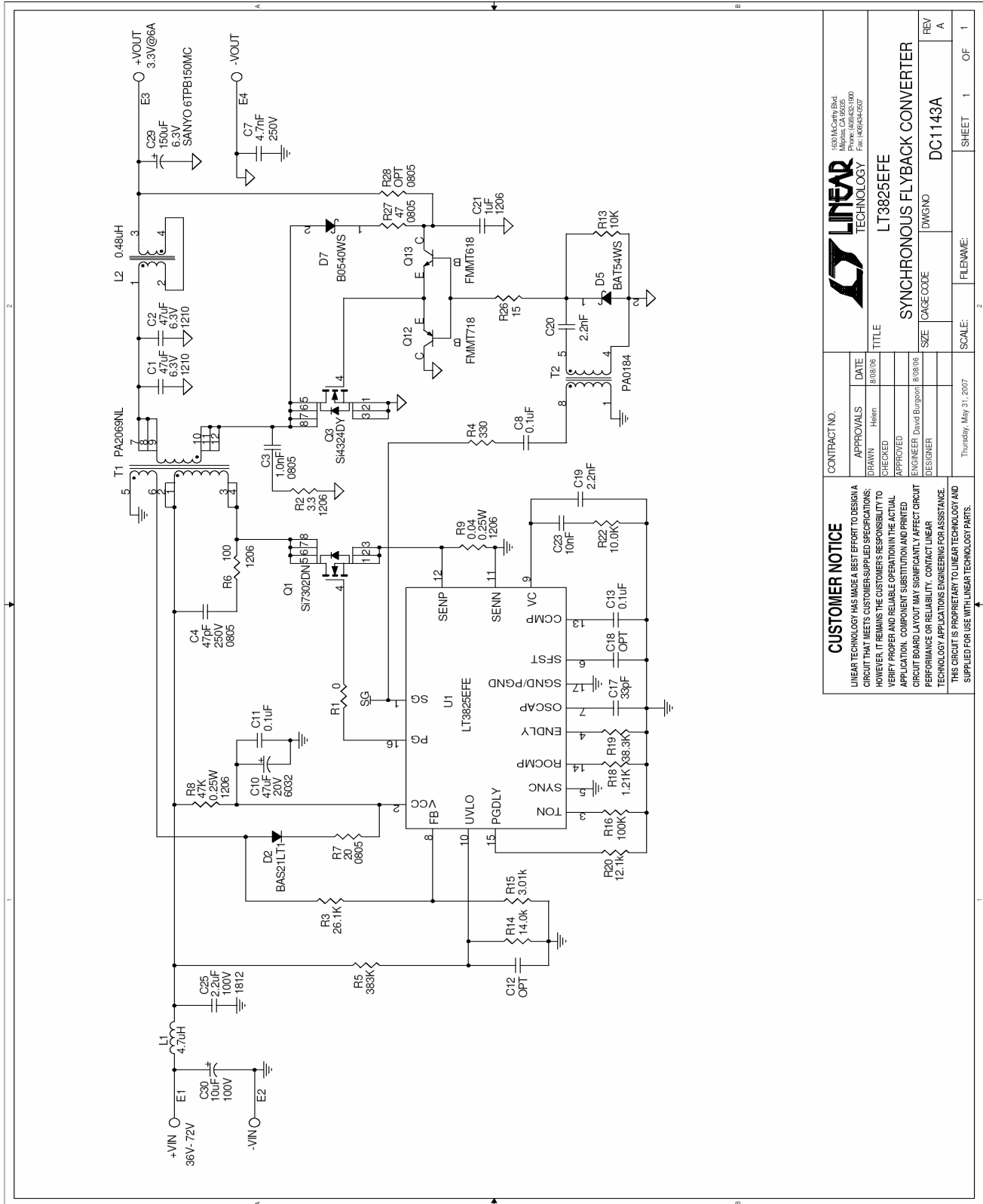


Figure 5. Transient Response Waveform at 48Vin and 5 - 6Aout – 200uS, 5A, and 200mV / div



CUSTOMER NOTICE LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS. HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.		CONTRACT NO.		APPROVALS		DATE	
				DRAWN: Helen		8/08/06	
				CHECKED:			
				APPROVED:			
				ENGINEER: David Burgess		8/08/06	
				DESIGNER:			
				Thursday, May 31, 2007			
				SCALE: 1		SHEET 1 OF 1	
				FLEWING:			
				SIZE: CAGE CODE		DWGNO: DC1143A	
				REV: A			