Dust Networks

Eterna® Evaluation & Development Board Set User Guide

For use with the following evaluation and development kits:

DC2274A-A, DC9000A, DC9000B, DC9001A, DC9001B, DC9003A, DC9004A, DC9006A, DC9007A, DC9011A, DC9018A, DC9018B, DC9020A, DC9020B, DC9021A and DC9022A.

Table of Contents

About This Guide

This document describes the use of the Eterna Evaluation & Development board set.

Audience

This document is intended for system developers, hardware designers, and software developers.

Related Documents

The following related documents are available:

DC9000A SmartMesh IP™ Starter Kit
DC9003A Eterna Evaluation & Development Board Design Data
DC9006A Interface Board Design Data
DC9007A SmartMesh™ WirelessHART Starter Kit
DC9021A SmartMesh IP RF Certified Starter Kit
DC9022A SmartMesh WirelessHART RF Certified Starter Kit
DC2274A-A SmartMesh IP SmartMesh IP USB Manager Kit
SmartMesh IP Easy Start Guide
SmartMesh WirelessHART Easy Start Guide
SmartMesh WirelessHART User Guide
LTC5800-IPM SmartMesh IP Mote Datasheet
LTC5800-IPR SmartMesh IP Manager Datasheet
LTC5800-WHM SmartMesh WirelessHART Mote Datasheet
LTP5901/2-IPM SmartMesh IP Mote Module Datasheet
LTP5901/2-IPR SmartMesh IP Embedded Manager Datasheet
LTP5901/2-WHM SmartMesh WirelessHART Mote Module Datasheet
Eterna Board Specific Parameter Configuration Guide
Eterna Serial Programmer Guide
Eterna2 RF Certification Guide

Conventions and Terminology

This guide uses the following text conventions:

- `Computer type` indicates information that you enter, such as a URL.
- **Bold type** indicates buttons, fields, and menu commands.
- *Italic type* is used to introduce a new term.
- **Note:** Notes provide more detailed information about concepts.
- **Caution:** Cautions advise about actions that might result in loss of data.
- **Warning:** Warnings advise about actions that might cause physical harm to the hardware or your person.

Revision History

Revision	Date	Description
040-0117 rev 1	4/20/2012	Preliminary Release
040-0117 rev 2	7/25/2012	
040-0117 rev 3	1/28/2013	
040-0117 rev 4	4/3/2013	
040-0117 rev 5	6/20/2013	Update for DC9018, DC9020 and DC9021
040-0117 rev 6	9/18/2013	Update for DC9020B and DC9022A Add references to LTP5903CEN and WirelessHART User Guide
040-0117 rev 7	9/26/2014	Update for DC9004A
040-0117 rev 8	3/23/2015	Update for DC2274A-A USB Manager
040-0117 rev 9	9/24/2015	Addendum: Fuse Table and 20MHz crystal change

Getting Started

Eterna Evaluation & Development Boards

The Eterna Evaluation & Development Mote is a wireless node of the SmartMesh network. It consists of a version of the DC9003A or the DC9018A, which includes the LTC5800 Eterna mote-on-chip integrated circuit.

The Eterna Evaluation & Development Mote may operate stand-alone powered with its battery or used in a board set connected to the DC9006 Interface Board when communication over USB or JTAG is desired.

The Interface Board features an isolated USB quad serial converter and provides power and signal isolation to Eterna Evaluation & Development Board. It is used to access to the Eterna mote-on-chip API, CLI, SPI and JTAG interfaces. The Interface Board also features test points to monitor the mote current consumption and jumpers for various configurations.

Most Eterna Evaluation & Development Kits include one or several Evaluation/Development Motes, an Interface Board, and a Manager. Depending on the kit version, the manager may consist of the SmartMesh IP USB Manager (DC2274A-A[1]) or the SmartMesh WirelessHART Manager (LTP5903CEN-WHR[2]).

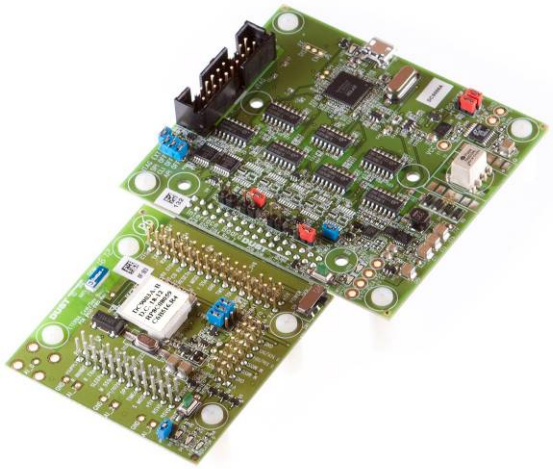


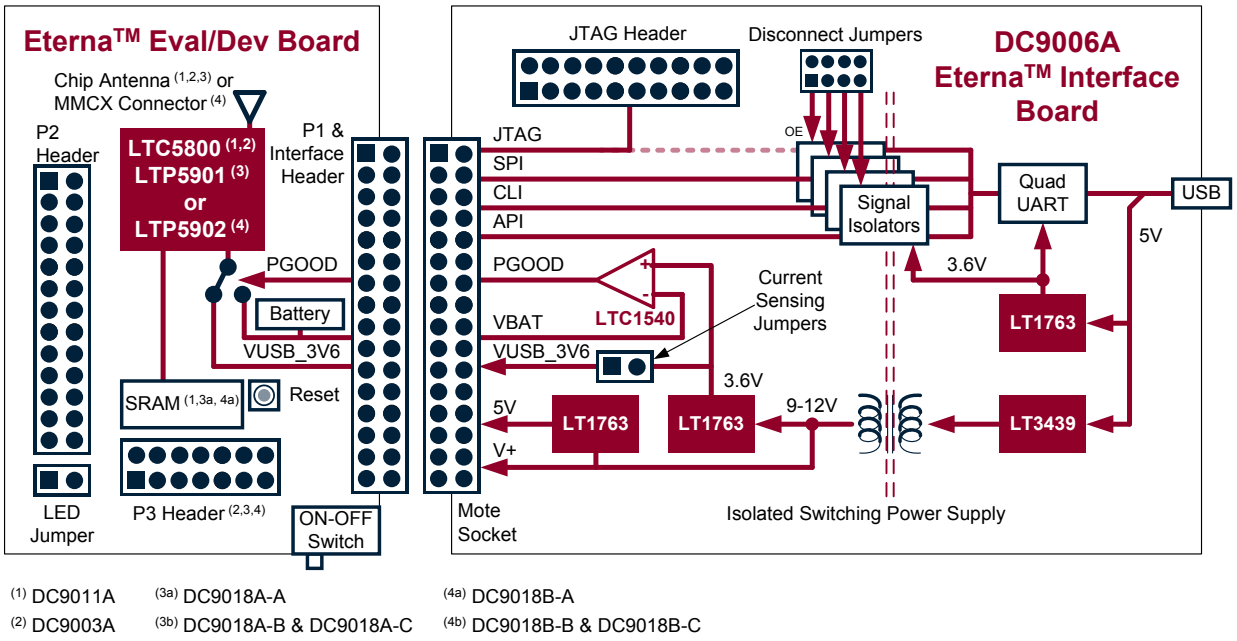
Figure 1 **DC9003 Eterna Evaluation & Development Mote (lower-left) connected to the DC9006 Interface Board (top-right)**

[1] Early versions of SmartMesh IP kits include DC9001 and DC9020 Manager assemblies.

[2] For details on the LTP5903CEN-WHR please refer to the SmartMesh WirelessHART Easy Start Guide and the SmartMesh WirelessHART User Guide.

Hardware Diagram

The following diagram depicts the main features of the Eterna Evaluation & Development Board Set.



(1) DC9011A
(2) DC9003A
(3a) DC9018A-A
(3b) DC9018A-B & DC9018A-C
(4a) DC9018B-A
(4b) DC9018B-B & DC9018B-C

Figure 2 Eterna Evaluation & Development Board Set Diagram

Installation

The Interface Board communicates with a host computer using a USB serial connection. When the Interface Board is first connected, the host computer should prompt to install a driver for it.

The Interface board requires USB driver from Future Technology Devices International (FTDI, http://www.ftdichip.com/). The FTDI "D2XX" drivers can be found at http://www.ftdichip.com/Drivers/D2XX.htm.

The FTDI serial chip set is found in many different devices and it is possible that a version of the FTDI drivers is already installed on your machine. It is important to use the latest version available on the web. The Interface board has been tested against D2XX Drivers revision 2.08.30.

Once drivers are installed for the Interface Board, one should use the same USB port each time the manager is connected to the computer. If a different USB port is used, the setup procedure will need to be repeated for that port.

The Eterna Evaluation and Development Board Set requires Windows 7 or Windows XP with SP3.

For details regarding the FTDI drivers installation, please refer to the FDTI documentation and the Eterna Serial Programmer Guide.

Setup

For details on operating the Eterna Evaluation & Development Board Set in a network, please refer to the starter kit documentation (SmartMesh IP Easy Start Guide or SmartMesh WirelessHART Easy Start Guide).

Warning

The Eterna Evaluation & Development Board includes a CR2032 Lithium battery.

Batteries can explode, ignite, leak, or cause personal injury if not used or disposed of properly. Do not open batteries; discard in fire, or heat above 100°C (212°F). Do not recharge the batteries, install them backwards, install used or other battery types, or expose battery contents to water.

Eterna Evaluation & Development Motes (DC9003 and DC9018)

Introduction

The Eterna Evaluation & Development Mote performs ultra low power wireless functions, such as sending and receiving sensor data and routing wireless packets.

The DC9003A-B and DC9003A-C versions of the Eterna Evaluation & Development Mote are included in the SmartMesh IP and WirelessHART Starter kits (respectively). The DC9018 versions integrate an RF certified module (LTP5901/2).

The following table summarizes all versions of the Eterna Evaluation and Development Motes.

Part Number	Network	Features	Notes
DC9003A-B	SmartMesh IP	LTC5800-IPM Chip Antenna	Included in Starter Kits : DC9000A and DC9000B
DC9018A-B	SmartMesh IP	LTP5901-IPM RF Certified * Chip Antenna	Included in RF Certified Kit: DC9021A
DC9018B-B	SmartMesh IP	LTP5902-IPM RF Certified * MMCX Antenna Connector	Available as an individual item, not in a kit
DC9003A-C	SmartMesh WirelessHART	LTC5800-WHM Chip Antenna	Included in Starter Kit: DC9007A
DC9018A-C	SmartMesh WirelessHART	LTP5901-WHM RF Certified * Chip Antenna	Included in RF Certified Kit: DC9022A
DC9018B-C	SmartMesh WirelessHART	LTP5902-WHM RF Certified * MMCX Antenna Connector	Available as an individual item, not in a kit
(*) Intended for regions where LTP5901/2 RF certification is required (*e.g.* Japan). Most regions do not require certification for evaluation units.			

All Eterna Evaluation & Development Boards contain an LTC5800 mote-on-chip, a battery, antenna, LEDs and signal breakout headers.

The Status LEDs provide the information about network connectivity and are available only when the LED Enable jumper is installed. Use the Reset button to manually reset a mote by pressing and releasing the button.

External sensors and digital devices may be attached to a mote via its signal breakout headers.

Hot Swap

While in operation, the Eterna Evaluation & Development Board may be connected to or disconnected from the Interface Board. Power is automatically switched from the battery to power provided from the interface board when available.

Power Switch

The Eterna Evaluation & Development Board features a sliding power switch (**SW1**) controlling the LTC5800 supply. When the Interface Board is connected, SW1 also disables the I/O lines to ensure that no power is provided in the "OFF" position.

Reset Pushbutton

The Eterna Evaluation & Development Board features a momentary push button (**PB1**). Press PB1 to reset the LTC5800.

Jumper Settings

The Eterna Evaluation & Development Board features jumper loading options. The 2mm shorting jumpers may be installed according to the following table.

Jumper	Description	Default	Note
JP1	Connects DP0 to the Interface Board (P1 EHORBAT)	OFF	
JP2	Connects DP1 to the Interface Board (P1 GPIO1)	OFF	
JP3	Connects DP2 to the Interface Board (P1 GPIO2)	OFF	
JP4	Controls the board visual indicators LED (Status 0, Status 1 and Indicator 0). Install to enable the LED functionality.	-	(1) (2) (3)

(1) Remove JP4 to prevent LED current consumption and increase battery life
(2) Default is ON for DC9011A, DC9003A-A and –B, DC9018A-A and -B, DC9018B-B
(3) Default is OFF for DC9003A-C, DC9018A-C and DC9018B-C

Figure 3 DC9003A and DC9011A[3] Board Jumpers

[3] DC9011A shown for reference only; it has been superseeded with the DC2274A-A manager

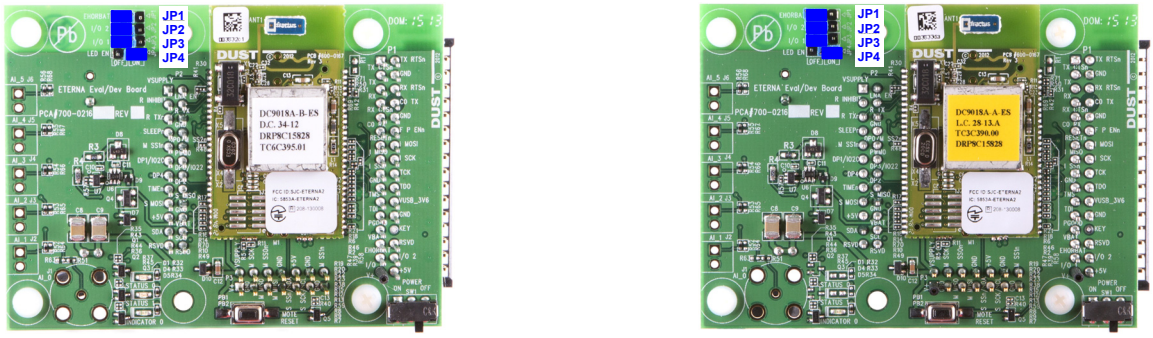


Figure 4 DC90018A-B and DC9018A-A[4] Board Jumpers

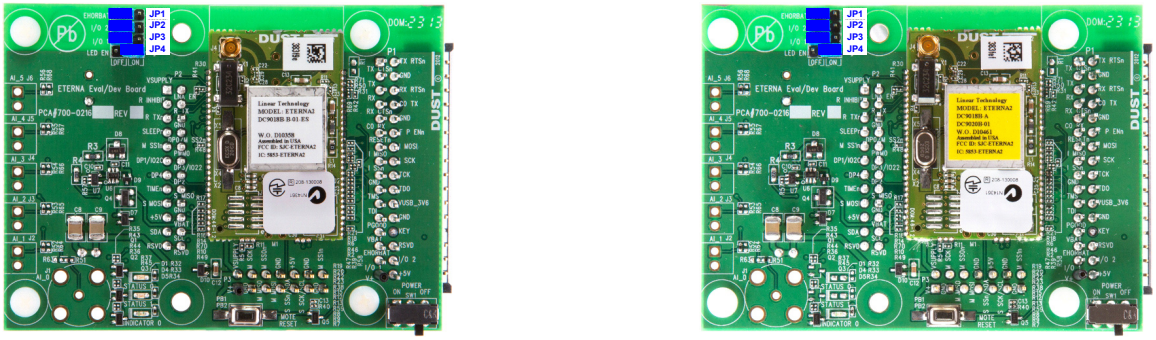


Figure 5 DC90018B-B and DC9018B-A[5] Board Jumpers

[4] DC9018A-A shown for reference only; it has been superseeded with the DC2274A-A manager

[5] DC9018B-A shown for reference only; it has been superseeded with the DC2274A-A manager

Signal Breakout Headers

For detail signal characteristics, refer to the SmartMesh IP LTC5800 or LTP59xx Datasheets.

P1: Development Header & Interface Board Connector

The following table shows the pinout of the P1 development header and connector to the Interface Board.

Pin #	Signal	Direction	Pin #	Signal	Direction
1	UART_TX_CTSn	I	2	UART_TX_RTSn	O
3	UART_TX	O	4	GND	-
5	UART_RX	I	6	UART_RX_RTSn	I
7	UART_RX_CTSn	O	8	UARTC0_TX/UARTC1_TX	O
9	UARTC0_RX/UARTC1_RX	I	10	GND	I
11	RESETn	I	12	FLASH_P_ENn (GPIO2)	I/O
13	IPCS_MISO (GPIO6)	I/O	14	IPCS_MOSI (GPIO5)	I/O
15	IPCS_SSn (GPIO3)	I/O	16	IPCS_SCK (GPIO4)	I/O
17	GND	I/O	18	TCK	I/O
19	TMS	I	20	TDO	I
21	TDI	O	22	VUSB_3V6	-
23	PGOOD	I	24	GND	-
25	VBATTERY	-	26	KEY	NC
27	Reserved (EHORBAT)	I/O	28	Reserved (MOTE_OFF)	I/O
29	Reserved (GPIO1)	I/O	30	Reserved (GPIO2)	I/O
31	V+	-	32	+5V	-

Signal direction is relative to the Eterna Evaluation and Development Board
Highlighted signals provide reserved connections for the evaluation of energy harvesting solutions
Mating connector: Samtec SSW-116-02-F-D or SSW-116-02-F-D-RA-025 (polarized right angle)

P2: Development Header

The following table shows the pinout of the P2 development header.

Pin #	Signal	Direction	Pin #	Signal	Direction
1	VSUPPLY	-	2	LNA_EN	O
3	RADIO_INHIBIT	I	4	RADIO_TX	O
5	RADIO_TXn	O	6	GND	-
7	SLEEPn	I	8	DP0 (SPIM_SS2n)	O
9	SPIM_SS1n	I/O	10	PWM0	I/O
11	DP1 (GPIO20)	I/O	12	DP3 (GPIO22)	I/O
13	DP4 (GPIO23)	I/O	14	DP2 (GPIO21)	I/O
15	TIMEn	I/O	16	SPIS_MISO (UARTC1_TX / 1-Wire)	O
17	SPIS_MOSI (UARTC1_RX)	I	18	GND	-
19	+5V	-	20	VBATTERY	-
21	Reserved (SDA)	-	22	Reserved (SCL)	-
23	Reserved (No Connect)	-	24	Reserved (No Connect)	-

Signal direction is relative to the Eterna Evaluation and Development Board
Mating connector: Samtec SSW-112-02-F-D

P3: Development Header (DC9003A, DC9018x-B/C only)

The following table shows the pinout of the P3 development header.

P3 signals are compatible with signals defined in the QuikEval interface. The header is however .100" pitch (instead of 2mm for QuikEval) in order to facilitate signal probing.

Pin #	Signal	Direction	Pin #	Signal	Direction
1	V+	-	2	VSUPPLY	-
3	GND	-	4	SPIM_SCK	O
5	SPIM_MISO	I	6	SPIM_SS0n	I/O
7	SPIM_MOSI	I/O	8	GND	-
9	SPIS_SSn (SDA)	I/O	10	+5V	-
11	SPIS_SCK (SCL)	I/O	12	GND	-
13	GND	-	14	SPIM_SS1n	I/O

Signal direction is relative to the Eterna Evaluation and Development Board.
Mating connector: Samtec SSW-107-02-F-D
P3 interface is not supported in the manager versions (DC9011, DC9018x-A or DC9018x-A)

J1, J2, J3 & J4: Analog Inputs (DC9003A and DC9018 only)

The Eterna Evaluation & Development Mote features four analog input test points directly connected to the LTC5800 ADC input pins.

J1, J2, J3 and J4 are not installed. Their connector pads may be used as test points, labeled "AI_0", "AI_1", "AI_2" & "AI_4" on the top side of the board.

The following table shows sourcing information for the analog connectors, should those connectors be required for specific evaluation or development applications.

Connector	Description	Manufacturer	Part Number
J1	BNC SOCKET50 OHM ELBOW	TE Connectivity	5-1634556-0
J2, J3, J4 (DC9003A)	3.5MM TERMINAL BLOCK	On Shore Technology Inc	OSTTE020104
J2, J3, J4 (DC9018)	100MIL TERMINAL BLOCK	On Shore Technology Inc	OSTVN02A150

Evaluation Managers

The manager coordinates routing, monitors and controls the SmartMesh network performance, collects network statistics, and publishes data via its computer interface.

Types of SmartMesh Evaluation Managers

The following table summarizes all versions of the Eterna Evaluation and Development Managers.

Part Number	Network	Features	Notes
DC2274A-A (**)	SmartMesh IP	LTP5902-IPRB Packaged USB Manager On-Board Memory RP-SMA dipole antenna	Up to 100-mote networks RF Certified *
LTP5903CEN-WHR	SmartMesh WirelessHART	Packaged Manager On-Board Memory RP-SMA dipole antenna	Up to 250-mote networks RF Certified *
DC9001A	SmartMesh IP	LTC5800-IPRA Chip Antenna	Up to 32-mote networks
DC9001B	SmartMesh IP	LTC5800-IPRB On-Board Memory Chip Antenna	Up to 100-mote networks
DC9020A	SmartMesh IP	LTP5901-IPRB On-Board Memory Chip Antenna	Up to 100-mote networks RF Certified *
DC9020B	SmartMesh IP	LTP5902-IPRB On-Board Memory MMCX Antenna Connector	Up to 100-mote networks RF Certified *
(*) Most regions do not require certification for evaluation units (**) Replaces DC9001 and DC9020 managers in most evaluation kits			

SmartMesh IP USB Manager (DC2274A-A)

The DC2274A-A evaluation SmartMesh IP USB manager features the LTP5902-IPRB, on-board SRAM and supports 100-mote IP networks.

Figure 6 SmartMesh IP USB Manager (DC2274A-A)

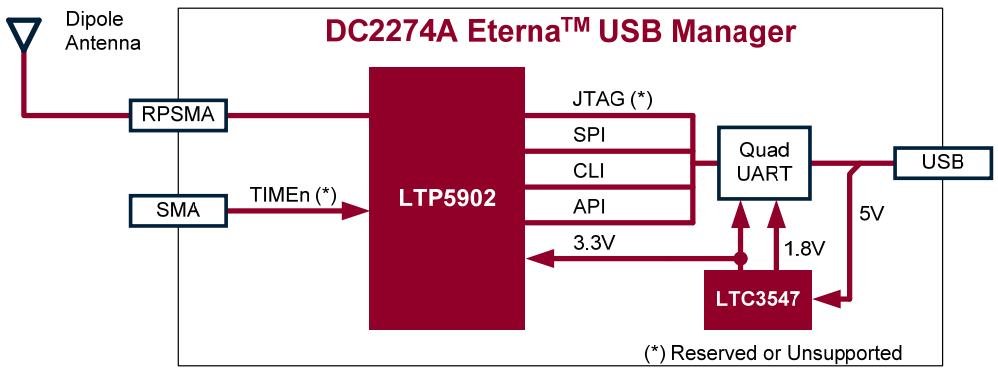


Figure 7 DC2274A-A Block Diagram

The DC2274A-A plugs into a computer USB 2.0 port and requires USB driver from Future Technology Devices International (FTDI, http://www.ftdichip.com/). The FTDI "D2XX" drivers can be found at http://www.ftdichip.com/Drivers/D2XX.htm. Please follow the installation instruction in Getting Started section.

The DC2274A-A is certified in countries where the LTP5901/2 are certified (refer to the Eterna2 RF Certification Guide for details).

Figure 8 SmartMesh IP USB Manager (DC2274A-A) in PC

SMA Input (Reserved)

The DC2274A-A evaluation SmartMesh IP USB manager features a SMA connector connected as an Input to the TIMEn signal of the LTP5902. This 5V tolerant input is reserved for future use.

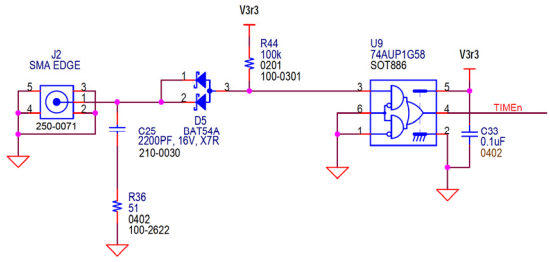


Figure 9 SmartMesh IP USB Manager SMA Input

SmartMesh WirelessHART Manager (LTP5903CEN-WHR)

In some SmartMesh WirelessHART evaluation kits such as the DC9007A and DC9022A, the Eterna Evaluation & Development Board Set is accompanied by a packaged SmartMesh WirelessHART Manager (LTP5903CEN-WHR), shown below.

For details on the LTP5903CEN-WHR please refer to the SmartMesh WirelessHART Easy Start Guide and the SmartMesh WirelessHART User Guide.

Figure 10 SmartMesh WirelessHART Manager (LTP5903CEN-WHR)

Legacy SmartMesh IP Evaluation Managers (DC9001, DC9020)

Early evaluation kits featured the following manager versions: DC9001A/B and DC9020A/B. Theses managers are composed of a DC9006A Interface Board connected to an evaluation board fitted a LTC5800-IPR Manager-on-Chip.

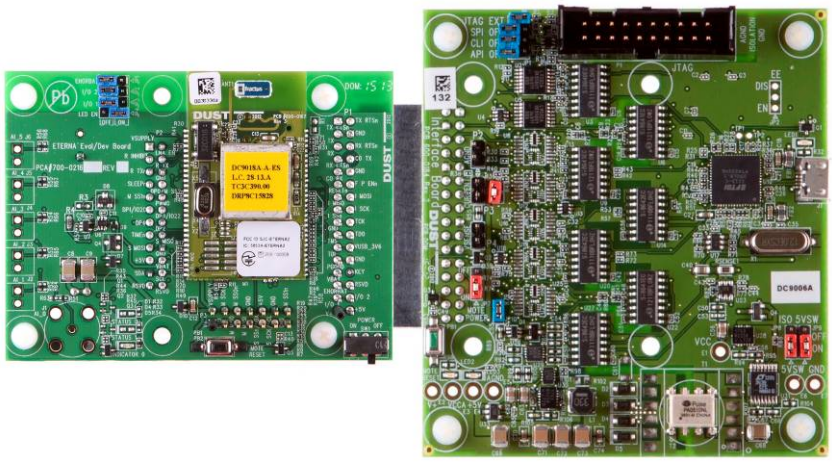


Figure 11 Early Evaluation & Development Manager, comprised of two boards

The DC9001B SmartMesh IP evaluation manager sub-assembly features the LTC5800-IPRB, on-board SRAM and supports 100-mote IP networks. The DC9001A features the LTC5800-IPRA and supports up to 32 IP motes. The DC9020A integrates the LTP5901-IPRB RF certified manager PCB module with chip antenna, on-board SRAM and supports up to 100 IP motes. The DC9020B integrates the LTP5902-IPRB RF certified manager PCB module with MMCX antenna connector, on-board SRAM and supports up to 100 IP motes. The DC9020A and DC9020B are certified in countries where the LTP5901/2 are certified (refer to the Eterna2 RF Certification Guide for details).

An manager sub-assembly board is normally powered through its Interface Board. However, it automatically switches to an on-board battery when the Interface Board power is temporarily interrupted.

The Indicator LED is illuminated when the power switch is turned on and the manager is receiving power and functioning properly. The Indicator LED is off when the power switch is off. If the Interface Board is disconnected and the LED fails to turn on when the power switch is on, it indicates that the battery is drained or missing. The **status LEDs** on the manager are not used.

The Reset button restarts the manager's software processes and wireless connection, causing the network to reform.

Interface Board (DC9006A)

USB Interface

The Interface Board communication interface to the USB host consists of four serial ports. After the FTDI driver installation, sequential serial ports are allocated to the Interface Board.

JTAG

The allocation of the first USB serial port is reserved for an isolated JTAG access, only available when JP1 “JTAG EXT” jumper is removed and no external JTAG is connected.

The USB JTAG feature of the Interface Board is not supported.

SPI

The second USB serial port is connected to the Eterna Evaluation & Development Mote slave serial interface (when JP1 “SPI OFF” jumper is not installed).

Further documentation on this interface is available in the Eterna Serial Programmer Guide.

CLI

The third USB serial port provides access to the UARTC0_TX and UARTC0_RX lines of the LTC5800 (when JP1 “CLI OFF” jumper is not installed).

A 2-wire serial interface is supported; the baud rate is application dependant and shall be described in specific evaluation and development tool documentation.

For example, at the time of redaction of this document, in the SmartMesh IP Evaluation Kit the default baud rate is 9600 baud.

API

The fourth USB serial port provides access to the serial API of the Eterna Evaluation & Development Board manager (when JP1 “API OFF” jumper is not installed).

The API serial interface supports from 2-wire to 6-wire communication, the baud rate is application dependant and shall be described in specific evaluation and development tool documentation.

Power Switch-Over

The Interface Board compares its VCCA rail to the battery voltage from the Eterna Evaluation & Development Board. When the VCCA rail is within 150 mV of the battery voltage, the PGOOD signal is asserted.

The Eterna Evaluation & Development Board uses the PGOOD signal to switch its supply from battery to the power provided by the Interface Board (VUSB_3V6).

Signal & Power Isolation

The Interface Board provides isolated power and signals to the Eterna Evaluation & Development Board from the USB micro-B interface (**J1**).

The external JTAG connector (**P1**) features signals that are directly connected to the Eterna Evaluation & Development Board connector. P1 signals are referenced to the isolated ground.

External JTAG & Reset Pushbutton

The external JTAG connector (**P1**) allows the use of 3rd party development systems with the Eterna Evaluation & Development Board. P1 is a 2x10 pin .100" header compatible with JTAG/SWD emulators such as IAR or Segger J-Link.

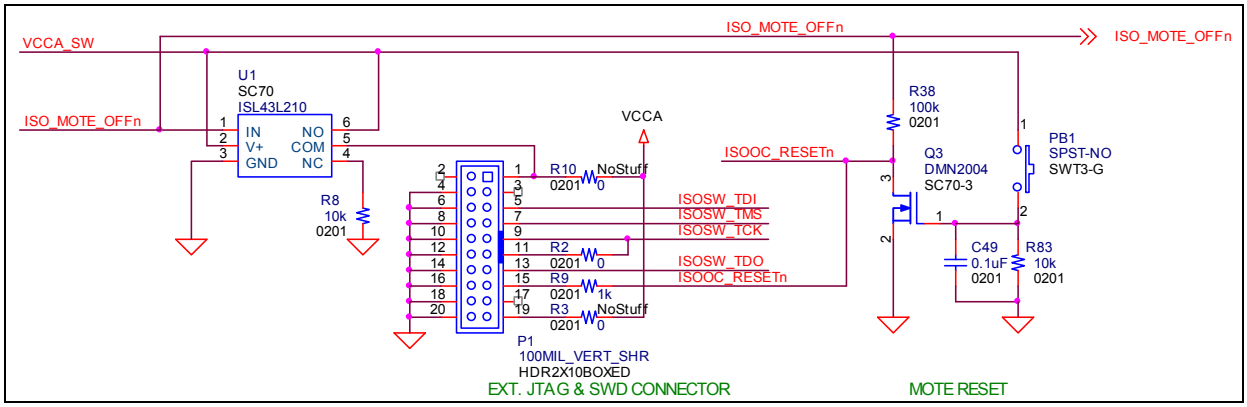


Figure 12 External JTAG Pinout, Reset & Vsense Logic

The Interface Board features a momentary push button (**PB1**). PB1 only asserts the JTAG and the Eterna Evaluation & Development Board reset signal (RESETn).

Mote Current Sensing

The Interface Board provides two current sensing headers (P3 and P4) working in conjunction with the JP5 jumper as shown in the schematics below.

With **JP5** jumper installed, a voltmeter across **P4** will measure the mote consumption: P4 voltage is equal to 10 times the mote current (voltage drop across the 10-ohm sense resistor R55 caused by the ISO_VSUPPLY current).

Alternatively and with **JP5** is removed, a ammeter may be connected across **P3** to directly measure the mote current.

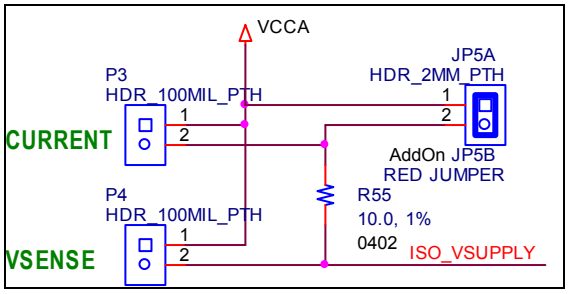


Figure 13 Current Sensing Jumpers

A third 0.100" header **P2** is provided for ground reference. Both P2 pins are connected to the isolated ground.

For accurate current measurements, all **JP1** headers shall be installed (see section: Mote Signal Disconnection).

Jumper Settings

The Interface Board features jumper loading options. The 2mm shorting jumpers may be installed according to the following table.

Jumper	Description	Default	Note
JP1	Disconnect signals to the Eterna Evaluation and Development Board, install JP1 jumpers as follows: "JTAG EXT" to enable the External JTAG port, this jumper disconnects the JTAG lines from one of the USB serial interface and should always be installed unless the USB JTAG interface is supported in the development or evaluation tools; "SPI OFF" to disconnect SPI lines, RESETn and FLASH_P_ENn; "CLI OFF" to disconnect UARTC0 TX and RX; and, "API OFF" to disconnect serial API signals.	ON OFF OFF OFF	
JP5	Carries current to the Eterna Evaluation and Development Board. JP5 should always be installed unless an ammeter is connected across the P3 header.	ON	
JP7	Enables the VCCA rail, the 3.6V isolated power supply to the Eterna Evaluation and Development Board. JP7 should normally be installed in the "ON" position (pin 1 & 2); the "OFF" position (pin 2 & 3) may be used to disable the VCCA rail and provide power from an external source.	ON	(1)
JP8	Controls the isolated supplies of the Interface Board (V+ and the derived VCCA and +5V rails). JP8 should normally be installed in the "ON" position (pin 1 & 2); the "OFF" position (pin 2 & 3) may be used to disable the on-board generation of the isolated V+ supply and provide power from an external source set between 9V and 12V.	ON	(1)
JP9	Controls a power switch on the USB 5V supply. JP8 should normally be installed in the "ON" position (pin 1 & 2); the "OFF" position (pin 2 & 3) may be used to disconnect the Interface Board from the USB 5V supply.	ON	(1)
JP10	Connects the Eterna Evaluation and Development Board battery to logic that determines when power is to be switched from battery to the isolated VCCA rail. JP10 jumper should normally be installed for proper power switching operation. JP10 jumper may be removed to prevent battery current flow in special situations such as unpowered Interface Board connected to the Eterna Evaluation & Development Board.	ON	

(1) when no jumper is installed, the Interface Board defaults to the "ON" state

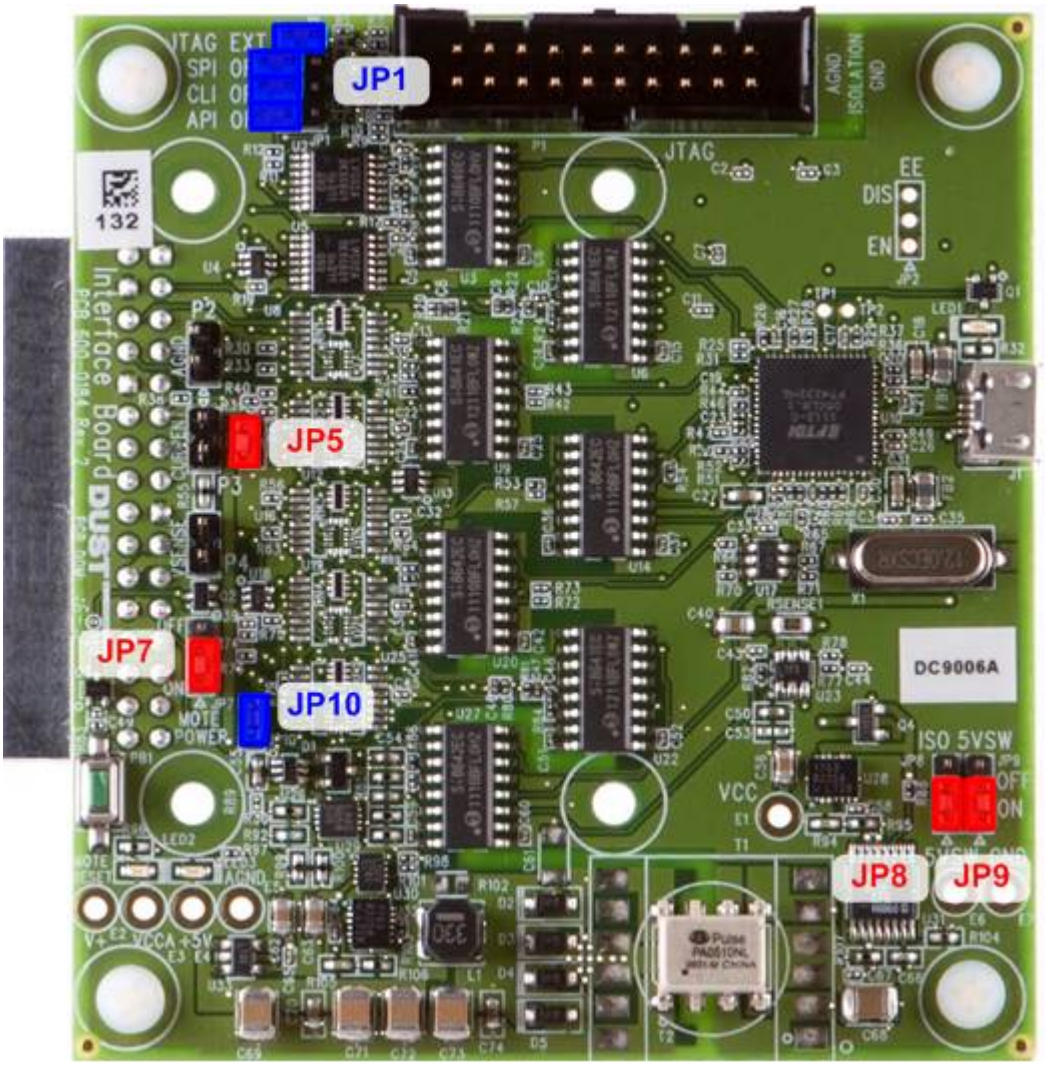


Figure 14 Interface Board Jumpers

Interface Signal Disconnection

To perform accurate current measurements, it is recommended to disconnect the Interface Board signals from the Eterna Evaluation & Development Board by installing all JP1 jumpers.

Since so little power is required by the LTC5800 to operate, the Eterna Evaluation & Development Board may gather enough power from current flowing through the Interface Board signals and its ESD protection diodes.

Programming Adapter (DC9004A)

Introduction

The DC9004A Programming Adapter enables the DC9006A Interface card to connect to the recommended programming header (2x5 2mm pitch header) on a customer board to program an Eterna chip or PCB module or to communicate via CLI.

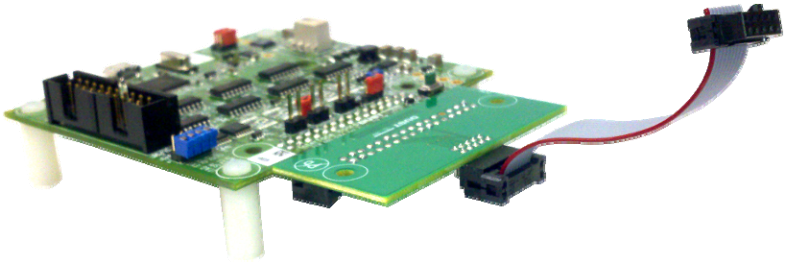


Figure 15 DC9004A (right) installed on a DC9006A (left)

Usage

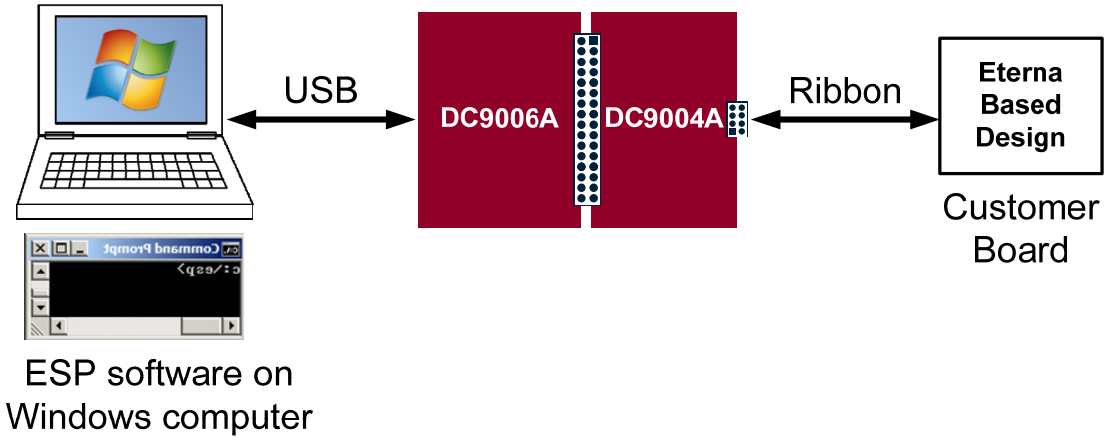


Figure 16 Connecting an Eterna Design to the DC9004A

For a non-powered customer board, where the customer board is powered by the VSUPPLY and GND signals of the DC9004A, simply connect the ribbon cable.

For an independently powered customer board, first place the DC9006A JP7 jumper (see Figure 14) in the "OFF" position, then connect the ribbon cable. Note that in this configuration the DC9006A will draw some power from the customer board to power some of its circuitry.

Interfaces

DC9006A Interface

The interface to the DC9006A consists of a 0.1" pitch 2x16 header with the same signals described in section "P1: Development Header & Interface Card Connector".

Programming Interface (2x5 2mm pitch header)

The programming header signals are shown below.

Pin #	Signal	Direction	Pin #	Signal	Direction
1	IPCS_SSn	O	2	FLASH_P_ENn	O
3	IPCS_SCK	O	4	IPCS_MOSI	O
5	IPCS_MISO	I	6	RESETn	O
7	VSUPPLY	-	8	GND	-
9	UARTC0_TX/UARTC1_TX	I	10	UARTC0_RX/UARTC1_RX	O
Signal direction is relative to the Programming Adapter board.					

Limitations

Ribbon Cable Length

For early versions of the DC9006A (700-0184 rev5 or earlier), the maximum recommended ribbon cable length is 2".

Voltage Level

In the configuration where the customer board is independently powered, the voltage supply must be greater than 2.7V.

Feature Comparison with DC9010

DC9010 vs. DC9004

The following table shows a feature comparison with the DC9010 Eterna Programmer (See Eterna Serial Programmer Guide).

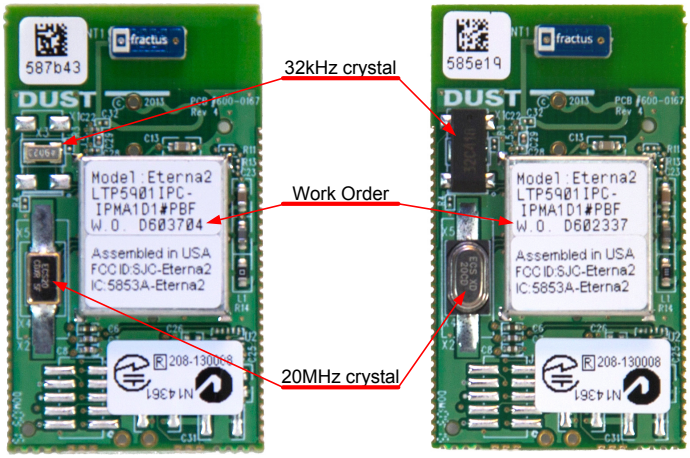
	Supports Recommended Header (2x5 2mm)	Enables CLI access	Enables FLASH SPI Programming	Provides Crystal Calibration Reference	Features LTP5900 Socket
DC9004A w/DC9006A	✓	✓	✓		
DC9010A	✓	✓	✓	✓	✓ (*) (**)

(*) LTP5900 does not include CLI; (**) Requires opening the DC9010A enclosure

Addendum

Crystal changes on Printed Circuit Assembly (PCA) and Demo Circuits

Starting with Work Order ("WO") number D603679, PCA products and Demo Circuits containing the LTC5800 feature different crystals. The following image illustrates the differences on an LTP5901 PCA product.



New (WO# > D603679) Former (WO# < D603679)

Board Specific Parameters ("Fuse Table") associated with the version of 20MHz crystal

If a PCA Product (LTP59xx) or a Demo Circuit (DCxxxx) is reprogrammed after it leaves the factory, attention should be given to Board Specific Parameters.

Linear Technology provides binary images of the Board Specific Parameters called "Fuse Tables" for each PCA Product and Demo Circuit. Fuse Table files are named after the product and an internal part number of the form 680-xxxx-yyyy, where xxxx is a sequential number specific to the PCA or Demo Circuit and yyyy is a version number.

PCA products and Demo Circuits[6] based on LTP5901 and LTP5902 with WO greater than D603679 shall include Board Specific Parameters with version -0003 or newer.

LTP5900 products with WO greater than D603679 shall include Board Specific Parameters with version -0005 or newer.

Other Demo Circuits such as the DC9000, DC9001, DC9003 and DC9007 are all built prior to WO D603679 and may be programmed with any of the respective mote or manager recommended Board Specific Parameters.

[6] Demo Circuits based on LTP5901 or LTP5902 include DC9018, DC9020, DC9021, DC2126 and DC2274 series

Board Specific Parameters ("Fuse Table") for PCA with WO# D603679 or newer (greater)

PCA Products or Demo Circuits for WO number equal or greater than D603679 shall be programmed with the Fuse Tables shown below (or newer).

Current Products	Fuse Table
LTP5900IPC-WHMA	FT-LTP5900-WHMA-M13-9600-115K-680-0204-0005REV1.bin
LTP5901IPC-IPMA [7]	FT-LTP5901-IPMA-M4-115K-680-0237-0003REV1.bin FT-LTP5901-IPRA-M4-115K-680-0238-0003REV1.bin FT-LTP5901-IPRB-MEM-128K-M4-115K-680-0301-0003REV1.bin
LTP5901IPC-WHMA	FT-LTP5901-WHMA-M4-115K-680-0236-0003REV1.bin
LTP5902IPC-IPMA [7]	FT-LTP5902-IPMA-M4-115K-680-0241-0003REV1.bin FT-LTP5902-IPRA-M4-115K-680-0242-0003REV1.bin FT-LTP5902-IPRB-MEM-128K-M4-115K-680-0302-0003REV1.bin
LTP5902IPC-WHMA	FT-LTP5902-WHMA-M4-115K-680-0240-0003REV1.bin

Legacy Products [8]	Fuse Table (if WO is D603679 or greater)
LTP5900IPC-WHMA***	FT-LTP5900-WHMA-M13-9600-115K-680-0204-0005REV1.bin
LTP5901IPC-IPMA***	FT-LTP5901-IPMA-M4-115K-680-0237-0003REV1.bin
LTP5901IPC-IPRA***	FT-LTP5901-IPRA-M4-115K-680-0238-0003REV1.bin
LTP5901IPC-IPRB***	FT-LTP5901-IPRB-MEM-128K-M4-115K-680-0301-0003REV1.bin
LTP5901IPC-IPRC***	FT-LTP5901-IPRC-MEM-128K-M4-115K-680-0305-0003REV1.bin
LTP5901IPC-WHMA***	FT-LTP5901-WHMA-M4-115K-680-0236-0003REV1.bin
LTP5902IPC-IPMA***	FT-LTP5902-IPMA-M4-115K-680-0241-0003REV1.bin
LTP5902IPC-IPRA***	FT-LTP5902-IPRA-M4-115K-680-0242-0003REV1.bin
LTP5902IPC-IPRB***	FT-LTP5902-IPRB-MEM-128K-M4-115K-680-0302-0003REV1.bin
LTP5902IPC-IPRC***	FT-LTP5902-IPRC-MEM-128K-M4-115K-680-0306-0003REV1.bin
LTP5902IPC-WHMA***	FT-LTP5902-WHMA-M4-115K-680-0240-0003REV1.bin

[7] LTP5901IPC-IPMA and LTP5902IPC-IPMA products may be programmed as a mote, 32-mote manager (which does not require external memory) or 100-mote manager (which requires external memory). The programmed software image shall include the Main Executable corresponding to the mote or manager function and the Fuse Table specified in this table. The Fuse Tables are respectively named after -IPMA, -IPRA and -IPRB, for mote, manager and manager with memory.

[8] LTP5900, LTP5901 and LTP5902 based products were originally shipped pre-programmed at the factory; these product versions are still available but referred to as Legacy Products. In this column, "***" represents a three digit alphanumeric field signifying the pre-programmed software revision (e.g. "LTP5901IPC-IPMA**1D1**"). If a Legacy Product is re-programmed and its WO number is greater than D603679, the Fuse Table specified in this table or newer is required.

Demo Circuits	Fuse Table (if WO is D603679 or greater)
DC2126A	FT-LTP5901-IPMA-M4-115K-680-0237-0003REV1.bin
DC2274A-A	FT-DC2274A-MEM-128K-M4-115K-680-0383-0003REV1.bin
DC9018A-B	FT-DC9018A-MOTE-M4-115K-680-0379-0003REV1.bin
DC9018A-C	FT-DC9018A-MOTE-M4-115K-680-0379-0003REV1.bin
DC9018B-B	FT-DC9018B-MOTE-M4-115K-680-0380-0003REV1.bin
DC9018B-C	FT-DC9018B-MOTE-M4-115K-680-0380-0003REV1.bin
DC9020A	FT-DC9020A-MANAGER-MEM-128K-M4-115K-680-0381-0003REV1.bin
DC9020B	FT-DC9020B-MANAGER-MEM-128K-M4-115K-680-0382-0003REV1.bin

Board Specific Parameters ("Fuse Table") for PCA with WO# older than D603679

The following details the latest compatible Fuse Table for older PCA Products or Demo Circuits with WO number smaller than D603679.

Legacy Products [8]	Fuse Table (if WO is smaller than D603679)
LTP5900IPC-WHMA***	FT-LTP5900-WHMA-M13-9600-115K-680-0204-0004REV1.bin
LTP5901IPC-IPMA***	FT-LTP5901-IPMA-M4-115K-680-0237-0002REV1.bin
LTP5901IPC-IPRA***	FT-LTP5901-IPRA-M4-115K-680-0238-0002REV1.bin
LTP5901IPC-IPRB***	FT-LTP5901-IPRB-MEM-128K-M4-115K-680-0301-0002REV1.bin
LTP5901IPC-IPRC***	FT-LTP5901-IPRC-MEM-128K-M4-115K-680-0305-0002REV1.bin
LTP5901IPC-WHMA***	FT-LTP5901-WHMA-M4-115K-680-0236-0002REV1.bin
LTP5902IPC-IPMA***	FT-LTP5902-IPMA-M4-115K-680-0241-0002REV1.bin
LTP5902IPC-IPRA***	FT-LTP5902-IPRA-M4-115K-680-0242-0002REV1.bin
LTP5902IPC-IPRB***	FT-LTP5902-IPRB-MEM-128K-M4-115K-680-0302-0002REV1.bin
LTP5902IPC-IPRC***	FT-LTP5902-IPRC-MEM-128K-M4-115K-680-0306-0002REV1.bin
LTP5902IPC-WHMA***	FT-LTP5902-WHMA-M4-115K-680-0240-0002REV1.bin

Older Demo Circuits	Fuse Table (if WO is smaller than D603679)
DC2126A	FT-LTP5901-IPMA-M4-115K-680-0237-0002REV1.bin
DC2274A-A	FT-DC2274A-MEM-128K-M4-115K-680-0383-0002REV1.bin
DC9001A	FT-DC9003A-M4-115K-680-0222-0004REV1.bin
DC9001B	FT-DC9011A-M4-115K-MEM256k-680-0258-0003REV1.bin
DC9003A-B	FT-DC9003A-M4-115K-680-0222-0004REV1.bin
DC9003A-C	FT-DC9003A-M4-115K-680-0222-0004REV1.bin
DC9018A-B	FT-DC9018A-MOTE-M4-115K-680-0379-0002REV1.bin
DC9018A-C	FT-DC9018A-MOTE-M4-115K-680-0379-0002REV1.bin
DC9018B-B	FT-DC9018B-MOTE-M4-115K-680-0380-0002REV1.bin
DC9018B-C	FT-DC9018B-MOTE-M4-115K-680-0380-0002REV1.bin
DC9020A	FT-DC9020A-MANAGER-MEM-128K-M4-115K-680-0381-0002REV1.bin
DC9020B	FT-DC9020B-MANAGER-MEM-128K-M4-115K-680-0382-0002REV1.bin

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