LT4363-1/LT4363-2 12V Systems ISO-7637-2 Surge Stopper

DESCRIPTION

Demonstration circuit 2062A showcases the LT®4363 surge stopper in a 12V, 3A ISO-7637-2 application. Inputs of up to 50VDC and load dumps of up to 100V are limited to 25V at the output. The MOSFET is protected against output overloads by current limiting. Sustained overvoltage or overcurrent conditions cause the LT4363 to turn off after a timer delay. The LT4363-1 (DC2062A-A) latches off and is reset by pulling $\overline{SHDN}$ low for at least 100µs. The LT4363-2 (DC2062A-B) automatically retries after a cool down delay; retry is inhibited if OV is higher than 1.275V.

Danger! High voltage testing should be performed by qualified personnel only. As a safety precaution at least two people should be present during high voltage testing.

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Board Layout

DC2062A is designed to withstand load dump. This high voltage is stood off by RUV4, ROV4, R7, RLED2, Q1, Q4. Maximum input voltage is limited by Q1's 100V BV_{DSS} rating. The permissible time at 100V is limited by MOSFET safe operating area (SOA) and R7, which dissipates slightly less than 1.2W and is capable of doing so for at least 500ms.

The minimum spacing is limited by 1206 pad spacing where the gap between solder pads is 2mm, or just under 80mils. Thus, the spacing between the input plane and all other board traces is maintained at a minimum of 2mm. As a point of reference, a 2mm needle gap in air breaks down well above 1kV.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input supply	Operating	5	12	23.5	V
	DC Survival	50			V
	500ms Transient	100			V
Reverse Input Protection	DC Survival	–30			V
	1ms Transient	–150			V
Output Regulation Voltage		23.5	25	25.4	V
Undervoltage Threshold		4	4.2	4.4	V
Retry Inhibit Threshold		18.2	19.1	20	V
Current Limit		3	3.8	4.6	A

QUICK START PROCEDURE

ISO-7637-2 Compliance

The DC2062A is fully compatible with electrical transients in a 12V ISO-7637-2 system. Compliance testing was performed by a third party company called TUV. Tests were performed at level 4, which is the most extreme condition an ISO-7637-2 system can face. The compliance report can be found on the sidebar of the LT4363 product landing page.

A summary of the report is shown in Table 1.

Load Dump Ride Through

The DC2062A showcases the ability of the LT4363 to ride through and suppress a 100V load dump pulse. While the DC2062A can ride through load dump events, several points should be kept in mind. First, the dissipation of several components rises to significant levels during a load dump event. Since this event lasts for approximately 500ms, these components are dissipating power for an appreciable amount of time. RUV4 dissipates 200mW, ROV4 dissipates 60mW, D1 dissipates 3.2W and R7 dissipates nearly 1.2W. These components are dissipating power for the duration of the 100V pulse and have been rated appropriately.

Another consideration is MOSFET SOA. Q1 dissipates an average of 80W throughout the time it is regulating a load dump pulse. While many modern MOSFETs have advertised power ratings much higher than 80W, these ratings are not indicative of performance in surge stopper applications for the following reasons: 1) The power ratings only apply for operation in triode and when the DUT is mounted on an infinite heat sink. 2) The power capability of a MOSFET reduces significantly when it is operated in saturation with a high V_{DS} across it.

MOSFET manufacturers provide an SOA graph which depicts the voltage and current conditions under which a MOSFET can be expected to operate safely. When selecting MOSFETs for a surge stopper application this graph must always be consulted carefully due to the fact that the points on the graph were tested under the previously discussed conditions.

Reverse Input Protection

The DC2062A features reverse protection circuitry that protects downstream components from reverse transients of up to –150V. This number is limited by the BV_{DSS} of Q2. The reverse protection circuitry also protects against reverse DC voltage of up to –30V.

DC2062A-A and DC2062A–B Options

The DC2062A-A is fitted with the LT4363-1 which latches off after a timer delay in the presence of overvoltage or overcurrent conditions. Once latched off the LT4363-1 may be restarted by pulsing the $\overline{SHDN}$ pin low for at least 100µs, or by briefly cycling power.

The DC2062A-B is fitted with the LT4363-2 which automatically retries after a cool-down cycle. Retry is inhibited by the OV pin, if the input is greater than 20V. Cool down time is typically 22.8 seconds.

Table 1. TUV ISO-7637 Report Summary

				CLASSIFICATION OF FUNCTIONAL STATUS			
TEST PULSE	LEVEL IV REQUIREMENTS	LEVEL PASSED	# OF PULSES/ DURATION	NO DEVIATION	DEVIATION WITHIN SPECIFICATION	DOES NOT COMPLY	NOT PERFORMED
1	–100V	–100V	5000 Pulses	❑ Class A	■ Class A	❑	❑
2a	+50V	+50V	5000 Pulses	■ Class A	❑ Class A	❑	❑
2b	+10V	+10V	10 Pulses	❑ Class A	■ Class A	❑	❑
3a	–150V	–150V	1 Hour	■ Class A	❑ Class A	❑	❑
3b	+100V	+100V	1 Hour	■ Class A	❑ Class A	❑	❑
4	–7V	–7V	3 Pulse	❑ Class A	■ Class A	❑	❑
5	+87V	+89V	3 Pulse	■ Class A	❑ Class A	❑	❑

QUICK START PROCEDURE

Operation

The shutdown pin, $\overline{SHDN}$, is floating so that when power is applied to the input, the LT4363 automatically turns on. The LT4363 protects the load from destruction by regulating the output voltage to a safe level during intervals of input overvoltage. DC2062A is designed to regulate the output at 25V. If the input voltage is less than 25V, power passes through directly to the output. The output is sensed by the R1/R2 divider and the FB pin. The GATE pin controls Q1 to regulate the output voltage in the event the input rises above 25V.

Overcurrent is sensed by RSNS and the SNS and OUT pins of the LT4363. If the load current reaches 50mV/13mΩ, the GATE pin will control Q1 to regulate the output current at 3.8A.

In both overcurrent and overvoltage conditions, current is sourced by the TMR pin into the timer capacitor, CTMR. It charges and upon reaching 1.375V, causes the LT4363 to turn off the MOSFET. As previously mentioned the LT4363-1 version latches off, while the LT4363-2 version automatically tries to restart the load after a 22.8 second cool-down interval.

The timer interval before the MOSFET turns off is variable, depending on the type and severity of the fault, and ranges from 135ms to 640ms. The cool-down time is 22.8s. For the LT4363-2 version, automatic retry is inhibited by the OV pin if the input remains higher than 20V, as set by the ROV4-ROV6 divider. For the LT4363-1 version, the OV pin becomes a ground pin (GND, Pin 7) and it is shorted to ground by a 0Ω jumper at ROV6. The LT4363-1 version simply latches off in response to a fault. Restart by pulling $\overline{SHDN}$ low for at least 100µs, or by briefly disconnecting the input supply.

The combined tolerances of the LT4363 and external resistive dividers are approximately 4% for output voltage regulation (FB pin), 5% for undervoltage (UV pin) and retry inhibit threshold (OV pin), and 21% for current limit.

A performance summary is shown in a table on the schematic diagram and is silk-screened on the front of the demo board for easy reference.

Test Points

A summary of the test points and their related LT4363 pin is shown in Table 2.

Table 2.

Test Point	LT4363 Pin
INPUT	(Board Input)
DRAIN	(Junction of Drains of Q1 & Q2)
GATE	GATE
SNS	SNS
OUT	OUT
GND	GND
DGATE	(Q2 Gate)
V_{CC}	V_{CC}

Small Turrets

No connection to any of the small turrets is necessary to make the board operate—the LT4363 defaults to the ON state. If the $\overline{SHDN}$ turret is left open, the board will turn on when power is applied. Short this turret to ground to turn off the LT4363.

$\overline{FLT}$ and ENOUT are open-collector outputs. If used, pull up to the output or an output-derived external logic supply. There are no pull-ups included on DC2062A. $\overline{FLT}$ and ENOUT have 100V ratings and can sink 100µA to less than 800mV. TMR is brought out to a turret for the purpose of monitoring the waveform there. It may also be used to connect external timer capacitors.

Quick Start

Connect a 12V supply to INPUT, and connect a load to OUTPUT as shown in Figure 1. The circuit will turn on automatically when power is applied, and green LED1 will show that the output is up. LED3 indicates that input power is present. If the input voltage is increased above 25V, the output will shut off and LED1 will extinguish. The output will remain off until the input is brought below 20V. Similarly, if the input voltage is decreased to less than 4V the output will shut off and LED1 will extinguish. It will restart when the input rises above 5V.

QUICK START PROCEDURE

To test ISO-7637-2 compliance, apply a transient to the input as shown in Figure 2. Use a storage oscilloscope to monitor both the input and the output, and use the NSG5500 trigger output to trigger the oscilloscope sweep. The expected output to ISO7637-2 load dump pulse 5 is shown in Figure 3.

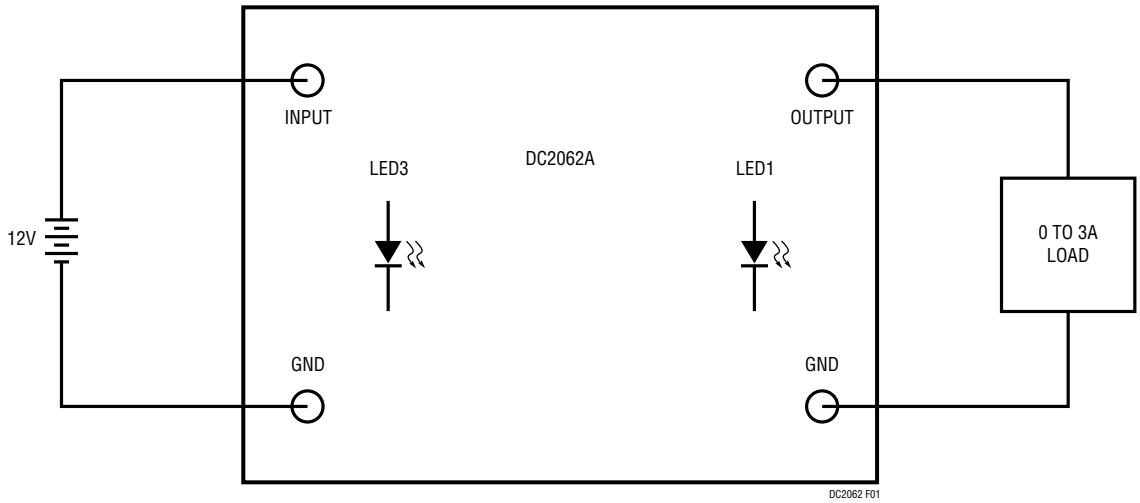


Figure 1: Basic Test Setup

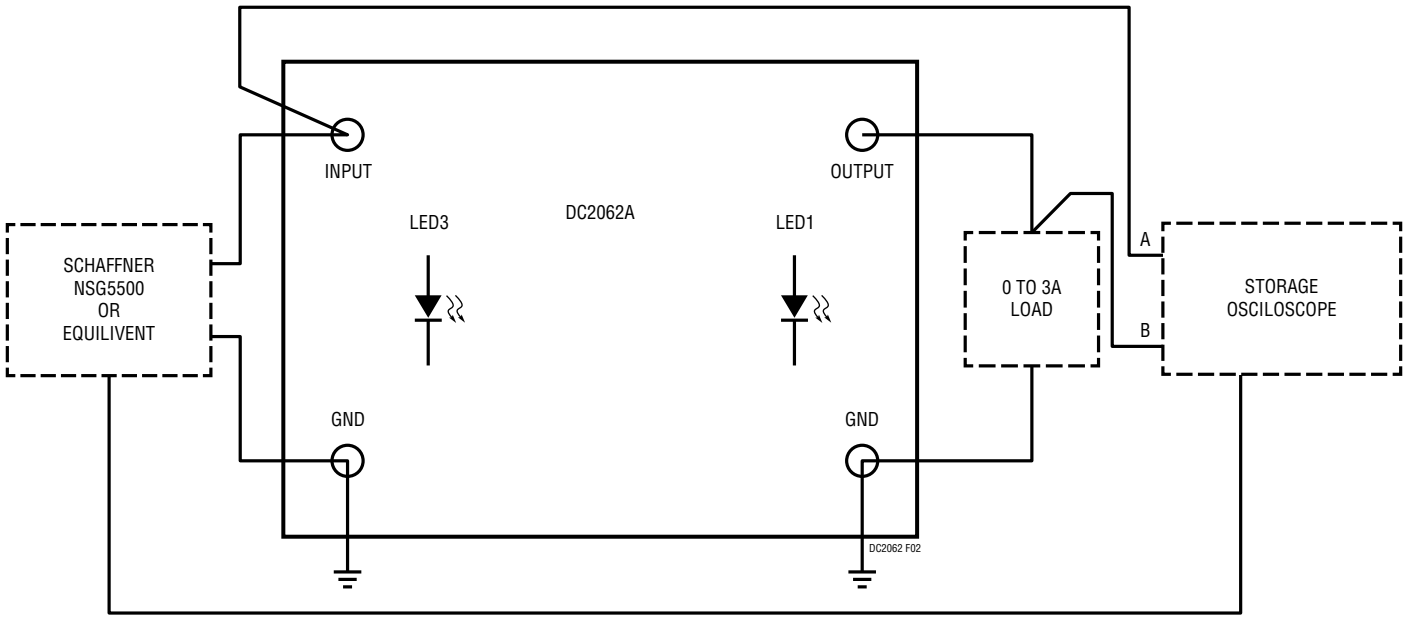


Figure 2: Testing ISO-7637-2 Transients.

QUICK START PROCEDURE

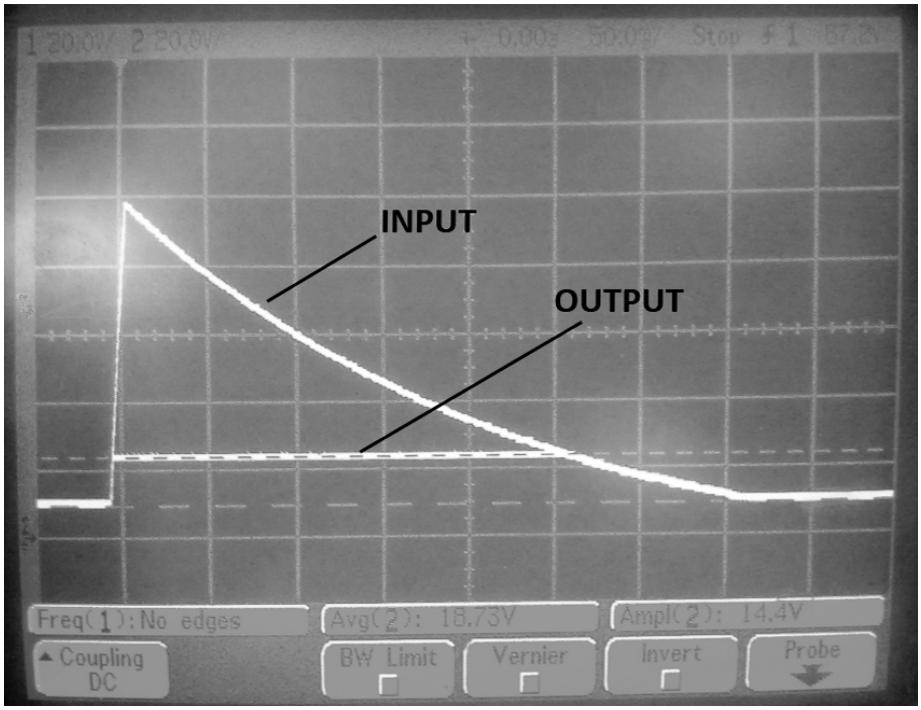


Figure 3: ISO-7637-2 Load Dump Event

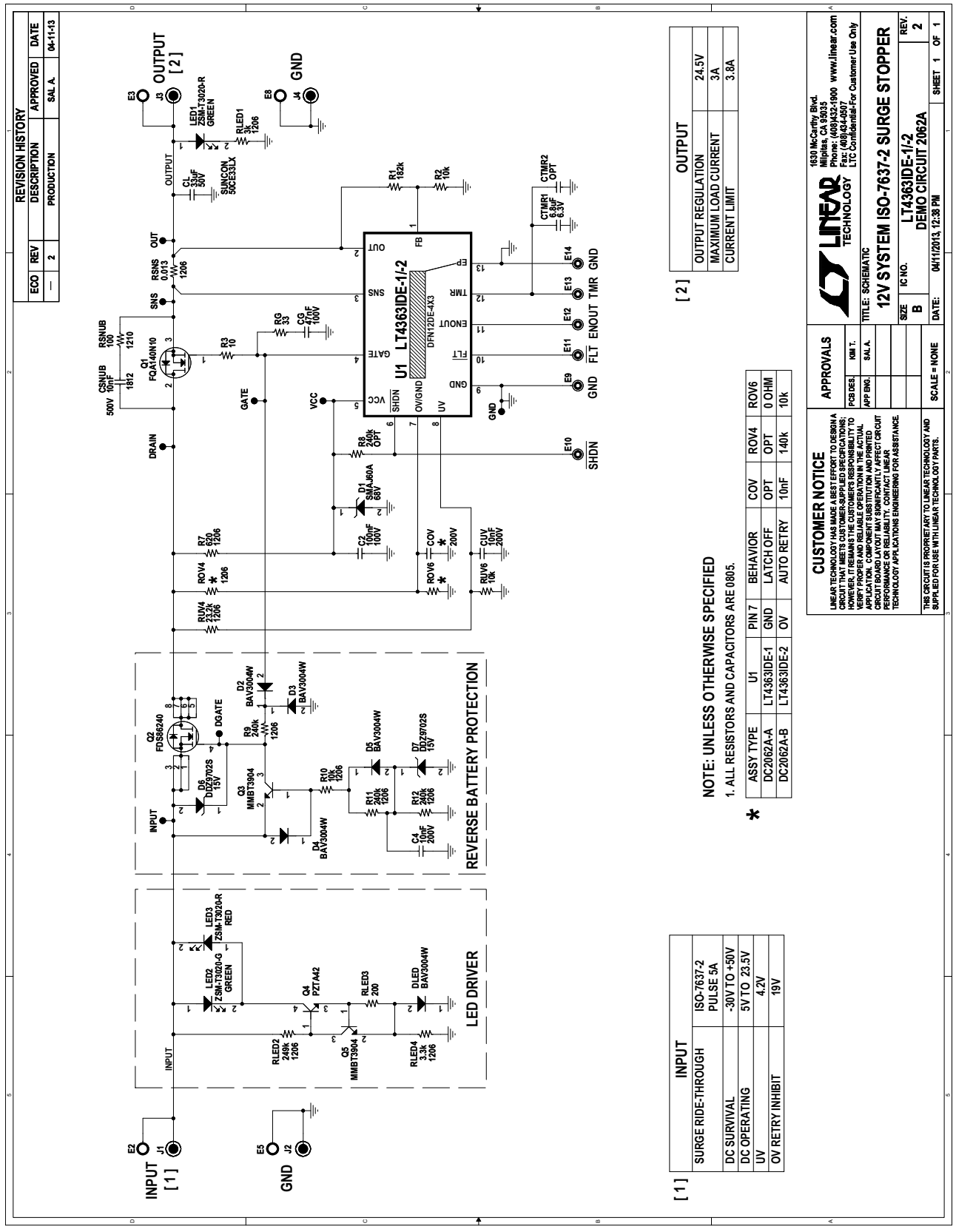
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CG	CAP., X7R, 47nF, 100V, 20%, 0805	AVX, 08051C473MAT2A
2	1	CL	CAP., ALUM., 33µF, 50V, 20%, SMT	SUN ELECT., 50CE33LX
3	1	CSNUB	CAP., X5R, 10nF, 500V, 20%, 1812	AVX, 18127C103MAT2A
4	1	CTMR1	CAP., X5R, 6.8µF, 6.3V, 20%, 0805	TDK C2012X5R0J685M
5	0	CTMR2	CAP., X7R, 4.7µF, 100V, 20%, 0805	OPT
6	1	C2	CAP., X7R, 100nF, 100V, 20%, 0805	AVX, 08051C104MAT2A
7	2	C4,CUV	CAP., X7R, 10nF, 200V, 20%, 0805	AVX, 08052C103MAT2A
8	5	D2, D3, D4, D5, DLED	DIODE, CURRENT LIMITING, SOD123	DIODES INC, BAV3004W
9	1	D1	DIODE, TVS, 60V, SMA-DIODE	DIODES INC, SMAJ60A-13-F
10	2	D6, D7	DIODE, ZENER 15V, SOD323	DIODES INC, DDZ9702S
11	4	E2, E3, E5, E8	TP, TURRET, .094"	MILL-MAX, 2501-2-00-80-00-00-07-0
12	6	E9, E10, E11, E12, E13, E14	TP, TURRET, .064"	MILL-MAX, 2308-2-00-80-00-00-07-0
13	4	J1, J2, J3, J4	BANANA JACK, NON-INSULATED	KEYSTONE, 575-4
14	2	LED1, LED2	LED, SMT GREEN, LED-ROHM-SML-010	ROHM, SML-010FT

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
15	1	LED3	LED, SMT RED, LED-ROHM-SML-010	ROHM, SML-010VT
16	1	Q1	MOSFET, N-CH,100V, TO-3PN	FAIRCHILD, FQA140N10
17	1	Q2	MOSFET, N-CH,150V, SO8	FAIRCHILD, FDS86240
18	2	Q3, Q5	XTOR, NPN, 40V, SOT23	DIODES INC., MMBT3904-7-F
19	1	Q4	XTOR, NPN, 300V, SOT223	FAIRCHILD, PZTA42
20	1	RG	RES., CHIP, 33Ω, 1/8W, 5% 0805	NIC, NRC10J330TRF
21	1	RLED1	RES., CHIP, 3kΩ 1/4W, 5% 1206	NIC, NRC12J302TR10F
22	1	RLED2	RES., CHIP, 249k, 1/4W, 1%, 1206	NIC, NRC12F2493TRF
23	1	RLED3	RES., CHIP, 200, 1/8W, 5%, 0805	NIC, NRC10J201TRF
24	1	RLED4	RES., CHIP, 3.3k, 1/4W, 5%, 1206	NIC, NRC12J332TRF
25	2	R2, RUV6	RES., CHIP, 10k, 1/4W, 1%, 0805	NIC, NRC10F1002TRF
26	1	RSNS	RES., CHIP, SENSE, 0.013Ω, 1/4W, 5%, 1206	NIC, NCST12JR013JTRF
27	1	RSNUB	RES., CHIP, 100Ω, 1/2W, 5%, 1210, PULSE PROOF	NIC, NRCP25J101TRF
			ALTERNATE PART NUMBER FOR RSNUB (3/4W PART)	VISHAY, CRCW1210100RJNEAHP
28	1	RUV4	RES., CHIP, 23.2kΩ, 1/4W, 1%, 1206	NIC, NRC12F2322TRF
29	1	R1	RES., CHIP, 182k, 1/8W, 1%, 0805	NIC, NRC10F1823TRF
30	1	R3	RES., CHIP, 10Ω, 1/8W, 5% 0805	NIC, NRC10J100TRF
31	1	R7	RES., CHIP, 620, 1/4W, 5%, 1206 PULSE PROOF (FOR PROD ASSY)	VISHAY, CRCW1206620RJNEAIF
32	0	R8	RES., CHIP, 240k, 1/8W, 5%, 0805	OPT
33	3	R9, R11, R12	RES., CHIP, 240k, 1/4W, 5%, 1206	NIC, NRC12J244TRF
34	1	R10	RES., CHIP, 10kΩ, 1/4W, 5%, 1206, PULSE PROOF	VISHAY, CRCW120610K0JNEAIF
35	4		STANDOFF, NYLON 0.5"	KEYSTONE, 8833 (SNAP ON)
DC2062A-A				
1	0	COV	CAP., 0805	OPT
2	0	ROV4	RES., 1%, 1206	OPT
3	1	ROV6	RES., CHIP, 0Ω, 0805	VISHAY, CRCW08050000Z0EA
4	1	U1	I.C., LT4363IDE-1, DFN12DE-4X3	LINEAR TECH., LT4363IDE-1
DC2062A-B				
1	1	COV	CAP., X7R, 10nF, 200V 20%, 0805	AVX, 08052C103MAT2A
2	1	ROV4	RES., CHIP, 140K, 1/4W, 1%, 1206	NIC, NRC12F1403TRF
3	1	ROV6	RES., CHIP, 10K, 1/4W, 1%, 0805	NIC, NRC10F1002TRF
4	1	U1	I.C., LT4363IDE-2, DFN12DE-4X3	LINEAR TECH., LT4363IDE-2

SCHEMATIC DIAGRAM



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