Low Quiescent Current Surge Stopper

FEATURES

- **Low Quiescent Current: 8µA Operating**
- **Withstands Surge Voltage Up to the MOSFET Limit**
- **Wide Operating Voltage Range: 4V to 72V**
- **Overcurrent Protection**
- **Selectable Internal 31.5V/50V or Adjustable Gate Clamp Voltage**
- Reverse Input Protection to –60V
- Adjustable Turn-On Threshold
- Adjustable Fault Timer with MOSFET Stress Acceleration
- Controls N-Channel MOSFET
- Latchoff and Retry Options
- Low Retry Duty Cycle During Faults
- 10-Pin DFN (3mm × 3mm) and MSOP Packages

APPLICATIONS

- Automotive/Avionic/Industrial Surge Protection
- Hot Swap, Live Insertion
- High Side Switch for Battery Powered Systems
- Automotive Load Dump Protection

DESCRIPTION

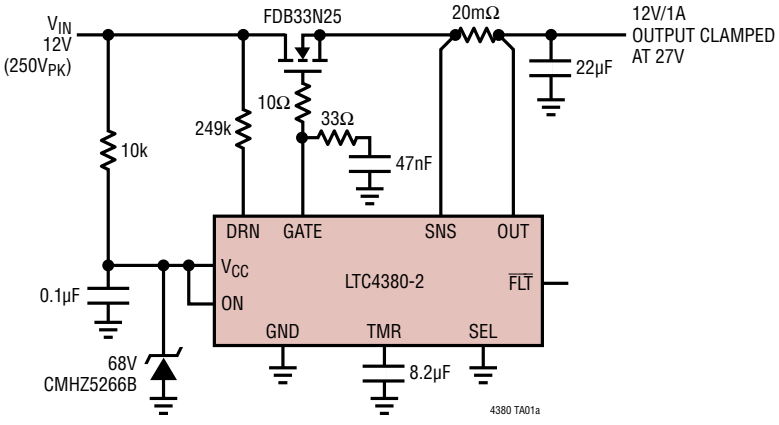
The LTC®4380 low quiescent current surge stopper protects loads from high voltage transients. Overvoltage protection is provided by clamping the gate voltage of an external N-channel MOSFET to limit the output voltage to a safe value during overvoltage events such as load dump in automobiles. Fixed gate clamp voltages are selectable for 12V and 24V/28V systems. For systems of any voltage up to 72V, use the adjustable gate clamp versions. Overcurrent protection is also provided.

An internal multiplier generates a TMR pin current proportional to V_{DS} and I_D, so that operating time in both overcurrent and overvoltage conditions is limited in accordance with MOSFET stress.

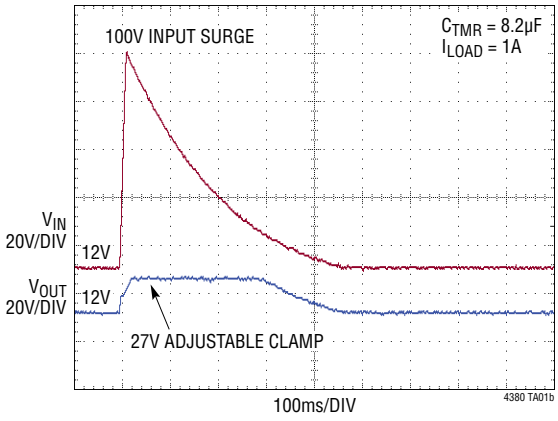
The GATE pin can drive back-to-back MOSFETs for reverse input protection, eliminating the voltage drop and dissipation of a Schottky diode solution. A low 8µA operating current permits use in always-on and battery powered applications. An accurate ON pin comparator monitors the input supply for undervoltage (UV) conditions and also serves as a shutdown input, reducing the quiescent current to 6µA.

TYPICAL APPLICATION

12V, 1A with 250V Overvoltage Protection



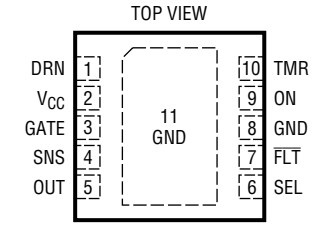
Surge Stopper Limits Output to 27V During Input Surge



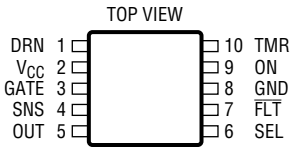
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

V_{CC}, ON, SEL ..... –60V to 80V
DRN (Note 3), SNS, OUT
  LTC4380-1/LTC4380-2 ..... –0.3V to 53V
  LTC4380-3/LTC4380-4 ..... –0.3V to 80V
SNS to OUT ..... –5V to 5V
GATE (Note 4)
  LTC4380-1/LTC4380-2 ..... –0.3V to 53V
  LTC4380-3/LTC4380-4 ..... –0.3V to 86V
GATE to OUT, GATE to V_{CC} (Note 4) ..... –0.3V to 10V
TMR ..... –0.3V to 5V
$\overline{FLT}$ ..... –0.3V to 80V
I_{DRN} 2.5mA
Operating Ambient Temperature Range
  LTC4380C ..... 0°C to 70°C
  LTC4380I ..... –40°C to 85°C
  LTC4380H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
  MSOP ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 135°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, PCB CONNECTION OPTIONAL



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 160°C/W

ORDER INFORMATION http://www.linear.com/product/LTC4380#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4380CDD-1#PBF	LTC4380CDD-1#TRPBF	LGHQ	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4380IDD-1#PBF	LTC4380IDD-1#TRPBF	LGHQ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4380HDD-1#PBF	LTC4380HDD-1#TRPBF	LGHQ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4380CMS-1#PBF	LTC4380CMS-1#TRPBF	LTGHR	10-Lead Plastic MSOP	0°C to 70°C
LTC4380IMS-1#PBF	LTC4380IMS-1#TRPBF	LTGHR	10-Lead Plastic MSOP	–40°C to 85°C
LTC4380HMS-1#PBF	LTC4380HMS-1#TRPBF	LTGHR	10-Lead Plastic MSOP	–40°C to 125°C
LTC4380CDD-2#PBF	LTC4380CDD-2#TRPBF	LGHS	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4380IDD-2#PBF	LTC4380IDD-2#TRPBF	LGHS	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4380HDD-2#PBF	LTC4380HDD-2#TRPBF	LGHS	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4380CMS-2#PBF	LTC4380CMS-2#TRPBF	LTGHT	10-Lead Plastic MSOP	0°C to 70°C
LTC4380IMS-2#PBF	LTC4380IMS-2#TRPBF	LTGHT	10-Lead Plastic MSOP	–40°C to 85°C
LTC4380HMS-2#PBF	LTC4380HMS-2#TRPBF	LTGHT	10-Lead Plastic MSOP	–40°C to 125°C
LTC4380CDD-3#PBF	LTC4380CDD-3#TRPBF	LGXZ	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4380IDD-3#PBF	LTC4380IDD-3#TRPBF	LGXZ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4380HDD-3#PBF	LTC4380HDD-3#TRPBF	LGXZ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4380CMS-3#PBF	LTC4380CMS-3#TRPBF	LTGYD	10-Lead Plastic MSOP	0°C to 70°C
LTC4380IMS-3#PBF	LTC4380IMS-3#TRPBF	LTGYD	10-Lead Plastic MSOP	–40°C to 85°C
LTC4380HMS-3#PBF	LTC4380HMS-3#TRPBF	LTGYD	10-Lead Plastic MSOP	–40°C to 125°C
LTC4380CDD-4#PBF	LTC4380CDD-4#TRPBF	LGYC	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4380IDD-4#PBF	LTC4380IDD-4#TRPBF	LGYC	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4380HDD-4#PBF	LTC4380HDD-4#TRPBF	LGYC	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4380CMS-4#PBF	LTC4380CMS-4#TRPBF	LTGYF	10-Lead Plastic MSOP	0°C to 70°C
LTC4380IMS-4#PBF	LTC4380IMS-4#TRPBF	LTGYF	10-Lead Plastic MSOP	–40°C to 85°C
LTC4380HMS-4#PBF	LTC4380HMS-4#TRPBF	LTGYF	10-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = OUT = SNS = DRN = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
V_{CC}	Operating Voltage Range	LTC4380-1/LTC4380-2	●	4		80	V
		LTC4380-3/LTC4380-4 (Note 6)	●	4		72	V
V_{OUT}	Operating Voltage Range		●			72	V
I_Q	Total Supply Current (Note 5)				8	11	µA
		C-Grade and I-Grade	●			12	µA
		H-Grade	●			20	µA
		V_{CC} = OUT = SNS = DRN = 4V			22	28	µA
			●			35	µA
I_{CC}	V_{CC} Current, Shutdown	ON = OUT = SNS = 0V	●		6	10	µA
	V_{CC} Current				7	9	µA
			●			12	µA
		V_{CC} = OUT = SNS = DRN = 4V			20	25	µA
			●			30	µA
I_{SNS}	SNS Current		●		0.5	1.4	µA
I_{OUT}	OUT Current		●		1.5	5.5	µA
	OUT Current, Shutdown	C-Grade and I-Grade	●		5	12	µA
		H-Grade	●			80	µA
I_R	Reverse Input Current	V_{CC} = –60V, ON Open, SEL = 0V	●		–0.4	–2	mA
		V_{CC} = ON = SEL = –60V	●		–1.2	–5	mA
Gate Drive							
ΔV_{GATE}	GATE Drive (GATE – OUT)	SEL = SNS = OUT = V_{CC} =12V					
		8V ≤ V_{CC} ≤ 30V; I_{GATE} = –1µA, 0µA	●	10	11.5	14	V
		V_{CC} = 4V; I_{GATE} = –1µA, 0µA	●	5		8	V
ΔV_{CLAMP}	GATE Clamp to V_{CC} (GATE – V_{CC})	SNS = OUT = 20V, I_{GATE} = 0µA	●	12	13.5	14.5	V
V_{GATE}	GATE Clamp to GND	V_{CC} = 30V, SEL = 0V (LTC4380-1/LTC4380-2)	●	30	31.5	33	V
		V_{CC} = 60V, SEL = V_{CC} (LTC4380-1/LTC4380-2)	●	47.5	50	52.5	V
$I_{GATE(UP)}$	GATE Pull-Up Current	V_{CC} = GATE = OUT = 12V, SEL = 0V	●	–10	–20	–30	µA
		V_{CC} = GATE = OUT = 24V, SEL = V_{CC}	●	–12	–25	–35	µA
$I_{GATE(DN)}$	GATE Pull-Down Current						
	Overcurrent	ΔV_{SNS} = 200mV, GATE = 12V, OUT = 0V	●	50	100		mA
	Shutdown	ON = 0V, GATE = 20V	●	0.3	5		mA
	Input UV	V_{CC} = 3.5V, GATE = 10V	●	2	5		mA
	Fault Time Out	TMR = 2V, GATE = 10V	●	1.5	3.5		mA
Current Limit							
ΔV_{SNS}	Current Limit Sense Voltage (SNS – OUT)	V_{CC} = 12V, 24V, OUT = 6V, 12V	●	45	50	55	mV
		V_{CC} = 12V, 24V, OUT = 0V	●	42	62	95	mV
$t_{OFF(OC)}$	Overcurrent Turn-Off Propagation Delay	ΔV_{SNS} Steps from 0V to 250mV, OUT = 6V	●		2	4	µs
		ΔV_{SNS} Steps from 0V to 250mV, OUT = 0V	●		2	4	µs
SEL, $\overline{FLT}$							
I_{SEL}	SEL Input Current	SEL = 0V to 80V	●			±0.1	µA
V_{SEL}	SEL Input Threshold		●	0.4		3	V
$I_{\overline{FLT}}$	$\overline{FLT}$ Leakage Current	$\overline{FLT}$ = 80V	●			2	µA
$V_{\overline{FLT}(LOW)}$	$\overline{FLT}$ Output Low	I_{SINK} = 0.1mA	●		0.1	0.5	V
		I_{SINK} = 3mA	●		1	4	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = OUT = SNS = DRN = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TMR, DRN							
ΔV_{DRN}	DRN Voltage (DRN – OUT)	I_{DRN} = 0.1mA, OUT = SNS = 12V	●	0.7	1.5	2.5	V
$V_{DS(MAX)}$	Overvoltage V_{DS} Threshold (DRN – OUT)	TMR = 0.8V, I_{DRN} = 2µA SNS = OUT = 12V	 ●	0.6 0.3	0.7	0.8 1.0	V V
$I_{TMR(DN)}$	TMR Pull-Down Current	TMR = 0.8V	●	1.25	2	2.75	µA
$I_{TMR(UP,COOL)}$	TMR Pull-Up Current, Cool Down	TMR = 2V	●	–1	–2	–3	µA
$I_{TMR(UP)}$	TMR Pull-Up Current, Overvoltage	TMR = 0.8V, OUT = 11V, I_{DRN} = 5µA, ΔV_{SNS} = 0mV	●	–0.8	–1.6	–2.4	µA
		OUT = 28V, TMR = 0.8V					
	Small OV, Light Load High OV, Light Load	I_{DRN} = 0.1mA, ΔV_{SNS} = 10mV I_{DRN} = 1mA, ΔV_{SNS} = 10mV	● ●	–3.5 –13	–6.7 –30	–11.6 –61	µA µA
	Small OV, Heavy Load High OV, Heavy Load	I_{DRN} = 0.1mA, ΔV_{SNS} = 40mV I_{DRN} = 1mA, ΔV_{SNS} = 40mV	● ●	–10 –60	–20 –120	–30 –180	µA µA
	TMR Pull-Up Current, Overcurrent	TMR = 0.8V					
		I_{DRN} = 0mA, OUT = 11V I_{DRN} = 0mA, OUT = 0V	● ●	–4 –17	–6 –27	–9 –34	µA µA
	Small OV, Light Load High OV, Light Load	I_{DRN} = 0.1mA, OUT = 11V I_{DRN} = 1mA, OUT = 11V	● ●	–16 –80	–27 –142	–38 –200	µA µA
	Small OV, Heavy Load High OV, Heavy Load	I_{DRN} = 0.1mA, OUT = 0V I_{DRN} = 1mA, OUT = 0V	● ●	–35 –130	–50 –170	–60 –220	µA µA
$V_{TMR(F)}$	TMR Gate Off Threshold	TMR Rising	●	1.178	1.215	1.251	V
D	Retry Duty Cycle; Overvoltage, LTC4380-2/LTC4380-4	ΔV_{SNS} = 40mV, I_{DRN} = 5µA, OUT = 28V, V_{CC} = 29V	●		2.8	3.5	%
		ΔV_{SNS} = 40mV, I_{DRN} = 500µA, OUT = 28V, V_{CC} = 80V	●		0.1	0.2	%
	Retry Duty Cycle; Overcurrent, LTC4380-2/LTC4380-4	I_{DRN} = 500µA					
		OUT = 0V, V_{CC} = 14V OUT = 6V, V_{CC} = 14V	● ●		0.1 0.35	0.2 0.7	% %
ON							
I_{ON}	ON Input Current	V_{ON} = 1V	●	–1	–2		µA
V_{ON}	ON Input Threshold	ON Rising	●	0.99	1.05	1.1	V
$V_{ON(HYST)}$	ON Input Hysteresis				45		mV
$t_{ON(ON)}$	Turn-On Propagation Delay	ON Steps from 0V to 1.5V, OUT = SNS = 0V	●		5	25	ms
$t_{OFF(ON)}$	Turn-Off Propagation Delay	ON Steps from 1.5V to 0V, OUT = SNS = V_{CC}	●		1	5	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: Internal clamps limit the DRN pin to a minimum of 10V above the OUT and SNS pins.

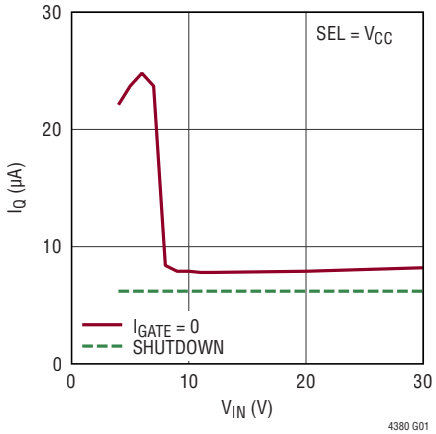
Note 4: Internal clamps limit the GATE pin to a minimum of 10V above the OUT pin or V_{CC} pin, or 50V (SEL = V_{CC}) or 31.5V (SEL = GND) above the GND pin (LTC4380-1/LTC4380-2). Driving this pin to voltages beyond the clamp may damage the device.

Note 5: Total supply current is the sum of the current into the V_{CC}, OUT, SNS and DRN pins.

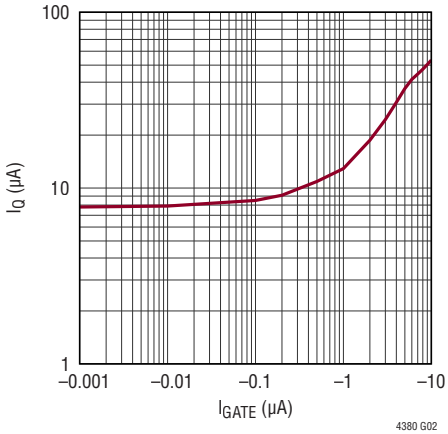
Note 6: Operating voltage is limited by the maximum GATE voltage of 86V.

TYPICAL PERFORMANCE CHARACTERISTICS V_{CC} = 12V, unless otherwise noted.

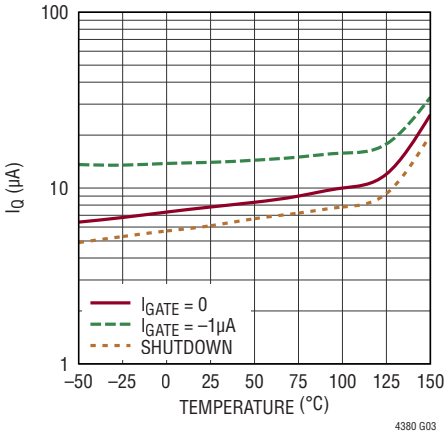
Total Supply Current (I_Q) vs Input Voltage



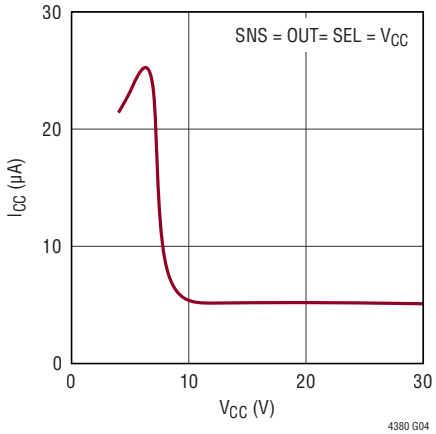
Total Supply Current (I_Q) vs Gate Leakage



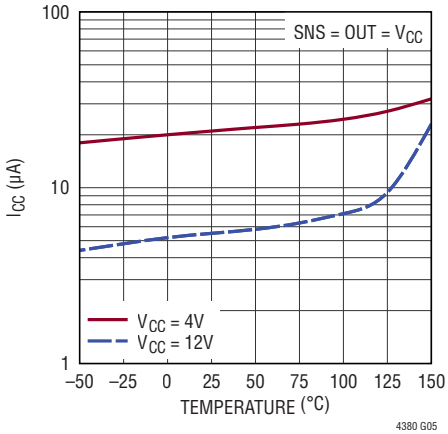
Total Supply Current (I_Q) vs Temperature



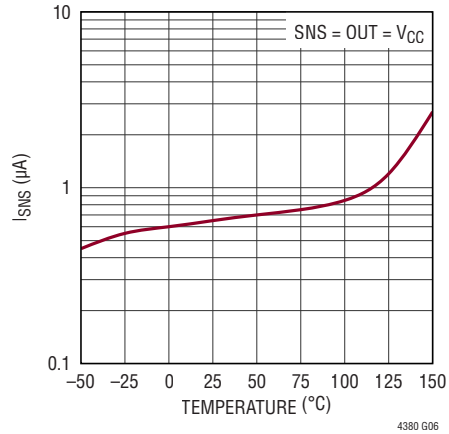
Supply Current (I_{CC}) vs Supply Voltage



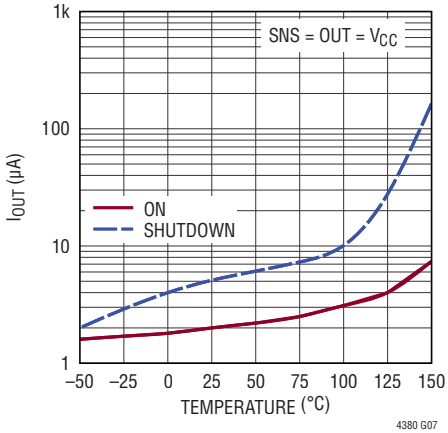
Supply Current (I_{CC}) vs Temperature



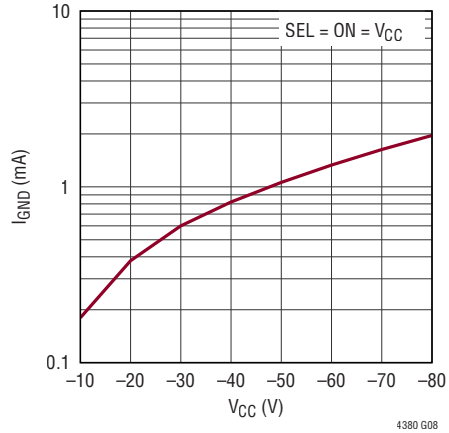
I_{SNS} vs Temperature



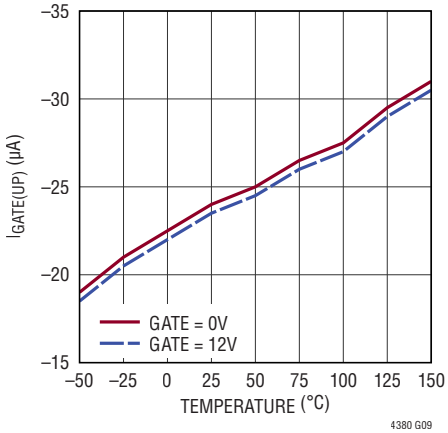
Output Pin Current vs Temperature



Reverse Current vs Reverse Voltage

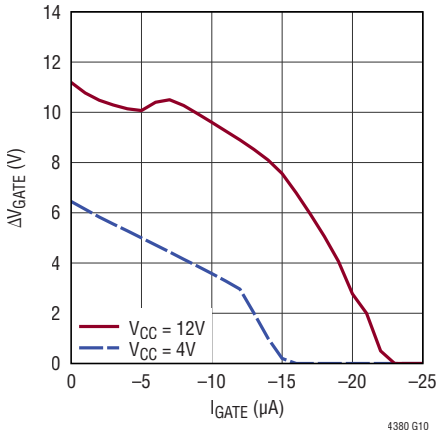


Gate Pull Up Current vs Temperature

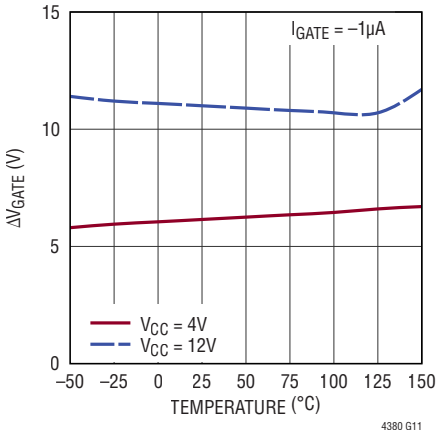


TYPICAL PERFORMANCE CHARACTERISTICS V_{CC} = 12V, unless otherwise noted.

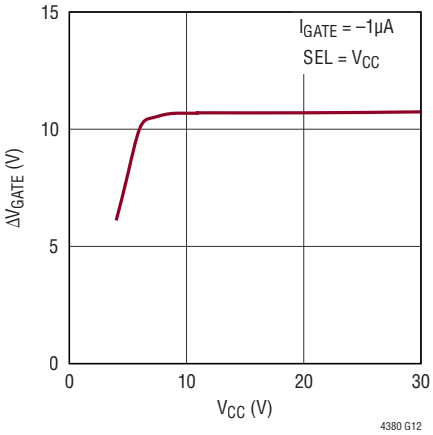
Gate Drive vs Gate Current



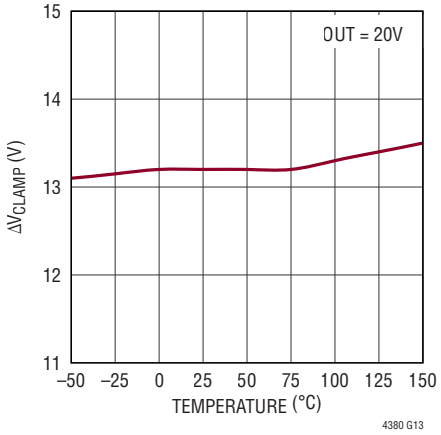
Gate Drive vs Temperature



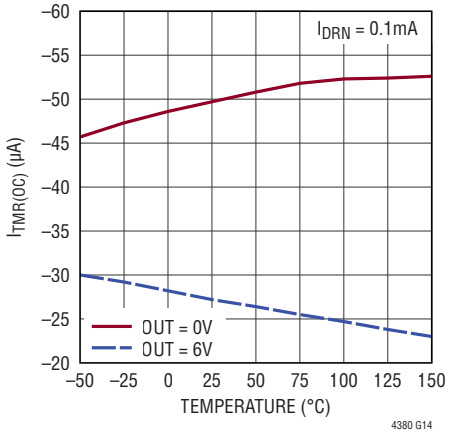
Gate Drive vs Supply Voltage



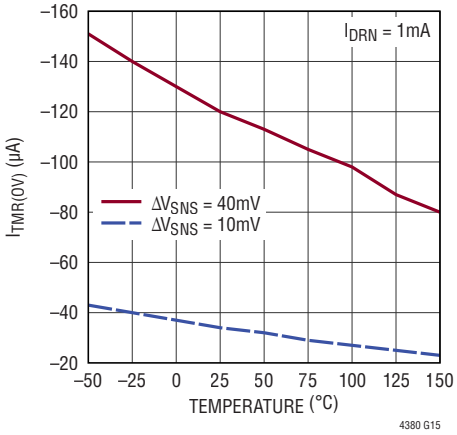
Gate Clamp to V_{CC} vs Temperature



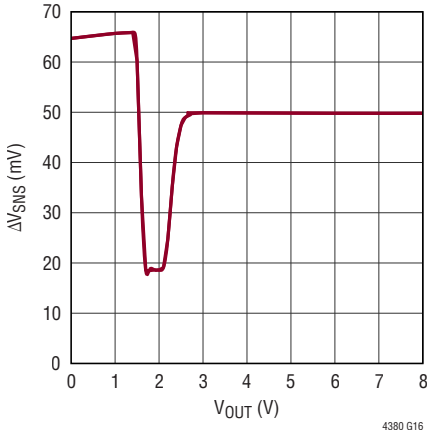
TMR Pin Current vs Temperature, Overcurrent Fault



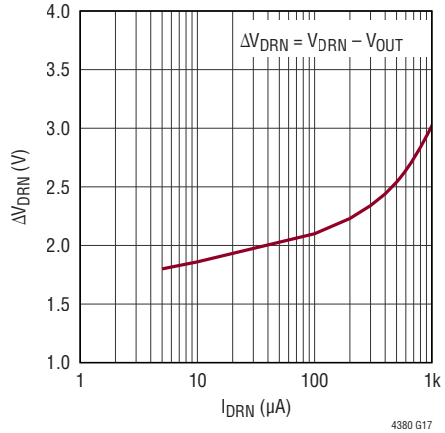
TMR Pin Current vs Temperature, Overvoltage Fault



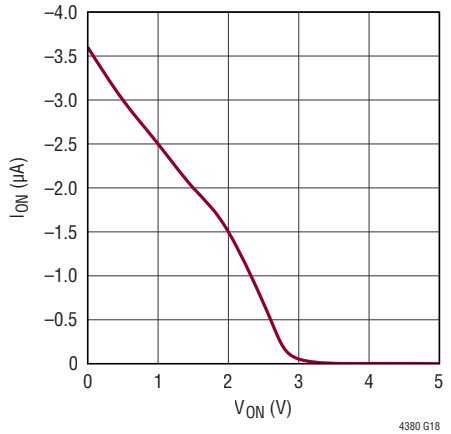
Current Limit vs Output Voltage



DRN Voltage vs Current



ON Pin Current vs Voltage



PIN FUNCTIONS

DRN: External MOSFET Drain-Source Sense. The DRN pin voltage tracks the OUT pin. The resulting DRN pin current through external resistor R_{DRN} is proportional to the external MOSFET V_{DS}. The DRN pin current and ΔV_{SNS} (SNS – OUT) are multiplied internally to produce a TMR pin current approximately proportional to the MOSFET's power dissipation. This reduces the SOA requirement of the MOSFET by timing out faster during more severe faults. Choose R_{DRN} to limit the current to 1mA at the peak input voltage. Connect to OUT if unused.

Exposed Pad: Exposed Pad. May be left open or connected to device ground (GND).

$\overline{FLT}$: Fault Output. This open drain logic output pin pulls low after the voltage at the TMR pin has reached the fault threshold of 1.215V. It indicates that the MOSFET is off because either the supply voltage has stayed at an elevated level for an extended period of time (voltage fault) or the device is in an overcurrent condition (current fault). The fault output is capable of sinking up to 3mA. Leave open or tie to GND if unused.

GATE: Gate Drive for N-Channel MOSFET. The GATE pin is pulled up by an internal 20µA charge pump that is regulated to 11.5V above the OUT pin. An amplifier controls the GATE pin to limit the current through the MOSFET. The GATE pin is clamped during an overvoltage event, thus indirectly limiting the output voltage. The clamp voltage is set to 31.5V with SEL = 0V, or 50V when SEL = V_{CC} for the fixed voltage versions, LTC4380-1/LTC4380-2. The LTC4380-3 and LTC4380-4 are adjustable versions without the internal gate clamp. The voltage at the GATE pin is limited to 13.5V above V_{CC} when not in regulation mode. A minimum of 47nF of capacitance and 33Ω series resistor at the pin is necessary to compensate the current limit amplifier. To avoid damaging the external MOSFET during an output short, GATE is also clamped internally to 17V above OUT.

GND: Device Ground.

ON: Turn-On Control Input. The LTC4380 can be turned on by pulling this pin above 1.05V or by leaving it open to allow an internal 1MΩ resistor to turn the part on. Pulling the pin below the threshold puts the part in shutdown mode and reduces the supply current to 6µA. Limit the ON to ground leakage current to less than 1µA if no external pull-up is used. The ON pin can be pulled up to 80V or below GND by 60V without damage.

OUT: Output Voltage Sense. This pin senses the output voltage at the output terminal of the current sense resistor. An internal clamp limits the voltage in between the GATE and OUT pins to 17V. Bypass the OUT pin with a minimum of 22µF as close to the pin as possible.

SEL: Gate Clamp Voltage Select for LTC4380-1 and LTC4380-2. Connect the SEL pin to GND to set the internal gate clamp voltage to 31.5V. Connect it to V_{CC} or OUT for a 50V gate clamp voltage. The SEL pin can be pulled up to 80V or below GND by 60V without damage. Connect SEL to GND for LTC4380-3 and LTC4380-4.

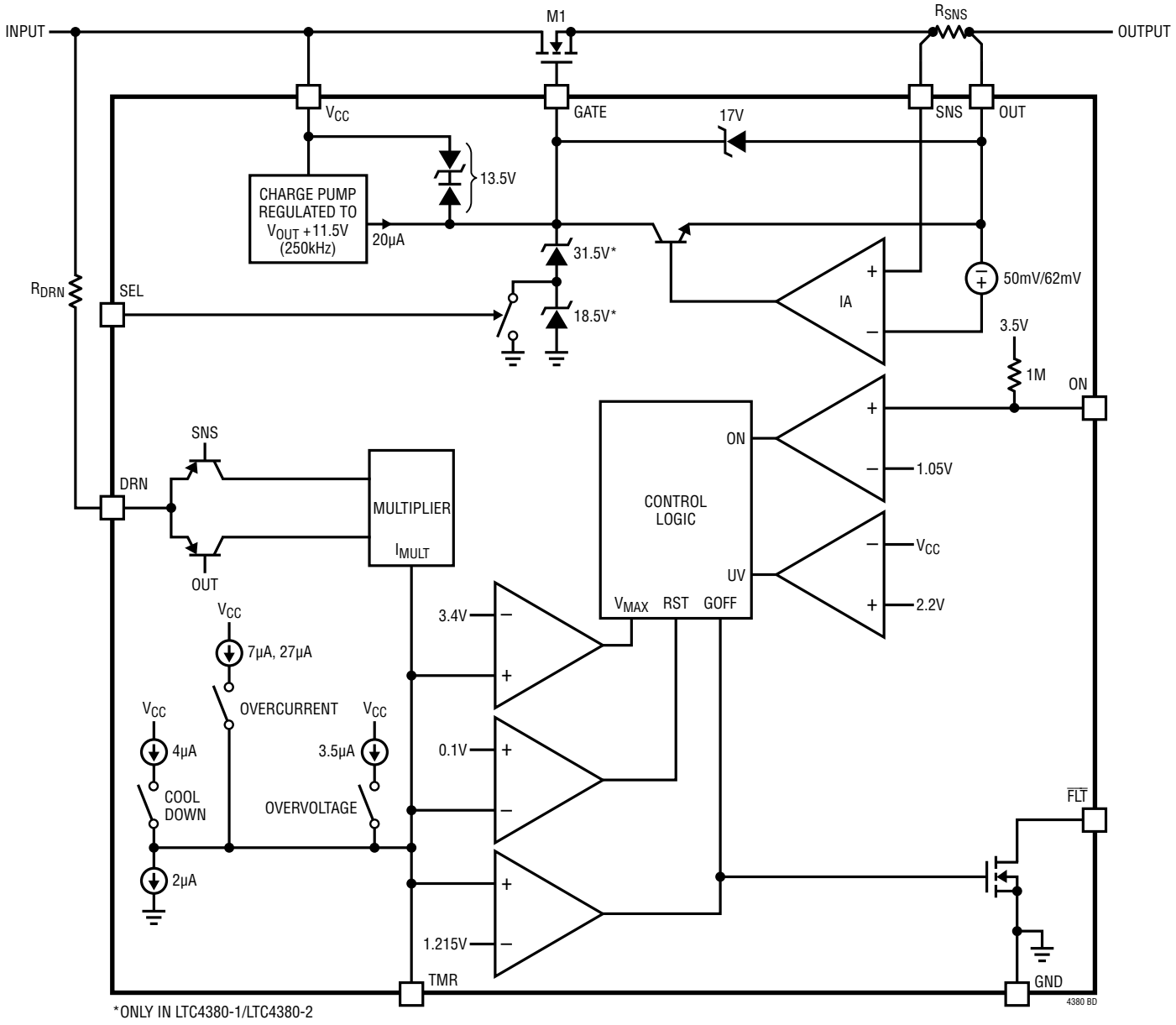
SNS: Current Sense Input. Connect to the input terminal of the current sense resistor. The current limit amplifier controls the GATE pin to limit the current sense voltage to 50mV. This voltage increases to 62mV in a severe fault when OUT is below 1.5V. A fixed 7µA is added to the TMR pin current during an overcurrent condition to shorten the turn-off time. In a severe short condition when the output voltage is below 1.5V, the extra current increases to 27µA to reduce the power dissipation in the MOSFET. ΔV_{SNS} (SNS – OUT) must be limited to less than ±5V. Connect to OUT if unused.

PIN FUNCTIONS

TMR: Fault Timer Input. Connect a capacitor between this pin and ground to set the fault turn-off time and cool down period. The charging current during fault conditions varies depending on the power dissipation of the MOSFET. When TMR reaches 1.215V, the MOSFET turns off and $\overline{FLT}$ pulls low. Upon gate off, the part immediately enters a cool down period with a 2µA current pull up and pull down on the TMR pin. After the cool down period has concluded, the LTC4380-2 and LTC4380-4 immediately restart, while the LTC4380-1and LTC4380-3 remain off until the ON pin is pulled low momentarily for more than 100µs or power is cycled. A 10V rated X7R capacitor is recommended for C_{TMR}.

V_{CC}: Positive Supply Voltage Input. The positive supply input ranges from 4V to 80V for normal operation. It can go below ground by up to 60V during a reverse battery condition, without damaging the part. For applications where the input voltage is expected to exceed 80V, the V_{CC} pin may be protected by a Zener diode clamp or, in the case of short duration spikes, by a simple RC filter. Clamping the V_{CC} pin with a Zener diode can also be used as a means of adjusting the GATE pin clamp voltage to a value less than the internal 31.5V or 50V clamps for the LTC4380-1/LTC4380-2. For the adjustable versions, LTC4380-3/LTC4380-4, which have no internal gate clamp, a Zener diode at the V_{CC} pin is the only way to limit the voltage at the GATE pin.

BLOCK DIAGRAM



OPERATION

The LTC4380 is a low quiescent current surge stopper that drives an external N-channel MOSFET as the pass device. In normal operation, a 20µA charge pump (see Block Diagram) drives the MOSFET (M1) high, turning it fully on and providing a low impedance path from input to the load. The MOSFET gate is clamped to ground by a Zener stack. If the input voltage rises to the point where the output approaches the gate clamp, the output is effectively limited to one threshold voltage below the gate clamp and the input surge is blocked from reaching the load.

For the LTC4380-1 and LTC4380-2 versions, two internal gate clamping voltages to ground are available: 31.5V, which limits the output to about 27V for use in 12V systems, and 50V, which limits the output to about 45V for use in 24V and 28V systems. The clamping voltage is selectable using the SEL pin. Besides the gate to ground clamp, the GATE pin is also limited to 13.5V above the V_{CC} pin voltage.

There is no internal gate clamp to ground for the LTC4380-3 and LTC4380-4 versions and the GATE pin is only limited to 13.5V above the voltage at the V_{CC} pin. A Zener diode clamp connected from the V_{CC} pin to ground thus clamps the voltages at both the V_{CC} and GATE pins during overvoltage events.

Load current is limited by a current limit amplifier (IA), using a sense resistor in series with the MOSFET source to monitor the current. The current limit threshold is 50mV rising to 62mV when the output is less than 1.5V.

MOSFET stress is monitored by a timer, whose current is a function of M1's V_{DS} as well as I_D. V_{DS} is monitored by R_{DRN} at the DRN pin, while I_D is monitored by sensing the voltage drop across R_{SNS}. The timer allows the load to continue functioning during short transient events while protecting the MOSFET from being damaged by a sustained overvoltage, such as load dump in vehicles, or an output overload or short circuit.

A multiplier sets the timer period depending on the power dissipation in the MOSFET. Higher power dissipation corresponds to a shorter timer period, helping to keep the MOSFET within its safe operating area (SOA).

The timer responds to stresses at start-up, during voltage limiting, and during current limiting. TMR pin current is integrated on timing capacitor C_{TMR} and if TMR charges to 1.215V, the MOSFET is turned off. At this point, the LTC4380-1 and LTC4380-3 latch off, and can be reset by cycling power or by pulling the ON pin low for at least 100µs. For the LTC4380-2 and LTC4380-4, the TMR pin enters a cool down phase, allowing time for the MOSFET temperature to equalize with its surroundings before automatically restarting. The TMR pin slowly charges up and down in between 3.4V and 1.215V for 15 times and discharges to ground at the last cycle. When the TMR pin has reached the 100mV threshold, the MOSFET is turned back on. The cool down interval can be curtailed by pulling the ON pin low for at least 10ms/µF of C_{TMR}.

In addition to resetting the timer, the ON pin is used for on/off control and for undervoltage detection. The ON pin threshold is 1.05V.

The open drain $\overline{FLT}$ pin pulls low whenever the timer is faulted off, and goes high again when reset by a power cycle, by pulling the ON pin low for at least 100µs or in the case of the LTC4380-2 and LTC4380-4, when the TMR pin discharges to 100mV.

Table 1. LTC4380 Options

LTC4380	GATE CLAMP	FAULT BEHAVIOR
–1	Internal 31.5V/50V to GND	Latchoff
–2	Internal 31.5V/50V to GND	Auto Retry
–3	Externally Adjustable	Latchoff
–4	Externally Adjustable	Auto Retry

APPLICATIONS INFORMATION

The LTC4380 limits the voltage and current delivered to the load during supply transient or output overload events. The N-channel MOSFET provides a low resistance path from the input to the load during normal operation, while in overvoltage conditions it limits the output to a threshold voltage below the clamped gate voltage. The total fault timer period is set to ride through short-duration faults, while longer events cause the output to shut off and protect the MOSFET from damage.

Startup

Figure 1 shows a 12V, 1A application which limits the output to approximately 27V. When power is first applied with $V_{CC} \geq 4V$ and ON ≥ 1.05V, there is a delay of about 5ms before the GATE pin begins charging C2 and M1's gate terminal with a fixed 20µA current source. M1, operating as a source follower, ramps the output up at a rate of $I_{GATE(UP)}/C2$. Inrush current in the load capacitance C_L is given by

$$I_{INRUSH} = I_{GATE(UP)} \bullet \frac{C_L}{C2}$$

where $I_{GATE(UP)}$ is typically 20µA.

Eventually, the GATE pin charges to the point where $V_{IN} \approx V_{OUT}$ and stops only when ΔV_{GATE} ($V_{GATE} - V_{OUT}$) reaches its regulation point of 11.5V, fully enhancing M1.

Overcurrent Fault Protection

The LTC4380 features an adjustable current limit that protects against short circuits and excessive load current. During an overcurrent event, the GATE pin is regulated to limit the current sense voltage across the SNS and OUT pins (ΔV_{SNS}) to 50mV when OUT is above 3V. In the case of a severe short at the output, where OUT is less than 1.5V, the current sense voltage is 62mV. Output current is thereby limited to $\Delta V_{SNS}/R_{SNS}$. Current limit may control the startup ramp rate in extreme cases, such as if C_L is unusually large or if current limit is set to an unusually low value, and artificially reduces C_L's inrush current below the value previously calculated.

Overvoltage Fault Protection

The LTC4380 limits the voltage at the output during an overvoltage at the input. For the LTC4380-1/LTC4380-2 illustrated in Figure 1, an internal clamp limits the GATE pin to either 31.5V or 50V, depending on the state of the SEL pin. With the SEL pin grounded as shown, the GATE pin is clamped at 31.5V. Assuming a threshold voltage of 5V for M1, this limits the output to approximately 26.5V. Tying the SEL pin high causes the GATE pin to clamp at 50V, and limits the output to approximately 45V.

The GATE pin may also be limited by the compliance of the internal 20µA current source, to V_{CC} + 13.5V. In the LTC4380-3/LTC4380-4 the GATE pin clamp is entirely disconnected, leaving only the V_{CC} + 13.5V compliance limit. This arrangement allows the GATE pin to be effectively clamped at any voltage from 18V to 86V, by clamping V_{CC} to between 4V and 72V.

V_{CC} Pin

The V_{CC} pin operating range extends from 4V to 80V. In the presence of an input overvoltage exceeding 80V, the V_{CC} pin must be protected by filtering or clamping. For short duration spikes and transients exceeding 80V, filtering is the most sensible means of protecting the V_{CC} pin. R1 and C1 provide filtering in Figure 1. Owing to the LTC4380's low I_{CC}, values up to 20k may be used for R1 without seriously impairing the lower end of the operating voltage range. For long duration surges such as automotive load dump, C1 becomes prohibitively large and Zener D1 is the most effective means of limiting the V_{CC} voltage. Using a 68V

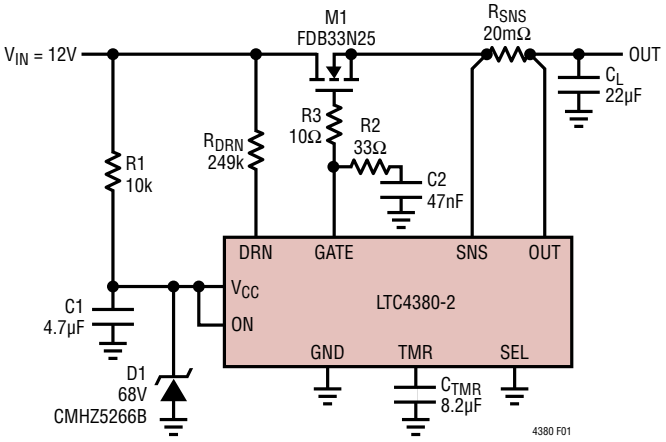


Figure 1. 12V/1A, Output Limited to 27V

APPLICATIONS INFORMATION

Zener assures that D1 will not override the internal GATE pin clamp in the LTC4380-1 and LTC4380-2 devices. For the LTC4380-3 and LTC4380-4, the V_{CC} operating range extends from 4V to 72V. Since the GATE pin is regulated to V_{OUT} + 11.5V, D1 is chosen to achieve the desired output clamping effect while at the same time keeping the V_{CC} pin within its 4V to 72V range.

Fault Timer Overview

Overvoltage and overcurrent conditions, and high V_{DS} conditions in M1 are limited in duration by an adjustable fault timer. A capacitor at the TMR pin (C_{TMR}) sets the delay time before a fault condition is reported at the $\overline{FLT}$ pin and M1 is turned off. C_{TMR} also sets the cool down time before M1 is permitted to turn back on for the LTC4380-2 and LTC4380-4 auto retry versions. The LTC4380-1 and LTC4380-3 versions simply latch off at the end of the timer delay. A 10V or higher rated X7R capacitor is recommended for C_{TMR} to minimize temperature and voltage sensitivity.

Fault timing starts as soon as the input power is applied with the part in the on condition, or when the part is turn on after application of power. A 1.5µA current is generated to pull up the TMR pin when the voltage across the MOSFET is higher than 0.7V. The timer speeds up with an additional current that varies with the power dissipated in the MOSFET, M1. The power dissipation is the product of the voltage across the MOSFET (V_{DS}) and the current flowing through it (I_D). V_{DS} is inferred from the voltage drop across the drain pin resistor, R_{DRN}, while ΔV_{SNS} represents I_D.

At initial power-up, the 1.5µA pilot current charges the TMR pin capacitor because the input supply is, at least for a short time, more than 0.7V above the output voltage. When the output rises to within 0.7V of the input supply voltage, the pull-up current disappears and an internal 2µA current source discharges the TMR pin capacitor. The capacitor must be sized to ride through the initial start-up interval for successful power-up.

In the presence of a sustained fault, the timer current charges the TMR pin to 1.215V. At this point the $\overline{FLT}$ pin pulls low to indicate a fault condition and the GATE pin pulls low, shutting off the MOSFET. After faulting off, the timer enters the cool down phase. At the end of the cool down period the LTC4380-1/LTC4380-3 remain off until manually reset, while the LTC4380-2/LTC4380-4 automatically restart.

Fault Timer Operation in Overvoltage

During an overvoltage condition, where the MOSFET's V_{DS} exceeds 0.7V, the TMR pin charges from 0V to 1.215V with a current that varies principally as a function of V_{DS} and I_D. V_{DS} is inferred from the current flowing in the DRN pin resistor, R_{DRN}, while the voltage difference between the SNS and OUT pins (ΔV_{SNS}) represents the MOSFET current, I_D.

The TMR pin current is given by

$$I_{TMR} = 1.5 \bullet 10^{-6}A + 0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet \Delta V_{SNS} \bullet \sqrt{I_{DRN}}$$

Where $1.5 \bullet 10^{-6}$A is the minimum TMR current and $0.0917\sqrt{A}/V$ is the gain term of the multiplier.

Substituting for ΔV_{SNS} and I_{DRN}

$$I_{TMR} = 1.5 \bullet 10^{-6}A + 0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet I_D \bullet \sqrt{V_{DS}} \frac{R_{SNS}}{\sqrt{R_{DRN}}}$$

When TMR reaches 1.215V, the $\overline{FLT}$ pin pulls low and the MOSFET is turned off and allowed to cool for an extended period. The total elapsed time between the onset of output clamping and turning off is given by:

$$t_{TMR} = V_{TMR(F)} \bullet \frac{C_{TMR}}{I_{TMR}}$$

Because I_{TMR} is a function of V_{DS} and I_D, the exact time spent in overvoltage before turning off depends upon the input waveform and the load current.

Fault Timer Operation in Overcurrent

TMR pin behavior in overcurrent is substantially the same as in overvoltage. In the presence of an overcurrent condition when the LTC4380 regulates the output current, the TMR pin charges from 0V to 1.215V with a current that varies principally as a function of the power dissipated in the MOSFET. In addition to the variable current, an additional 27µA hastens timeout in a low impedance short where the output is less than 1.5V. This additional current is reduced to 7µA when V_{OUT} is above 3V.

APPLICATIONS INFORMATION

The TMR pin current with V_{OUT} less than 1.5V is given by

$$I_{TMR} = (27 + 1.5) \bullet 10^{-6}A + 0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet I_D \bullet \sqrt{V_{DS}} \frac{R_{SNS}}{\sqrt{R_{DRN}}}$$

Where $27 \bullet 10^{-6}A$ is the extra TMR current during overcurrent condition.

And with V_{OUT} above 3V

$$I_{TMR} = (7 + 1.5) \bullet 10^{-6}A + 0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet I_D \bullet \sqrt{V_{DS}} \frac{R_{SNS}}{\sqrt{R_{DRN}}}$$

Where $7 \bullet 10^{-6}A$ is the extra TMR current during overcurrent condition.

When TMR reaches 1.215V, the $\overline{FLT}$ pin pulls low and the MOSFET is turned off and allowed to cool for an extended period. The total elapsed time between the onset of output clamping and turning off is given by

$$t_{TMR} = V_{TMR(F)} \bullet \frac{C_{TMR}}{I_{TMR}}$$

Because I_{TMR} is a function of V_{DS} and I_D, the exact time spent in overcurrent before turning off depends upon the input waveform, the output voltage and the time required for the output current to come into regulation.

Cool Down Phase

Cool down behavior is the same whether initiated by overvoltage or overcurrent. During the cool down phase, the timer continues to charge from 1.215V to 3.4V with 2µA, and then discharge back down to 1.215V with 2µA. This cycle repeats 14 times and at the 15th cycle the TMR pin is pulled all the way to ground. The total cool down time is given by:

$$t_{COOL} = C_{TMR} \frac{15 \bullet 4.37V + (1.215V - 0.1V)}{2\mu A}$$

Up to this point the operation of the LTC4380-1/LTC4380-3 and LTC4380-2/LTC4380-4 is the same. Behavior at the end of the cool down phase is entirely different.

At the end of the cool down phase, when TMR crosses the 100mV reset threshold, the LTC4380-1/LTC4380-3 remain latched off and $\overline{FLT}$ remains low. They may be restarted by pulling the ON pin low for at least 100µs or by cycling the power supply. The cool down phase may be interrupted at anytime by pulling the ON pin low for at least 10ms/µF of C_{TMR}; the LTC4380-1/LTC4380-3 will restart when ON goes high. The LTC4380-2/LTC4380-4 will automatically retry at the end of the cool down phase without cycling the ON pin and the cool down phase may be interrupted by pulling the ON pin low for at least 10ms/µF of C_{TMR}.

For both versions, the $\overline{FLT}$ pin goes high in shutdown and is cleared high when power is first applied to V_{CC}. If $\overline{FLT}$ is set low, it can be reset during the cool down phase by pulling the ON pin low for at least 10ms/µF of C_{TMR}.

Supply Transient Protection

The LTC4380 is tested to operate to 72V and guaranteed to be safe from damage up to 80V. Voltage transients above 80V may cause permanent damage. During a short-circuit condition, the large change in current flowing through power supply traces and associated wiring can cause inductive voltage transients which can exceed 80V. To minimize the voltage transients, minimize the power trace parasitic inductance by using short, wide traces. An RC filter at the V_{CC} pin is an effective measure against voltage spikes.

Another way to limit transients to less than 80V at the V_{CC} pin is to use a small Zener diode and a resistor, D1 and R1 in Figure 1. The Zener diode limits the voltage at the pin while the resistor limits the current through the diode to a safe level during the surge. However, D1 can be omitted if the filtered voltage at the V_{CC} pin, due to R1 and C1, stays below 80V. The inclusion of R1 in series with the V_{CC} pin modestly increases the minimum required voltage at V_{IN} due to the extra voltage drop across it from the small V_{CC} current of the LTC4380 and the leakage current of D1.

A total bulk capacitance of at least 22µF low ESR electrolytic or ceramic is required close to the source pin of MOSFET M1.

APPLICATIONS INFORMATION

MOSFET Selection

The LTC4380 drives an N-channel MOSFET to carry the load current. The important features of the MOSFET are on-resistance $R_{DS(ON)}$, the maximum drain-source voltage $V_{(BR)DSS}$, the threshold voltage, and the safe operating area (SOA).

The maximum allowable drain-source voltage must be higher than the peak supply voltage. If the output is off or shorted to ground during an overvoltage event, the full supply voltage will appear across the MOSFET.

The gate drive for the MOSFET is guaranteed to be more than 10V and less than 14V above the OUT pin for those applications with V_{CC} higher than 8V. This allows the use of a standard threshold voltage N-channel MOSFET. For systems with steady state V_{CC} less than 8V, a logic level MOSFET is required since the gate drive can be as low as 5V.

The SOA of the MOSFET must encompass all fault conditions. In normal operation the MOSFET is fully on, dissipating very little power. But during overvoltage or overcurrent faults, the GATE pin is either clamped to limit the output voltage or controlled to regulate the current through the MOSFET. Large current and high voltage drop across the MOSFET can coexist and dissipate significant power in these cases. The SOA curves of the MOSFET must be considered carefully in conjunction with the selection of the fault timer capacitor.

Transient Stress in the MOSFET

During an overvoltage event, the LTC4380 clamps the gate of the pass MOSFET to limit the output voltage at an acceptable level. The load circuitry may continue operating throughout this interval, but only at the expense of dissipation in the MOSFET pass device. MOSFET dissipation or stress is a function of the input voltage waveform, output voltage and load current. The MOSFET must be sized to survive this stress.

Most transient event specifications use the prototypical waveshape shown in Figure 2, comprising a linear ramp of rise time t_r, reaching a peak voltage of V_{PK} and exponentially decaying back to V_{IN} with a time constant of τ. A common automotive transient specification has constants of t_r = 10µs, V_{PK} = 80V and τ = 1ms. A surge

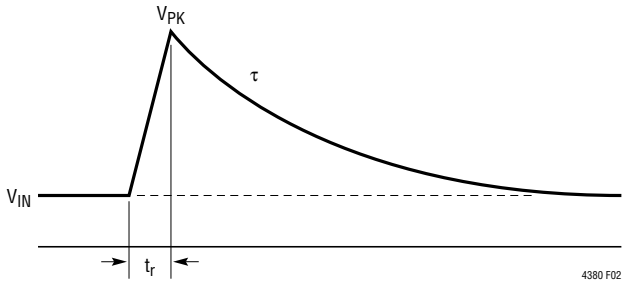


Figure 2. Prototypical Transient Waveform

condition known as load dump commonly has constants of t_r = 5ms, V_{PK} = 60V and τ = 200ms.

MOSFET stress is the result of power dissipated within the device. For long duration surges of 100ms or more, stress is increasingly dominated by heat transfer out of the package; this is a matter of device packaging and mounting, and heat sink thermal mass. This is best analyzed by simulation, using the MOSFET thermal model.

For short duration transients of less than 100ms, MOSFET survival is a matter of safe operating area (SOA), an intrinsic property of the MOSFET. SOA quantifies the time required at any given condition of V_{DS} and I_D to raise the junction temperature of the MOSFET to its rated maximum. MOSFET SOA can be expressed in units of watt-squared-seconds (P^2t). This figure is essentially constant for intervals of less than 100ms for any given device type, and rises to infinity under DC operating conditions. Destruction mechanisms other than bulk die temperature distort the lines of an accurately drawn SOA graph so that P^2t is not the same for all combinations of I_D and V_{DS}. In particular P^2t tends to degrade as V_{DS} approaches the maximum rating, rendering some devices useless for absorbing energy above a certain voltage.

Calculating Transient Stress

To select a MOSFET suitable for any given application, the SOA stress must be calculated or simulated for each input transient which shall not interrupt operation. It is then a simple matter to choose a device which has adequate SOA to survive the maximum calculated stress. P^2t for a prototypical transient waveform is calculated as follows (Figure 3):

APPLICATIONS INFORMATION

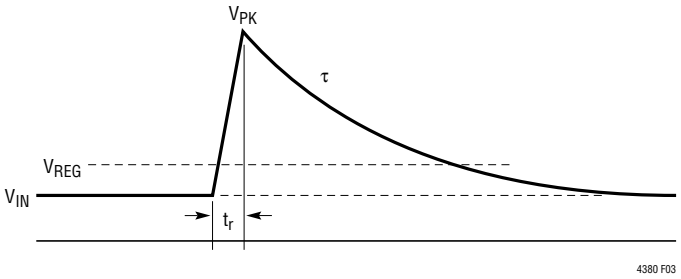


Figure 3. Safe Operating Area Required to Survive Prototypical Transient Waveform

Let

$a = V_{REG} - V_{IN}$

$b = V_{PK} - V_{IN}$

(V_{IN} = Nominal Input Voltage)

Then

$$P^2t = I_{LOAD}{}^2 \bullet \left[\frac{1}{3}t_r\frac{(b-a)^3}{b} + \frac{1}{2}\tau\left(2a^2\ln\frac{b}{a} + 3a^2 + b^2 - 4ab\right)\right]$$

For the transient conditions of V_{PK} = 100V, V_{IN} = 12V, V_{REG} = 27V, t_r = 10µs, τ = 1ms, and a load current of 3A, P^2t is $18W^2s$ which can be handled by a MOSFET in a DPAK package. The P^2t of other transient waveshapes is evaluated by integrating the square of MOSFET power over time. LTspice® can be used to simulate timer behavior for more complex transients and cases where overvoltage and overcurrent faults coexist, as well as the peak temperature rise of the MOSFET.

Calculating Short-Circuit Stress

SOA stress must also be calculated for a short-circuit condition. Short-circuit P^2t is given by:

$$P^2t = \left(\Delta V_{DS} \bullet \frac{\Delta V_{SNS}}{R_{SNS}}\right)^2 \bullet t_{TMR} \quad \left[W^2s\right]$$

Where ΔV_{DS} is the voltage across the MOSFET, ΔV_{SNS} is the current limit threshold and t_{TMR} is the overcurrent timer interval.

For V_{IN} = 15V, ΔV_{DS} = 12V (V_{OUT} = 3V), ΔV_{SNS} = 50mV, R_{SNS} = 12mΩ, R_{DRN} = 100kΩ and C_{TMR} = 68nF, P^2t is $24.5W^2s$ – somewhat higher than the transient SOA calculated in the previous example.

Limiting Inrush Current and GATE Pin Compensation

The LTC4380 limits the inrush current to any load capacitance by controlling the GATE pin voltage slew rate. An external capacitor, C2, can be connected from GATE to ground to reduce the inrush current at the expense of slower turn-off time. The gate capacitor is set at:

$$C2 = I_{GATE(UP)} \bullet \frac{C_L}{I_{INRUSH}}$$

The LTC4380 needs a minimum of 47nF capacitance (C2) and a 33Ω (R2) resistor in series at the GATE pin to stabilize the current limit amplifier during an overcurrent event. C2 also limits self enhancement of the MOSFET. A 10Ω resistor, R3, is connected to the gate of the MOSFET to suppress parasitic oscillations.

Automobile Cold Crank Ride Through

During cold crank the battery potential drops from the 12V nominal to as low as 3V for up to 40ms. The LTC4380 needs at least 4V at the V_{CC} pin to function correctly. The low quiescent current requirement of the part allows an RC filter with reasonable values to be placed at the V_{CC} pin to ride through cold crank, as shown in Figure 4.

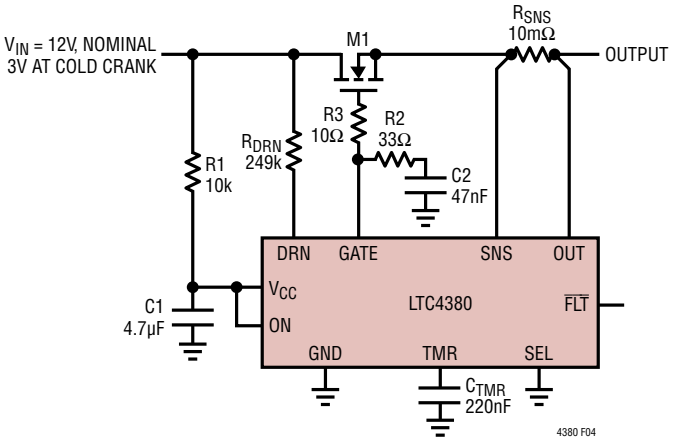


Figure 4. Automotive Cold Crank Ride Through

APPLICATIONS INFORMATION

Ignoring the supply current (I_{CC}), the V_{CC} potential at the end of cold crank is given by:

$$V_{CC} = (V_{IN(NOM)} - V_{IN(LOW)}) \bullet e^{\frac{-t}{R1 \bullet C1}} + V_{IN(LOW)}$$

Where $V_{IN(NOM)}$ is the input voltage before the cold crank starts, $V_{IN(LOW)}$ is the lowest input voltage during cold crank, and t is the duration of the cold crank.

With the combination of R1 (10kΩ) and C1 (4.7µF), V_{CC} drops to 6.8V after the input voltage drops from 12V to 3V for 40ms. During this time GATE stays high, keeping the MOSFET on to continue providing current to the output.

Reverse Input Protection

A blocking diode is commonly employed to protect the load where reverse input is possible, such as in automotive applications. This diode causes extra power loss, generates heat, and reduces the available supply voltage range. During cold crank, the extra voltage drop across the diode is particularly undesirable.

The LTC4380 is designed to withstand reverse voltage without damage to itself. The V_{CC}, ON, and SEL pins can withstand up to 60V of DC voltage below GND. Back-to-back MOSFETs can be used to block the reverse current path through M1's body diode to protect the load. See Figure 5.

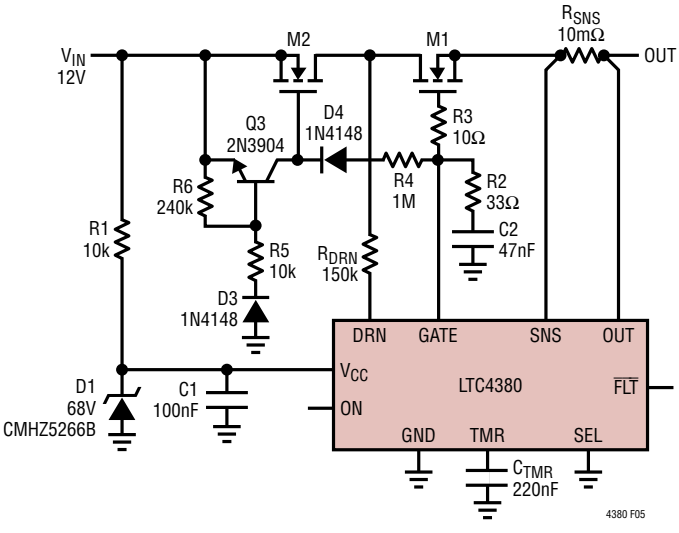


Figure 5. Overvoltage Protector with N-Channel MOSFET Reverse Input Protection

Shutdown

The LTC4380 can be shut down to a lower current mode by pulling the ON pin below the shutdown threshold of 1.05V. The quiescent current drops down to 6µA. An external Zener diode from the input supply to the ON pin can be used to implement undervoltage lockout, as illustrated in Figure 8. The UV threshold is the Zener voltage plus the shutdown threshold voltage.

The ON pin can be pulled up to 80V or below GND by up to 60V without damage. Leaving the pin open allows an internal resistor to pull it up and turn on the part. The leakage current at the pin should be limited to no more than 1µA, if no pull up device is used to help turn on the part.

Layout Considerations

To achieve accurate current sensing, use Kelvin connections to the current sense resistor (R_{SNS} in Figure 5). The minimum trace width for 1 oz copper foil is 0.02" per amp to ensure the trace stays at a reasonable temperature. 0.03" per amp or wider is recommended. Note that 1 oz copper exhibits a sheet resistance of about 530µΩ/square. Small resistances can cause large errors in high current applications.

Design Example

As a design example, take an application with the following specifications: V_{IN} = 5V to 14VDC with a transient of 150V and decay time constant (τ) of 400ms, $V_{OUT} \leq 27V$, current limit (I_{LIM}) at 5A, and cold crank to 3V for 40ms.

The SEL pin is grounded for 27V output clamping in Figure 6. The selection of a 68V Zener diode for D1 limits the voltage at the V_{CC} pin to less than 80V during a 150V surge. The minimum required voltage at the V_{CC} pin is 4V when V_{IN} is at 5V; the V_{CC} pin input current is less than 40µA. The maximum value for R1 to ensure proper operation is:

$$R1 = \frac{\text{Minimum } V_{IN} - \text{Minimum } V_{CC}}{\text{Supply Current}} = \frac{5V - 4V}{40\mu A} = 25k\Omega$$

Select 10kΩ for R1 to accommodate all conditions.

The maximum current through R1 into D1 during transients is then calculated as:

$$I_{D1} = \frac{150V - 68V}{10k\Omega} = 8.2mA$$

APPLICATIONS INFORMATION

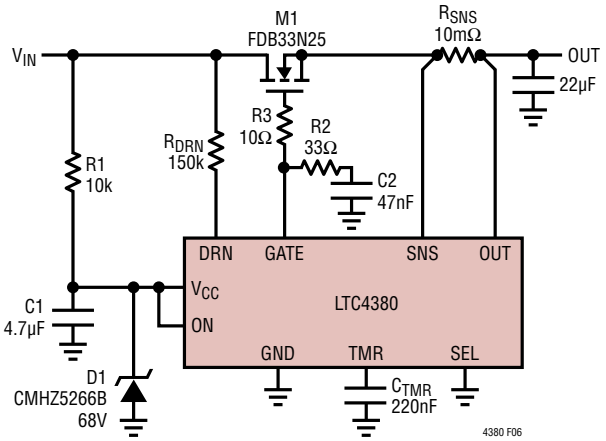


Figure 6. Design Example

CMHZ5266B can handle 500mW indefinitely and 1W for 1 second.

The V_{CC} pin needs at least 4V to operate through cold crank from 12V down to 3V for 40ms. The value of C1 can be calculated as:

$$C1 = \frac{-40ms}{10k\Omega \bullet \ln\left(\frac{1}{9}\right)} = 1.82\mu F$$

4.7µF is chosen to accommodate for the supply current of the part and other conditions.

With C1 = 4.7µF and R1 = 10kΩ, high voltage transients up to 200V with a pulse width of less than 10ms are filtered out at the V_{CC} pin. Longer surges are suppressed by D1.

Next calculate the sense resistor (R_{SNS}) value where the current limit threshold is 50mV:

$$R_{SNS} = \frac{50mV}{I_{LIM}} = \frac{50mV}{5A} = 10m\Omega$$

R_{DRN} is chosen to produce a current into the DRN pin of 1mA, during the maximum overvoltage transient event:

$$R_{DRN} = \frac{150V - 27V}{1mA} = 123k\Omega$$

150kΩ is chosen to ensure enough margin.

Next C_{TMR} is chosen to power up the output before the TMR pin reaches the gateoff threshold of 1.215V:

$$C_{TMR} = \frac{I_{TMR(UP)} \bullet t_{INRUSH}}{V_{TMR}}$$

Where

$$t_{INRUSH} = \frac{V_{IN} \bullet C2}{I_{GATE(UP)}} = V_{IN}\frac{C_{LOAD}}{I_{INRUSH}}$$

$$= \frac{14V \bullet 47nF}{20\mu A} = 32.9ms$$

$I_{TMR(UP)} \approx 1.5\mu A$. To limit the rise of V_{TMR} to 0.4V

$$C_{TMR} = \frac{1.5\mu A \bullet 32.9ms}{0.4V} \approx 123nF$$

220nF is chosen to accommodate all conditions.

The pass transistor, M1, should be chosen to withstand an output short with V_{CC} = 14V. In the case of a severe output short where V_{OUT} = 0V, the total overcurrent fault time is:

$$t_{OC} = \frac{220nF \bullet 1.215V}{30.5\mu A} = 8.76ms$$

The power dissipation in M1 is:

$$P = \frac{14V \bullet 62mV}{10m\Omega} = 86.8W$$

and $P^2t = 66W^2s$

During an output overload or soft short, the voltage at the OUT pin could stay at 3V or higher. The total overcurrent fault time when V_{OUT} = 3V is:

$$t_{OC} = \frac{220nF \bullet 1.215V}{9.75\mu A} = 27.4ms$$

The power dissipation in M1 is:

$$P = \frac{(14V - 3V) \bullet 50mV}{10m\Omega} = 55W$$

and $P^2t \approx 83W^2s$

These conditions are well within the safe operating area of the FDB33N25.

APPLICATIONS INFORMATION

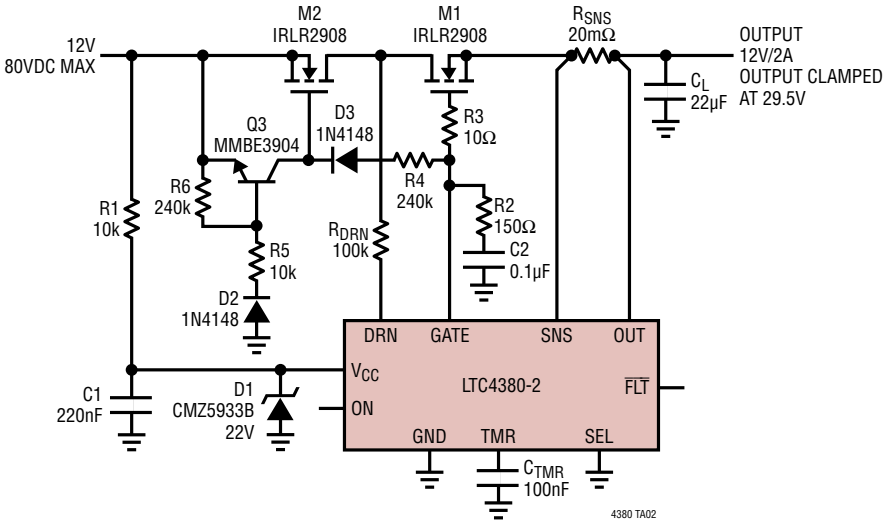


Figure 7. 12V Overcurrent Protected High Side Switch

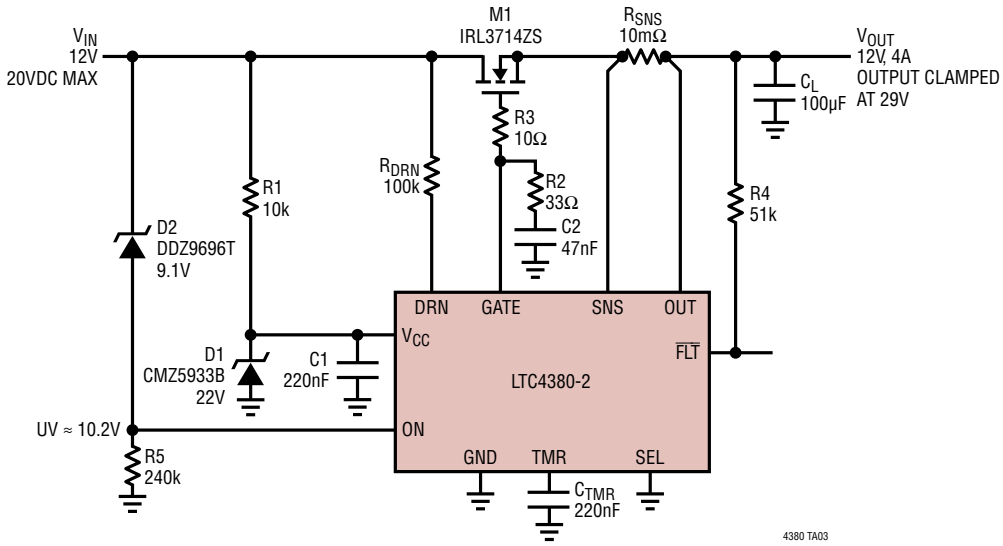


Figure 8. 12V Hot Swap Controller with Input UV Detection

APPLICATIONS INFORMATION

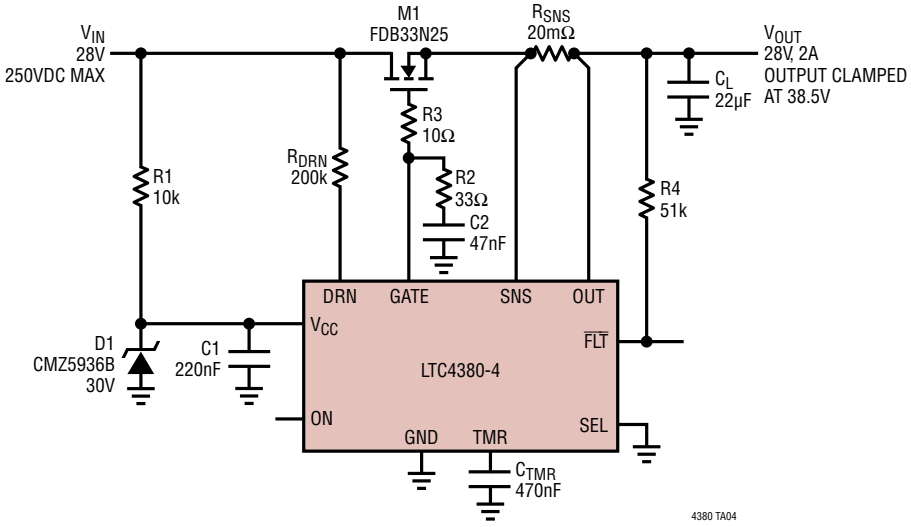


Figure 9. 28V Surge Stopper with Output Clamped to Below 40V

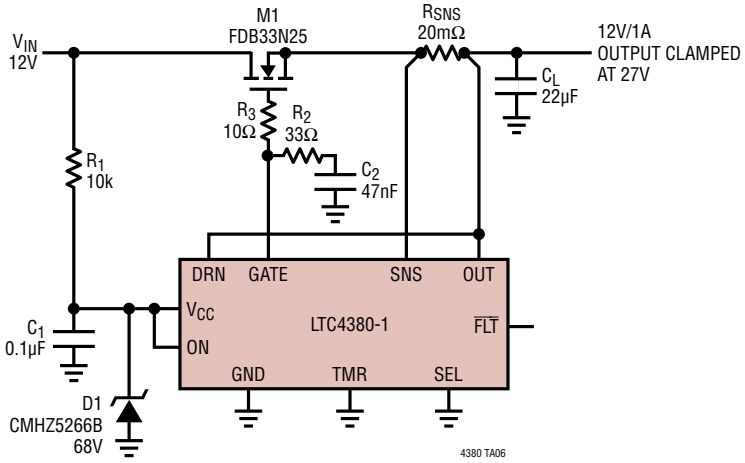
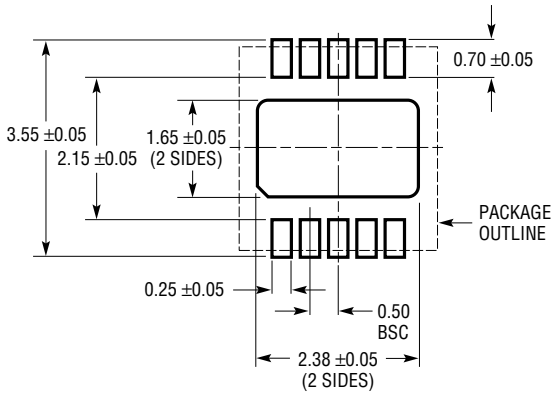


Figure 10. 12V Surge Stopper with Fault Timer Disabled

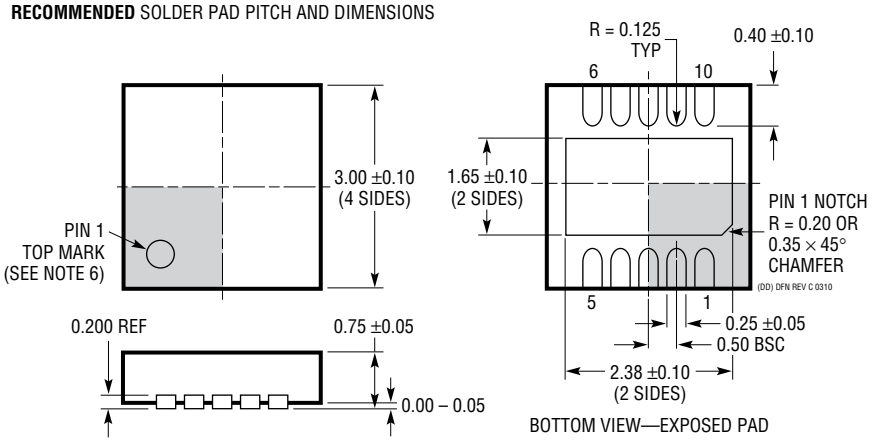
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4380#packaging for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



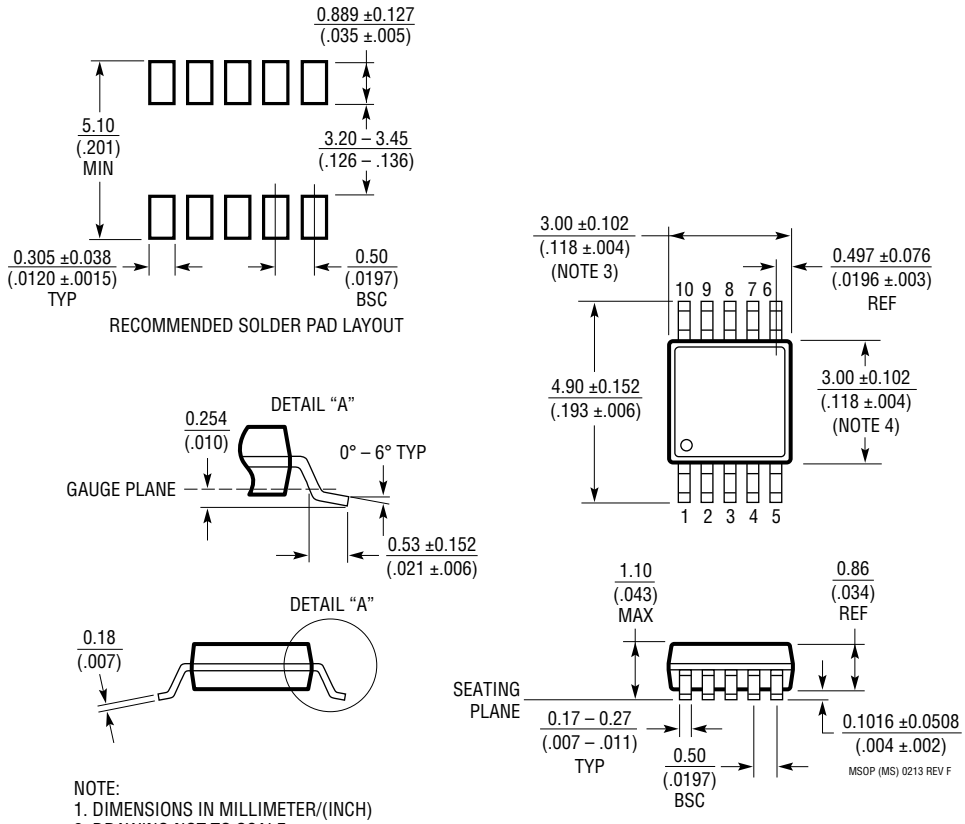
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4380#packaging for the most recent package drawings.

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/16	Updated specification limits: I_{OUT} ON, ΔV_{SNS} at OUT = 6V/12V.	3, 4
		TMR pin function: Added recommendation for capacitor rating and type.	7
B	06/17	Clarified pin conditions for Electrical Characteristics	4
		Updated conditions for $I_{TMR(UP)}$ Overvoltage and Retry Duty Cycle Overcurrent specifications	5

TYPICAL APPLICATION

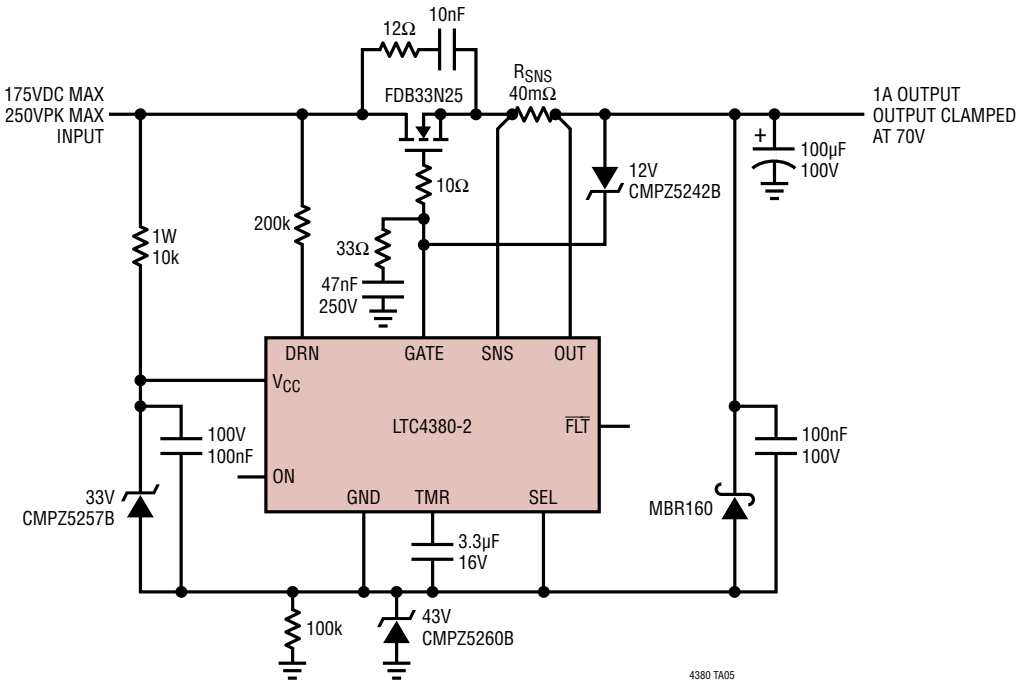


Figure 11. 48V Floating Surge Stopper

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT4356	Surge Stopper with Current Limit	4V to 80V Operation; 100V Protection; DFN-12, MSOP-10 and SO-16 Packages
LTC4359	Ideal Diode Controller	4V to 80V Operation, –40V Input Protection, DFN-8 and MSOP-8 Packages
LTC4361	Overvoltage/Overcurrent Protection Controller	2.5V to 5.5V Operation, 80V Protection, TSOT-8 and DFN-8 Packages
LT4363	Surge Stopper with Current Limit	4V to 80V Operation; >100V Protection; DFN-12, MSOP-12 and SO-16 Packages
LTC4364	Surge Stopper with Ideal Diode	4V to 80V Operation; –40V to >100V Protection; DFN-14, MSOP-16 and SO-16 Packages
LTC4365	OV, UV and Reverse Input Protection Controller	2.5V to 34V Operation, –40V to 60V Protection, DFN-8 and TSOT-8 Packages
LTC4366	High Voltage Surge Stopper	9V to >500V Operation, Floating Topology, TSOT-8 and DFN-8 Packages
LTC4367	OV, UV and Reverse Input Protection Controller	2.5V to 60V Operation, –40V to 100V Protection, DFN-8 and MSOP-8 Packages
LTC4368	LTC4367 + Bidirectional Circuit Breaker	±50mV or +50mV/–3mV Circuit Breaker Thresholds; DFN-10, MSOP-10 Packages
LTC7860	Switching Surge Stopper	3.5V to 60V Operation, >100V Protection, MSOPE-12 Package

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