LTM2893 Isolated 100MHz ADC Serial Interface and LTC2328-18

DESCRIPTION

Demonstration circuit 2405A shows an LTM®2893 isolating and interfacing an LTC®2328-18. The LTM2893 is a high speed SPI isolator for interfacing read only ADCs with a full complement of control signals. The LTC2328-18 is a low noise, high speed 18-bit successive approximation register (SAR) ADC. Low noise isolated power is delivered to the isolated side with an LT3999 push-pull driver and isolation transformer.

The DC2405A demonstrates the DC and AC operation of the LTC2328-18 without performance degradation with the LTM2893. The Serial Peripheral Interface (SPI) runs at a maximum 100MHz SCK frequency. The LTM2893 is compatible with many ADCs with SPI clock frequencies up to 100MHz.

The DC2405A connects to either the DC890 for measurements with PScope™, or DC590 for measurements with QuikEval™, or DC2026 for measurements with QuikEval and a DC590 sketch or single sample measurements with an example sketch.

Design files for this circuit board are available at http://www.linear.com/demo/DC2405A

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range	V_{CC} – GND	4.75		5.25	V
Analog Signal Input Range (AIN)				±10.24	V
Clock Frequency (CLK IN)		10		100	MHz
DC590 Interface Voltage Supply		3.0	3.3	3.6	V

DC2405A CONNECTION DIAGRAM

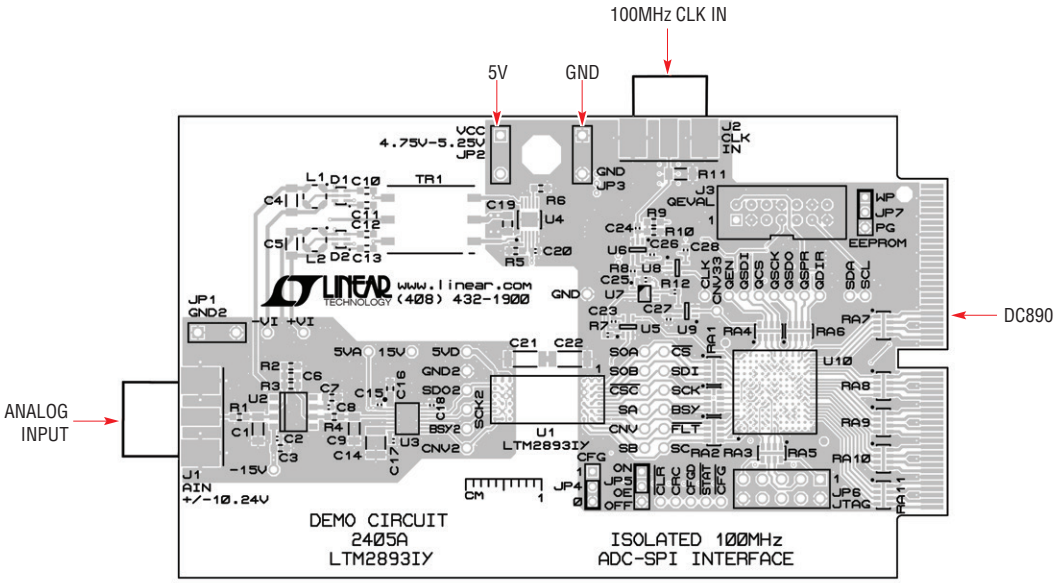


Figure 1. DC2405A Setup

DC2405A JUMPERS

DEFINITIONS

JP1 – GND2, Isolated ground connection

JP2 – VCC, 5V Power supply input connection

JP3 – GND, Power supply return connection

JP4 – CFG, Default 0, when CFG = 1 a secondary image in U10 is selected, currently not implemented.

JP5 – OE, Output enable for U10, default ON. When OE is ON, U10 drives the signals to U1 (for use with the DC890, DC590, and DC2026). When OE is OFF the signals to U1 are high impedance from U10 and the interface signals can be driven externally.

JP6 – JTAG, header for factory use only

JP7 – EEPROM, is for factory use only, default WP.

DC890 QUICK START PROCEDURE

Check to make sure that all switches and jumpers are set to their default settings as described in the DC2405A Jumpers section and Figure 1 of this manual. The demo board is designed to use the onboard isolated power supply to generate all the required bias voltages. The analog input is DC coupled.

1. Connect the DC2405A to a DC890 USB High Speed Data Collection Board using the edge connector J4.
2. Connect the DC890 to a host PC with a standard USB A/B cable.
3. Apply +5V and ground to the VCC and GND terminals.
4. Apply a low jitter signal source to J1. Observe the recommended input voltage range for the analog input.
5. Connect a low jitter 100MHz 2.5V_{P-P} sine wave or square wave to connector J2. Note that J2 has a 50Ω termination resistor to ground. Alternatively, a DC1216A 100MHz fixed frequency clock source board can be used.
6. Run the PScope software (Pscope.exe version K83 or later), which can be downloaded from www.linear.com/designtools/software. The PScope software should recognize the DC2405A and configure itself automatically.
7. Click the Collect button (see Figure 2) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

Complete PScope software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

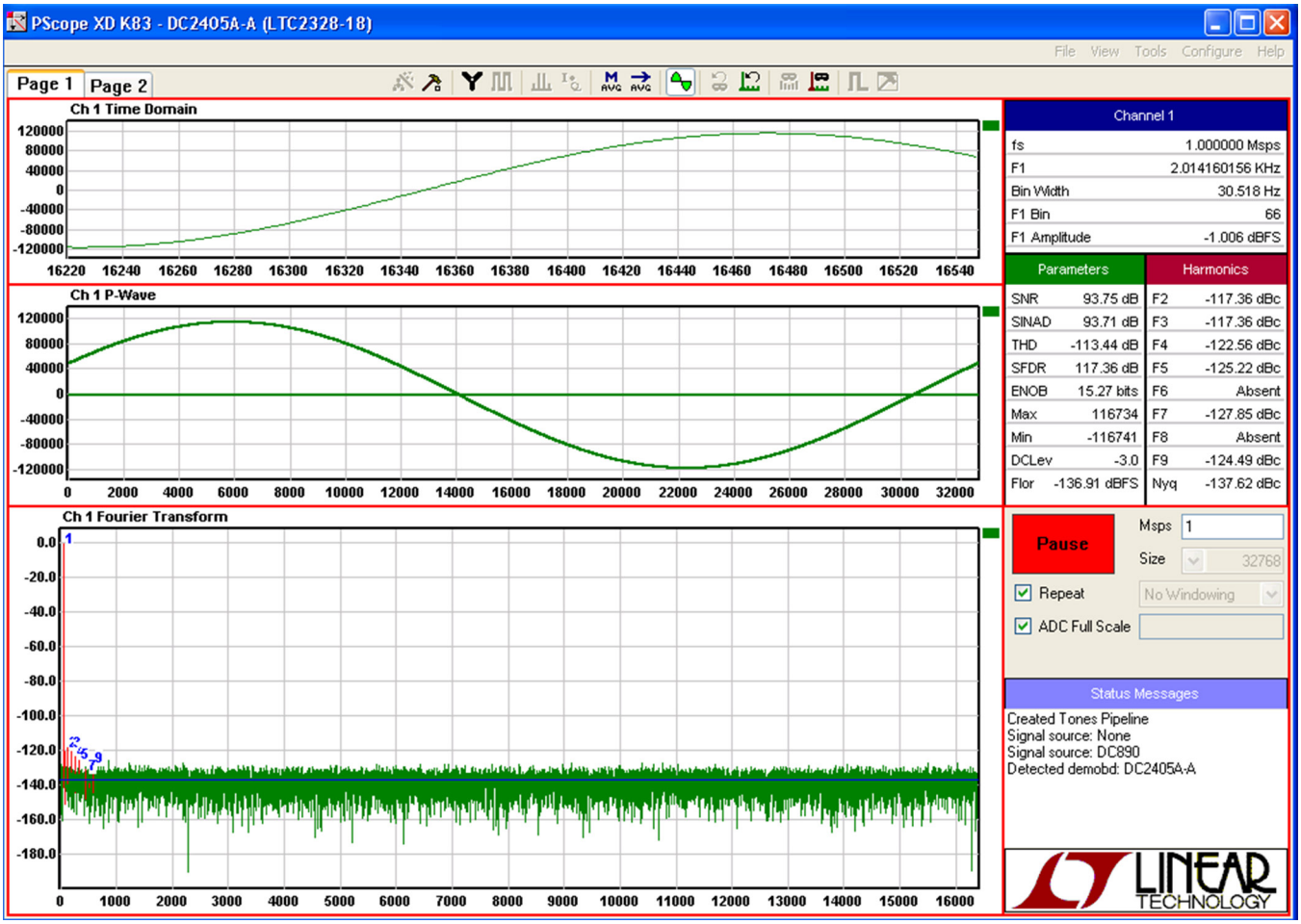


Figure 2. PScope Display Capturing 2kHz Input Tone

DC590/DC2026 QUICK START PROCEDURE

IMPORTANT! To avoid damage to the DC2405A, make sure that VCCIO (JP6 of the DC590, JP3 of the DC2026) of the DC590/DC2026 is set to 3.3V before connecting the DC590/DC2026 to the DC2405A.

1. To use the DC590/DC2026 with the DC2405A, it is necessary to apply 5V and ground to the VCC and GND terminals of the DC2405A.
2. Connect the DC590/DC2026 to a host PC with a standard USB A/B cable.
3. Connect the DC2405A to a DC590/DC2026 USB serial controller using the supplied 14-conductor ribbon cable.
4. Apply a signal source to J1. A clock source on J2 is not necessary.
5. Run the QuikEval software (QuikEval.exe version K107 or later), which is available from www.linear.com/designtools/software. The correct control panel will be loaded automatically.
6. Click the COLLECT button (Figure 3) to begin reading the ADC.

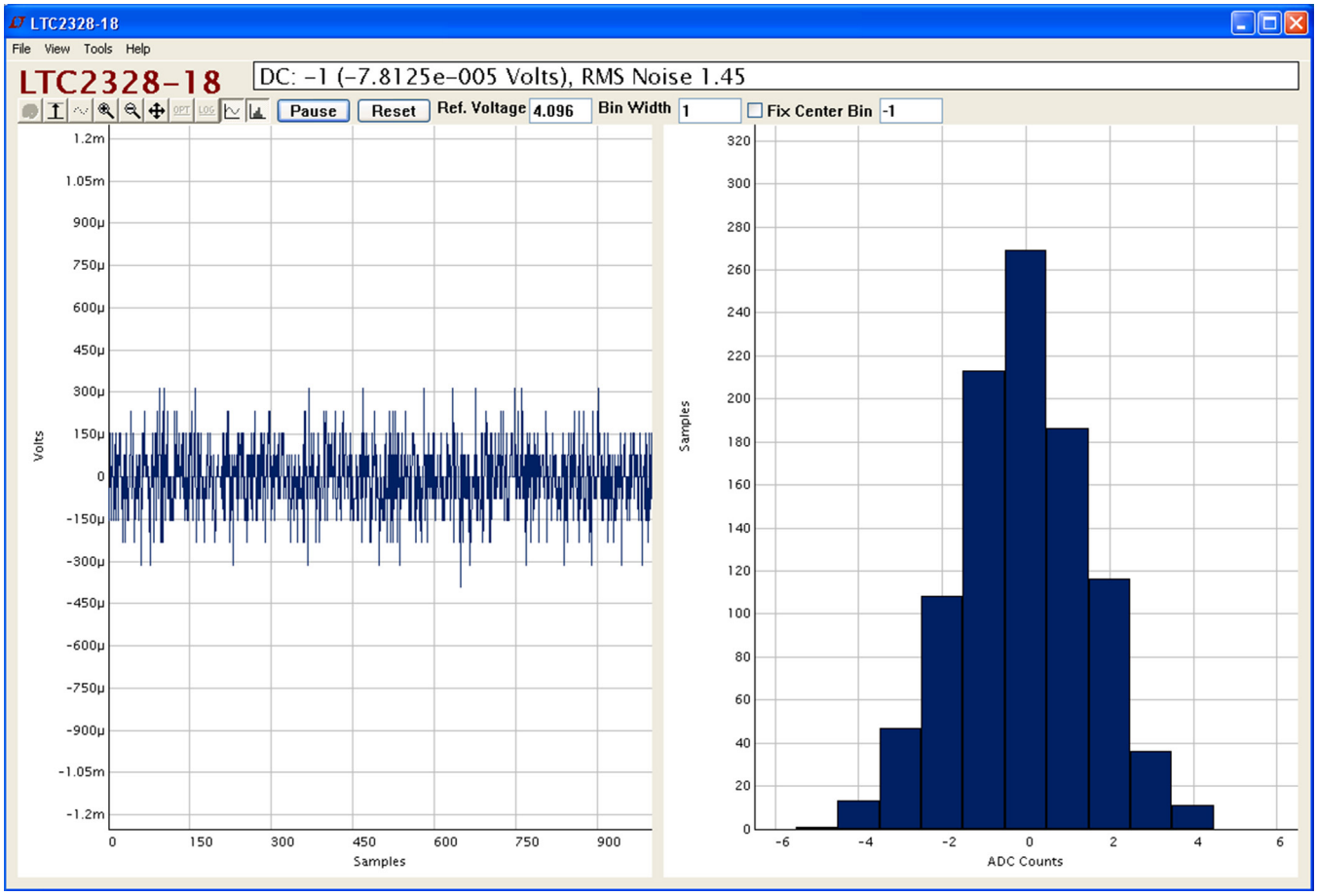


Figure 3. QuikEval Screenshot Captured with a 50Ω Terminator on AIN

DC2405A SETUP

DC POWER

The DC2405A requires +5V_{DC} and draws ~265mA. This current is split between the isolated side and the logic side. The isolated side current consumption is through the DC/DC power converter supplying the LT1468, input buffer, LTC2328-18 ADC, and the isolated side of the LTM2893. The logic side current supplies the FPGA, clock input path, and the LTM2893.

CLOCK SOURCE

You must provide a low jitter 2.5V_{P-P} sine or square wave to the clock input J2 for data collection with the DC890. The clock input is AC-coupled so the DC level of the clock signal is not important. A generator, such as the Rohde & Schwarz SMB100A high speed clock source, is recommended to drive the clock input. Drive J2 with a 100MHz clock frequency. The ratio between the clock source and the sampling frequency is 100:1. A 100MHz clock source results in a 1Msps sampling rate.

DATA OUTPUT

If not connected to a DC890, parallel data output from this board (0V to 2.5V by default), can be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use pin 50 of J4, edge connector, to latch the data. The data should be latched using the negative edge of this signal.

ANALOG INPUTS

The DC2405A analog input AIN is a single-ended input referenced to GND2. AIN has a high input impedance buffer (LT1468) before the LTC2328-18 ADC. The default setup for the DC2405A requires that AIN be driven with a low noise, low distortion generator for SINAD, THD, or SNR testing. Use an analog source such as the Stanford Research DS360 or SR1. Synchronize the clock source to the analog source through an external reference input to generate SNR and SINAD results similar to Figure 2 without windowing.

LTM2893 DIGITAL INTERFACE

The demo board has an unpopulated header placeholder in-between U10 and U1. All interface signals between the FPGA (U10) and the logic interface of the LTM2893 (U1) are exposed. An external interface may be connected to this header location by setting the OE jumper JP5 off. When JP5 is low, all signals to the LTM2893 will be high impedance from the FPGA. The header placeholder pin pitch is on 0.100-inch centers.

DC2405A DATA COLLECTION

This demo board is tested in-house by attempting to duplicate the FFT plot shown in Figure 2. This involves a 100MHz clock source synchronized with a reference clock to an SR1 sinusoidal generator. The SR1 sinusoidal generator is set at a frequency of 2.01416kHz. The input signal level is approximately –1dBFS. A typical FFT obtained with DC2405A is shown in Figure 2. Note that to calculate the real SNR, the signal level (F1 amplitude = –1.006dB) has to be added back to the SNR that PScope displays. With the example shown in Figure 2, this means that the actual SNR would be 94.76dB instead of the 93.76dB that PScope displays.

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with an input frequency that is a sub-multiple of the sample rate and will only exercise a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and N/2. Multiply M/N by the sample rate to obtain the input sine wave frequency. Another scenario that can yield poor results is if you do not have a signal generator capable of ppm frequency accuracy or if it cannot be locked to the clock frequency. You can use an FFT with windowing to reduce the "leakage" or spreading of the fundamental, to get a close approximation of the ADC performance. If an amplifier or clock source with poor phase noise is used, the windowing will not improve the SNR.

DC590/DC2026 DATA COLLECTION

Due to the relatively low and somewhat unpredictable sample rate of the DC590/DC2026, its usefulness is limited to noise measurement and data collection of slowly moving signals.

To observe measurements from QuikEval, use a DC590 or program a DC2026 with a DC590 sketch from an Arduino IDE. Then launch QuikEval, a typical data capture and histogram are shown in Figure 3.

To observe measurements and see example code for reading and configuring the LTM2893 from the DC2026, run an Arduino IDE and select File > Sketchbook > Part Number > 2000 > 2800 > 2893 >DC2405A. Upload the program to the DC2026 and launch the Serial Monitor from the tools menu. A brief menu will display on the serial monitor output. Selecting 1 and sending to the DC2026 will result in a single conversion and the result will be displayed in the Serial Monitor window.

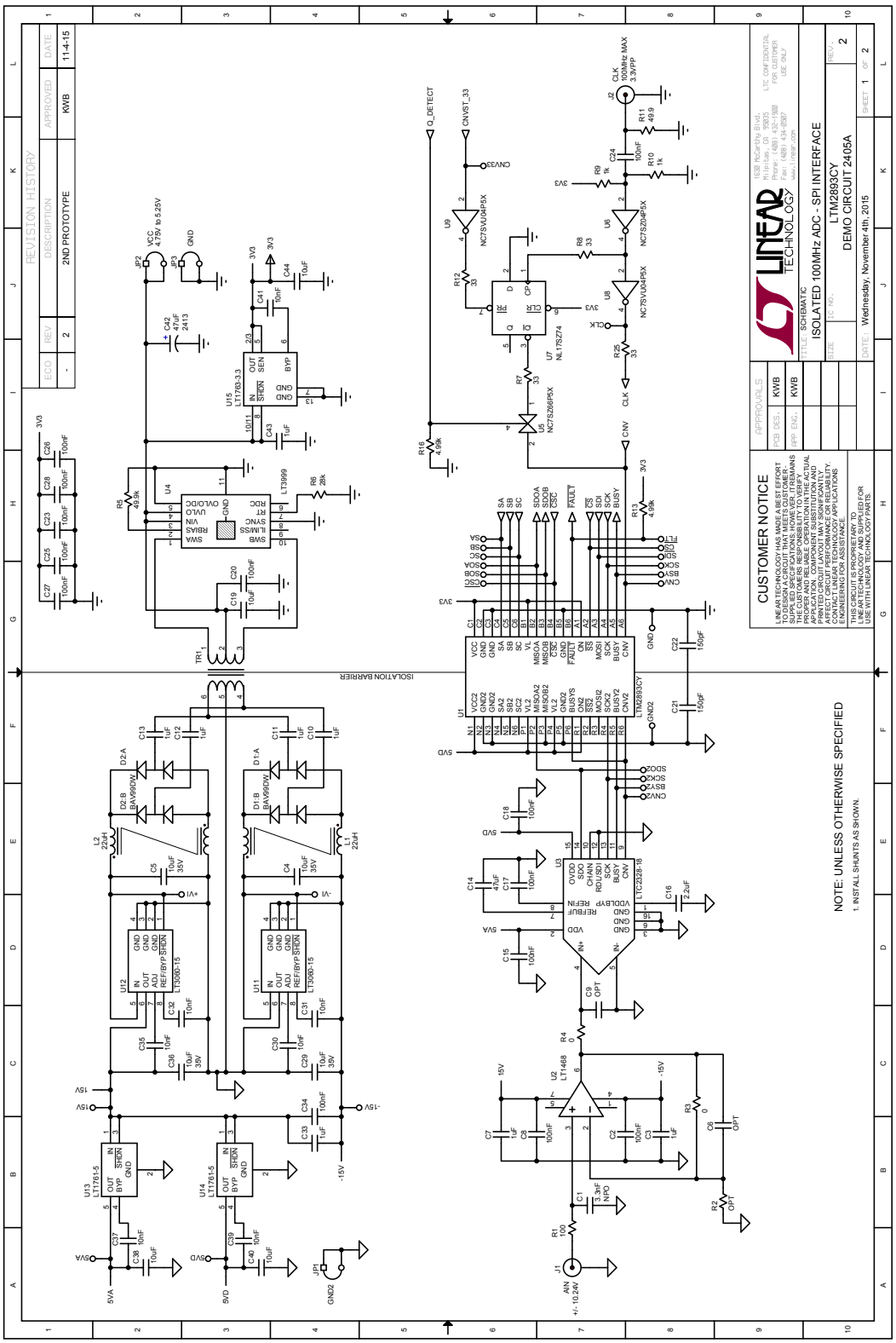
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	1	C1	CAPACITOR, CERAMIC, 3.3nF 5% 1206 250V NPO	TDK/C3216C0G2E332J085AA
2	40	C2, C8, C15, C17, C18, C20, C23-C28, C34, C45-46, C48-71, C73	CAPACITOR, CERAMIC, 100nF 10% 0402 50V X7R	TDK/C1005X7R1H104K050BB
3	9	C3, C7, C10-13, C43, C47, C72	CAPACITOR, CERAMIC, 1µF 10% 0603 35V X7R	TDK/C1608X7R1V105K080AC
4	4	C4-5, C29, C36	CAPACITOR, CERAMIC, 10µF 10% 1206 35V X7R	TDK/C3216X7R1V106K160AC
5	0	C6, C9	OPTIONAL	
6	1	C14	CAPACITOR, CERAMIC, 47µF 20% 1210 6.3V X7S	TDK/C3225X7S0J476M250AC
7	1	C16	CAPACITOR, CERAMIC, 2.2µF 10% 0603 10V X7R	TDK/C1608X7R1A225K080AC
8	4	C19, C38, C40, C44	CAPACITOR, CERAMIC, 10µF 10% 0805 16V X6S	TDK/C2012X6S1C106K085AC
	2	C21-22	CAPACITOR, CERAMIC, 150pF 10% 1808 250V X7R	MURATA/GA342QR7GF151KW01L
9	7	C30-32, C35, C37, C39, C41	CAPACITOR, CERAMIC, 10nF 10% 0402 50V X7R	TDK/C1005X7R1H103K050BB
10	1	C33	CAPACITOR, CERAMIC, 1µF 10% 1206 100V X7R	TDK/C3216X7R2A105K160AA
11	1	C42	CAPACITOR, TANTALUM, 47µF 10% 2413 16V	KEMET/T494C476K016AT
12	2	D1-2	DIODE, ARRAY, 75V 215mA SOT363	DIODES INC/BAV99DW-7-F
13	2	J1-2	CONNECTOR, BNC JACK, EDGE MOUNT	TE CONNECTIVITY/1274727-1
14	1	J3	HEADER, 2 × 7 2mm SHROUDED	MOLEX/87831-1420
15	3	JP1-3	HEADER, LOOP 1 × 2, 0.2mm	AAVID/125700D00000G
16	3	JP4-5, JP7	HEADER, 1 × 3, 2mm	WURTH/62000311121
17	3	JP4-5, JP7	SHUNT, 1 × 2, 2mm	WURTH/60800213421
18	1	JP6	HEADER, 2 ×5, 0.1mm	WURTH/61301021121
19	2	L1-2	INDUCTOR, COUPLED, 22µH 3 × 3mm 1.9Ω 0.44A	COILCRAFT/LPD3015-223MRB
20	6	MH1-6	STANDOFF, NYLON 0.25"	KEYSTONE, 8831 (SNAP ON)
21	2	R3-4	RESISTOR, 0Ω 1% 0603	VISHAY/CRCW06030000Z0EA
22	1	R2	OPTIONAL	
23	3	R9-10, R35	RESISTOR, 1kΩ 1% 0603	VISHAY/CRCW06031K00FKEA
24	4	R7-8, R12, R25	RESISTOR, 33Ω 1% 0402	VISHAY/CRCW040233R0FKED
25	1	R11	RESISTOR, 49.9Ω 1% 1206	VISHAY/CRCW120649R9FKEA
26	1	R6	RESISTOR, 28kΩ 1% 0603	VISHAY/CRCW060328K0FKEA
27	1	R5	RESISTOR, 49.9kΩ 1% 0603	VISHAY/CRCW060349K9FKEA
28	7	R13, R16, R22, R36-38, R40	RESISTOR, 4.99kΩ 1% 0603	VISHAY/CRCW06034K99FKEA
29	14	R14-15, R17-21, R24, R26, R28, R31-33, R34	RESISTOR, 10kΩ 1% 0402	VISHAY/CRCW040210K0FKED
30	2	R1, R23	RESISTOR, 100kΩ 1% 0603	VISHAY/CRCW0603100RFKEA
31	3	R27, R29-30	RESISTOR, 100kΩ 1% 0402	VISHAY/CRCW0402100KFKED
32	1	R39	RESISTOR, 2kΩ 1% 0603	VISHAY/CRCW06032K00FKEA
33	11	RA1-11	RESISTOR ARRAY, 33kΩ 4 RES 1206	PANASONIC/EXB-38V330JV
34	1	TR1	TRANSFORMER, 5kV 2:1	WURTH/750313626
35	1	U1	IC, 100MHz ADC-SPI ISOLATOR	LINEAR TECH/LTM2893CY#PBF
36	1	U2	IC, OPAMP	LINEAR TECH/LT1468CS8#PBF
37	1	U3	IC, ADC, 1MSPS, 18-BIT, BIPOLAR, ±10.24V	LINEAR TECH/LTC2328CMS-18#PBF
38	1	U4	IC, PUSH-PULL DC/DC DRIVER, 1A, 1MHz	LINEAR TECH/LT3999EMSE#PBF

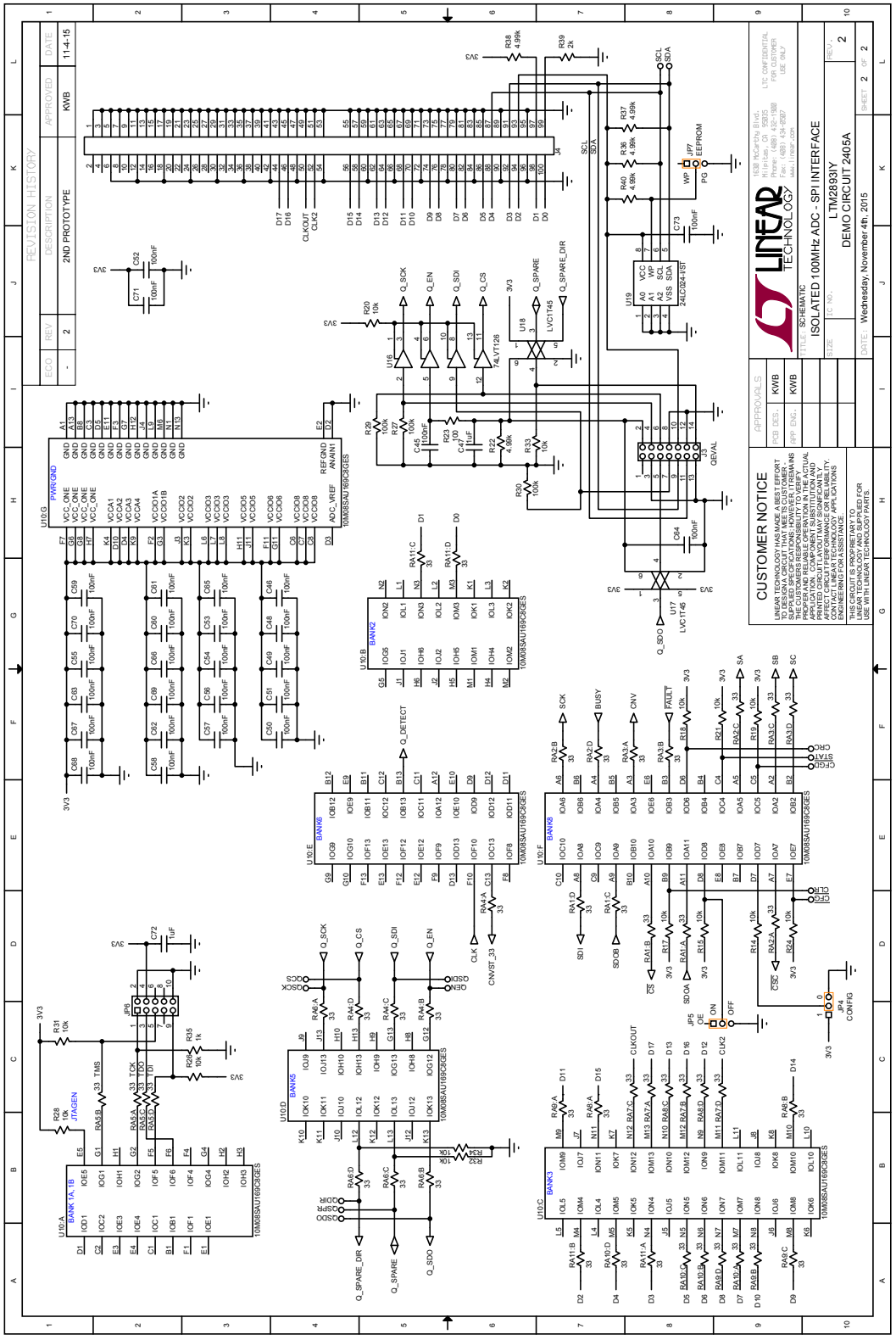
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
39	1	U5	IC, BUS SWITCH, SPST, SC70-5	FAIRCHILD SEMI/NC7SZ66P5X
40	1	U6	IC, INVERTER, SC70-5	FAIRCHILD SEMI/NC7SZ04P5X
41	1	U7	IC, D-TYPE POS TRG, MSOP8	ON SEMI/NL17SZ74USG
42	2	U8-9	IC, UNBUFFERED INVERTER, SC70-5	FAIRCHILD SEMI/NC7SVU04P5X
43	1	U10	IC, FPGA/CPLD 130 I/O 169UBGA	ALTERA/10M08SAU169C8GES
44	2	U11-12	IC, LDO, 15V, 100mA	LINEAR TECH/LT3060ETS8-15#PBF
45	2	U13-14	IC, LDO, 5V, 100mA	LINEAR TECH/LT1761ES5-5#PBF
46	1	U15	IC, LDO, 3.3V, 500mA	LINEAR TECH/LT1763CDE-3.3#PBF
47	1	U16	IC, BUFFER, TRI-STATE, QUAD, 14TSSOP	NXP/74LVT126PW,118
48	2	U17-18	IC, BUS TRANSCEIVER, TRI-STATE, SOT-563	TI/SN74LVC1T45DRLR
49	1	U19	IC, EEPROM, 2-KBIT, I^2C, 8TSSOP	MICROCHIP/24LC024-I/ST

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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