LTC6268 and LTC6268-10 3-Channel SOT-23 Transimpedance Amplifier

DESCRIPTION

Demonstration Circuit 2414A has layouts for three channels of SOT-23 transimpedance amplifiers. Each of the three layouts applies different techniques achieving various parasitic feedback capacitances (C_F). The upper channel, U3, assumes a low Transimpedance gain, has a parasitic C_F of 0.1pF, and provides a footprint for an additional component C_F in an 0402 footprint (C29). The lower channel, U1, assumes high transimpedance gain and was laid out to minimize C_F, achieving approximately 7fF, although the real situation is more complex. The middle channel, U2, assumes a middle case. The outputs of the circuit are laid out for SMA edge connectors. The inputs consist of six pads per channel along the edge where a through-hole photodiode can be mounted, with provision for any photodiode pinout. The reverse bias voltage for the photodiode can be applied at a V_{BB} turret, or can be taken from V^+ or V^- through jumper JP4. The V_{BB} traces were spaced according to IPC2221 for 150V working voltage, so high voltage APDs can be applied. **Take caution when working with high voltages to avoid contact with any part of the VBB trace.** Because of the many possible varieties of population, the board is stocked as a bare unpopulated board.

Design files for this circuit board are available at http://www.linear.com/demo/DC2414A

BOARD PHOTO

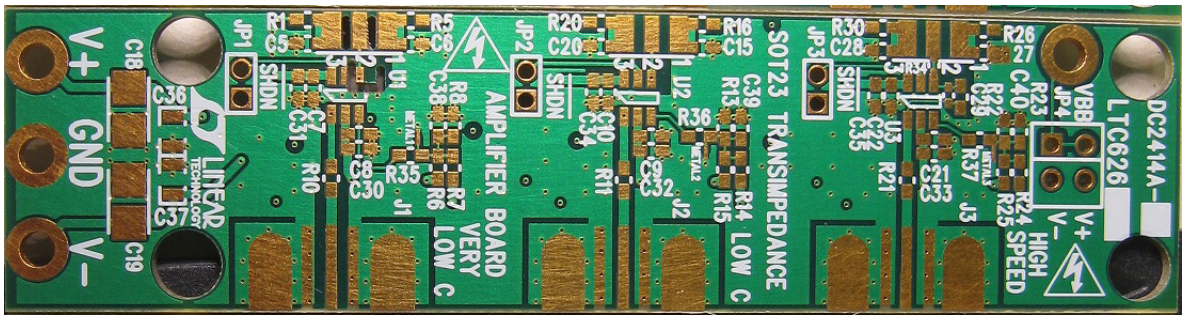


Figure 1. Topside Bare PCB DC2414A, for SOT-23 LTC®6268 and LTC6268-10 Op Amps

OPERATING PRINCIPLES

The LTC6268 and LTC6268-10 have gain bandwidth products of 500MHz and 4GHz respectively. At low transimpedance gain with small photodiodes (say 10k gain and 1pF photodiode) the bandwidth achieved can be quite high, such as 200MHz. The upper channel, U3, is best suited for these types of applications. The parasitic C_F around the R_F is about 0.1pF in this channel, and an 0402 footprint is provided so additional C_F can be added. The R_F and C_F in this highest speed channel are on the topside to avoid vias, and are close to the op amp.

At very high gains, much less bandwidth is achievable both because the gain is high and because parasitic feedback capacitance reduces the effective impedance of the feedback resistor prematurely. For both the low capacitance channels, the R_F is mounted on the bottom side for the most effective shielding from the output trace.

But the resistor and its pads also have parasitic capacitance. For example, a typical 0805 resistor has about 70fF of capacitance in air, so a 10M resistor would already be 3dB lower impedance at 220kHz. However, the circuit is not "in air," but on a board; and by placing some grounded copper underneath a resistor, the parasitic C_F can be greatly reduced.

The middle channel, U2, applies this technique rather modestly under an 0603 resistor, while the lower channel, U1, has a rather extreme layout under a 1206 resistor. These channels have parasitic C_F of about 33fF and "7fF," respectively, with a regular Vishay CRCW resistor installed. However, the "7fF" is a simplification, derived from the fact that at 10M of gain, that channel achieves rise times as low as 100ns. In fact, however, the extended body of the resistor and the ground underneath it cause some capacitive loading of the resistor element, perhaps best modelled as an RC network as shown in Figure 2.

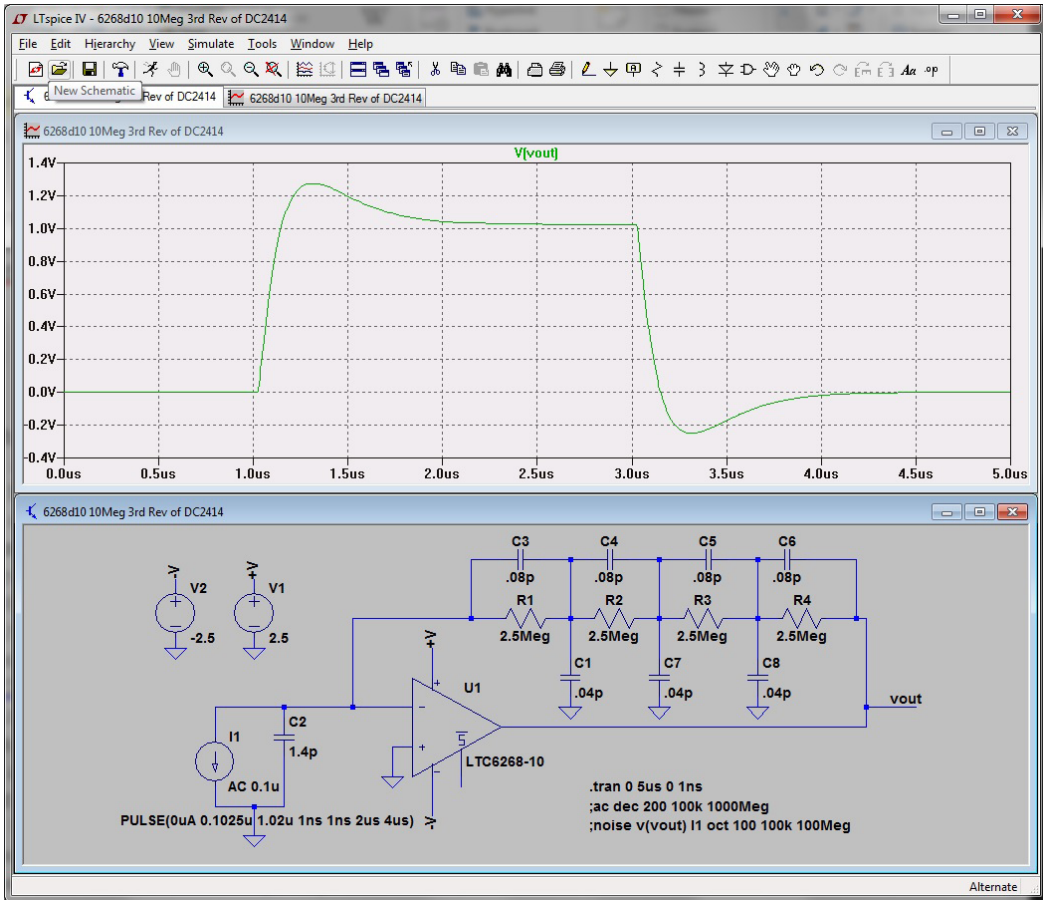


Figure 2. Capacitively Loaded Resistor Element Approximation for the U1 Channel, with R_F = 10M

OPERATING PRINCIPLES

Split Supply vs Single Supply

The default configuration of the board assumes a ±1.55V to ±2.5V split supply. To use a single supply, short V^- to ground at the GND and V^- turrets. Also, in order to keep inductance low at the op amp's V^- connection, short the V^- bypass capacitor locations near the op amp (C8/C9/C21) depending on which op amp is installed. Valid single supplies are 3.1V to 5V. When using a single supply, you will probably want to change the default voltage on the +input.

The +Input

On all 3 channels, the +input is grounded through R35/R36/R37 and a trace called "METAL" to ground. The series resistor may be a 0Ω jumper, or a 33Ω to 100Ω resistor to de-Q the path. To create a voltage other than ground at the +input, cut the "METAL" trace and create the desired voltage with the resistor strings there (R6-8, R13-15, and R23-25). Capacitors C38/C39/C40 are provided to filter the resistor noise and any supply ripple.

V_{BB}

The photodiode reverse bias can be applied at the V_{BB} turret. (Note that all "turrets" are close to the edges of the board, so clips can be applied directly to the plated holes, thus not requiring turrets to be populated.) V_{BB} can also be taken from V^+ or V^- though jumper selection JP4. **If V_{BB} will be a high voltage, be careful not to touch it when energized, as the trace runs along the entire edge of the photodiode side of the board. Lightning bolts are placed in the silkscreen as a reminder when high voltage is used for V_{BB}.** Various pads are provided to RC connect V_{BB} to the cathode or anode of the photodiode. In practice, very few of the passives shown around the photodiode will be installed. Which ones will be installed will depend on the photodiode pinout and whether the TIA will be anode or cathode connected.

Shutdown (Floats "On")

The LTC6268 _SHDN pin floats high, turning the op amp on. If you want to play with the shutdown function, install JP1/JP2/JP3. Placing the shunt on the jumper pulls the _SHDN to ground turning off the op amp.

PCB Material

The PCB dielectric, chosen for its low dielectric constant of 3.4, is Nelco-4000-EP-SI. If FR-4 is used with a similar layout, remember that the parasitic capacitances will increase by 30% to 40%. Note that this demo board is not fabricated to controlled impedance. The special material was chosen purely for low capacitance.

Checking for High Frequency Oscillations in LTC6268-10 Designs

The LTC6268-10 has a gain bandwidth product of 4GHz. When checking an LTC6268-10 design for any problems, it is best to use an oscilloscope with adequate bandwidth (>1GHz), so that any high frequency oscillations are not hidden by limited scope bandwidth. If using a spectrum analyzer, it should have at least 3GHz of bandwidth.

The DC2414A high speed channel was designed with little ground copper in the photodiode region, to support the lowest input capacitance possible. However, when the photodiode is larger, then input inductance can become an issue. For example, at 12pF of lumped element photodiode C, and with the nominal 20k || 0.1pF feedback network in place, ~30mV_{P-P} oscillations were detected at 1.4GHz. Placing a grounded copper foil tape along the bottom side copper void thoroughly quenched the oscillations.

SAMPLE POPULATION

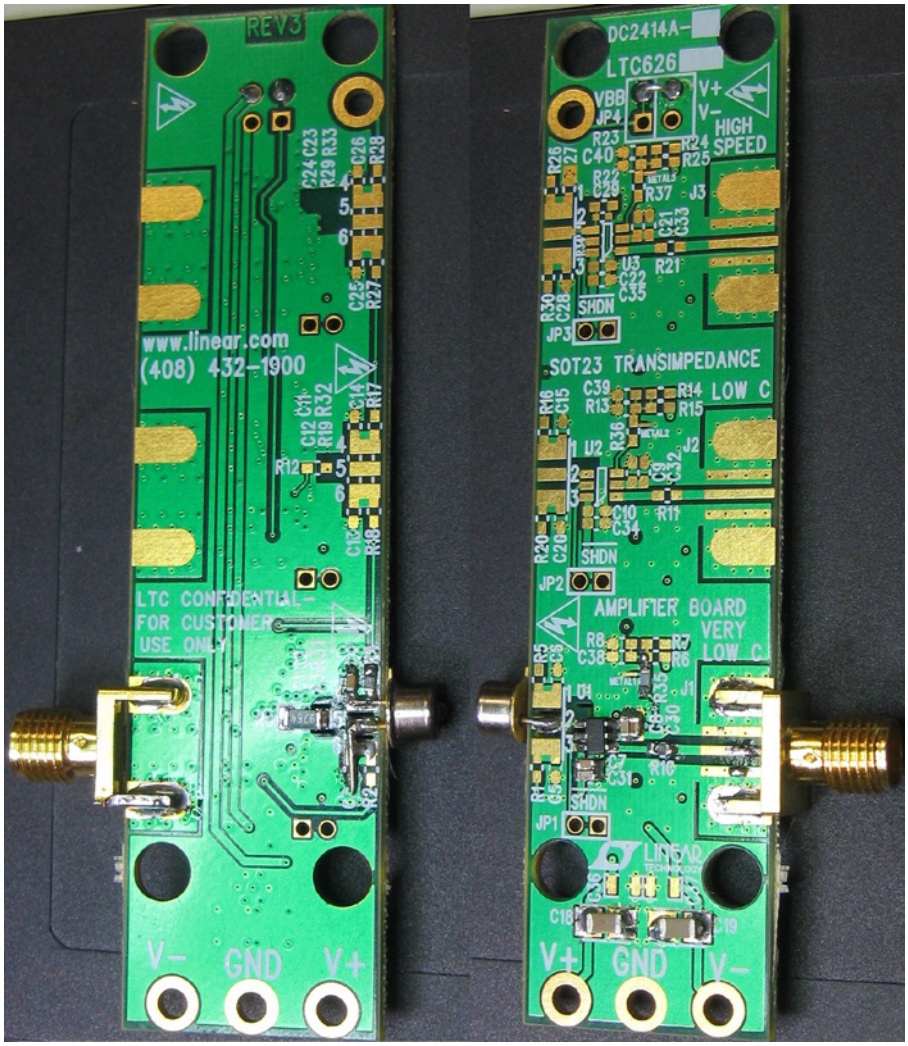
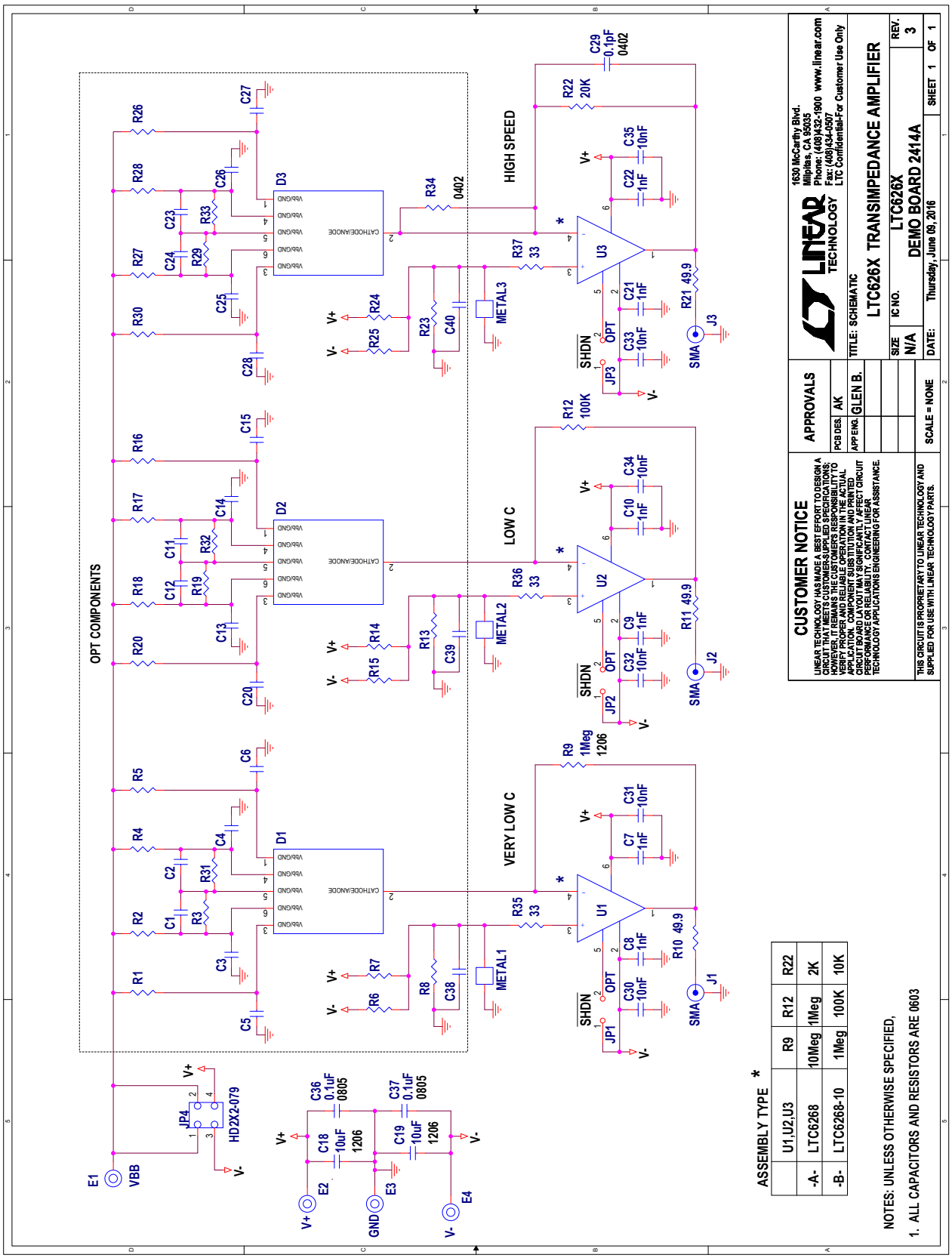


Figure 3. An Example of a Population of the Very Low Capacitance Channel Around U1. Photodiode is OSI FCI-125G-006HRL, Anode Connected to the TIA Input, so Cathode is Held High to V_{BB} Shorted to V^+. R_F is 9.76M on the Bottom Side (Left)

SCHEMATIC DIAGRAM



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