LTM9100

Anyside™ High Voltage Isolated Switch Controller with I^{2}C Command and Telemetry

DESCRIPTION

Demonstration circuit 2423A showcases the LTM®9100 Isolated Switch Controller in either a typical 48V application (–A) or in a high voltage 380V application (–B). The board may be configured for either high side or low side operation, dependent on the connection of external supply and load to the banana jacks. An on board capacitive load may also be wired into the circuit. LEDs indicate the presence of input and output voltage. The MOSFET can be easily exchanged or replaced due to screw terminal block mounting. Protection is also included to protect the GATE and SENSE pins in the event of MOSFET destruction. The circuit can be operated manually or by computer control.

Design files for this circuit board are available at http://www.linear.com/demo/DC2423A

$\boldsymbol{\mathit{LT}}$, LT, LTC, LTM, Linduino, Linear Technology and the Linear logo are registered trademarks and QuickEval and Anyside are trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

PERFORMANCE SUMMARY Specifications are at T$_A$ = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V$_{CC}$	Input Supply Range		4.5	5	5.5	V
I$_{CC}$	Input Supply Current			50		mA
V$_L$	Logic Input Supply Range		3	3.3	5.5	V
	UV Off Threshold DC2423A-A 48V Input DC2423A-B 380V Input	V$_{UV}$ Rising	2.518 41.8 251	2.56 43.4 261	2.598 44.9 270	V V V
	UV On Threshold DC2423A-A 48V Input DC2423A-B 380V Input	V$_{UV}$ Falling	2.248 37.3 224	2.291 38.8 233	2.328 40.3 242	V V V
	OV On Threshold DC2423A-A 48V Input DC2423A-B 380V Input	V$_{OV}$ Rising	1.735 69.8 420	1.770 71.8 432	1.805 73.9 444	V V V
	OV Off Threshold DC2423A-A 48V Input DC2423A-B 380V Input	V$_{OV}$ Falling	1.673 67.3 405	1.733 70.3 423	1.787 73.1 440	V V V
	Current Limit (Circuit Breaker) Threshold DC2423A-A Trip Current DC2423A-B Trip Current	 R$_S$ = 0.008Ω ±1% R$_S$ = 0.017Ω ±1%	45 5.57 2.62	50 6.25 2.94	55 6.94 3.27	mV A A
	Circuit Breaker GATE Off Delay	SENSE > 50mV	440	530	620	µs
	10-Bit ADC Full-Scale Voltage	SENSE ADIN, ADIN2	62.8 2.514	64 2.56	65.2 2.606	mV V
	Timer (TMR) Delay			12		ms
	Slow Start (SS) Time			56		ms
V$_{IORM}$	Maximum Working Insulation Voltage	GND to V$_{EE}$	1000 690			VDC VRMS
	Common Mode Transient Immunity		30	50		kV/µs

OPERATING PRINCIPLES

OVERVIEW

The LTM9100 contains an isolated DC/DC converter, delivering power to V_S at 10.4V and V_{CC2} at 5V from the input supply, V_{CC}. Isolation is maintained by the separation of GND and V_{EE} so that significant operating voltages and transients can exist without affecting the operation of the LTM9100. The logic side ON pin enables or shuts down the LTM9100. The isolated side GATE pin and MOSFET turn on are controlled by the logic side EN input. The logic side also has two status pins, PG for power good and $\overline{ALERT}$ to indicate an internal fault. LEDs indicate if either pin has been activated.

All logic side signals are referenced to the logic supply pin V_L, which may be connected to V_{CC} or to the V_L input by jumper (JP2) selection.

The DC2423A is designed to be used either stand-alone or interfaced directly with a DC590 isolated serial controller or a DC2026 Linduino® One. The QuickEval™ software may be used with either the DC590 or DC2026 (when running the DC590 Arduino code). Example Arduino code specifically for the DC2423A is also available for the DC2026. The LTM9100 includes an I^2C/SMBus interface for communication to its isolated side control and status functions, as well as ADC results. The isolated side includes two jumpers for selection of the I^2C address.

The isolated side of the LTM9100 controls the turn-on of an external MOSFET. The MOSFET leads are connected by screw terminal block, and its body is screw mounted to a heatsink and PCB. This allows the MOSFET to be easily interchanged or replaced. The design can accommodate TO-247 (default), TO-264, and TO-220 packages.

The demo board can be connected for either high side or low side applications. Banana jacks are provided and clearly labeled for voltage input and load connection depending on the selected configuration. The line monitor jumper (JP7) must also be configured for the same configuration so that the LTM9100 ADC reports the proper input voltage. LEDs indicate the presence of line voltage in blue and load voltage in yellow once the MOSFET has been turned on.

An optional capacitive load with banana connections has been provided on the demo board. It may be used by externally wiring to the proper load terminals.

Transient suppression is included to protect the MOSFET and on board load capacitor for the –B version of the demo board. The GATE pin and SENSE+ pins include external overvoltage/overcurrent protection in the event the MOSFET shorts either drain to gate or drain to source, protecting the LTM9100.

The DC2423A may be configured for other input voltages and load currents by changing a handful of components. The assembly table located on the demo board schematic lists the component variations between the –A and –B versions.

JUMPERS

DC2423A contains 7 jumpers, and a 14-pin connector for the I^2C interface. The jumpers provide either pin or function configuration, a description of jumper follows.

JP1: EEPROM Program (PG) or Write Protect (WP). For factory use only in programming the demo board ID for QuickEval. Default position: Not Populated.

JP2: V_L Supply Jumper. May be connected to V_{CC} input terminal or V_L (default) input terminal.

JP3: ON Jumper. Enables the LTM9100 in the ON (default) position, and disables operation in the OFF position. The ON terminal either monitors the state of the ON jumper, or if the ON jumper is removed, allows the ON terminal to be externally driven.

JP4: EN Jumper. Enables the LTM9100 GATE pin, provided both UV and OV functions are satisfied, in the ON (default) position, and disables GATE in the OFF position. Operation of the GATE pin may be subsequently controlled via the I^2C interface, but the EN pin must be in the high position. See the LTM9100 data sheet for I^2C only operation. The EN terminal either monitors the state of the EN jumper, or if the EN jumper is removed, allows the EN terminal to be externally driven.

OPERATING PRINCIPLES

JP5 & JP6: I^2C Address Configuration. JP5 corresponds to ADR0 and JP6 to ADR1. The address pins are 3-state inputs; they can be LO (V_{EE}), open, or HI (V_{CC2}). The default stuffing is LO-LO, which corresponds to a device write address of 0010000 (20h). An address of ADR0 = LO and ADR1 = HI puts the LTM9100 in Single-Wire Broadcast Mode, and free-running serial data appears on SDA. See data sheet for additional details.

JP7: Line Monitor Jumper. This jumper consists of two shunts which can be placed in the HIGH SIDE or LOW SIDE state as indicated. The default jumper is configuration is HIGH SIDE. Improper setting will result in invalid data representation of the input voltage at the ADIN pin.

I^2C INTERFACE – J5

A simple means of exercising the I^2C port is provided at J5, to be used in conjunction with a PC and DC590 or DC2026. The DC590 or DC2026 act as an intermediary between DC2423A and a PC, complete with isolation. Simply plug in the 14-wide interface cable from J5 to the DC590 or DC2026.

The QuickEval software is found here: www.linear.com/designtools/software. There is a 'personality' EEPROM near the J5 connector which is read by the DC590 or DC2026 to automatically bring up the correct software. From there, all of the LTM9100 registers can be read from or written to, allowing full control over all of the device's features. Alternatively the DC2026 may be used as a gateway for Arduino programming, example code provided at www.linear.com/product/LTM9100.

To connect an external I^2C interface, disconnect the DC590 or DC2026 and either use pins 4 and 7 on J5 or the SCL and SDA test points located near J5. Note that the I^2C lines are referenced to V_L and GND.

SINGLE WIRE INTERFACE

It is possible to operate the LTM9100 autonomously yet still retain the monitoring functions by placing it in Single-Wire Broadcast Mode. To do this, set the I^2C address jumpers to ADR0 = LO and ADR1 = HI. A serial data stream is then observable on the SDA pin of J5 or SDA test point near J5. See the LTM9100 data sheet for additional details.

QUICK START PROCEDURE

Demonstration circuit 2423A is easy to set up and evaluate the performance of the LTM9100. For the proper setup of a high side 48V application using the DC2423A-A, refer to Figure 1 and follow the procedure below. The procedure for DC2423A-B and/or low side applications are essentially the same, but make sure to observe proper polarities and connections in steps 3 and 4 for the alternate configurations. Also, for low side applications make sure JP7 (LINE MONITOR) is set correctly.

1. Connect external power supply to V_{CC} and GND.

2. Connect external power supply to V_L and GND, or move jumper JP2 to the V_{CC} position.

3. Connect external power supply from HIGH SIDE INPUT+ banana jack to HIGH SIDE INPUT– banana jack.

4. Connect external 48V load from HIGH SIDE LOAD+ banana jack to HIGH SIDE LOAD– banana jack. The on-board 330µF load capacitor may be used in addition to or as the only load. Connect banana jacks together observing the proper polarities.

5. Turn on V_{CC}, V_L, and 48V supplies.

6. The LTM9100 can be turned on by moving the EN jumper (JP4) to the ON position, or by connecting external stimulus between EN and GND with JP4 removed. The power good ($\overline{PG}$) LED will light after the MOSFET is on.

7. To control the LTM9100 through I^{2}C, install the Quick-Eval System software on a computer with an available USB port. The download website is www.linear.com/software. Connect DC590 or DC2026 between the computer and DC2423A, and open the QuickEval software. If already installed, update the software to obtain the LTM9100/DC2423A driver.

QUICK START PROCEDURE
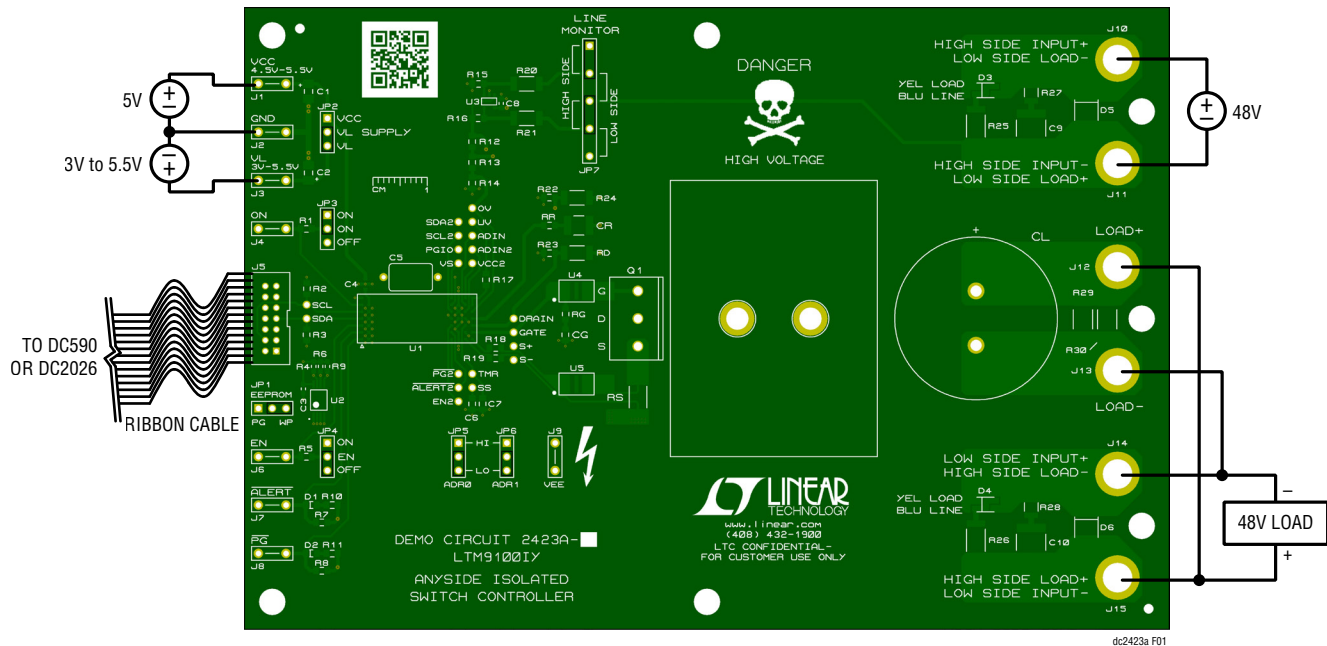
Figure 1. Demo Board Setup – High Side with On-Board and External Loads

dc2423af

6 **Linear Technology Corporation**
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

dc2423af
LT 0217 • PRINTED IN USA
© LINEAR TECHNOLOGY CORPORATION 2017