PIC16C781/782

8-Bit CMOS Microcontrollers with A/D, D/A, OPAMP, Comparators and PSMC

Microcontroller Core Features:

- High performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Direct, indirect and relative addressing modes
  - Operating speed: DC - 20 MHz clock input
    DC - 200 ns instruction cycle

Device	Program Memory X14	Data Memory X8
PIC16C781	1K	128
PIC16C782	2K	128

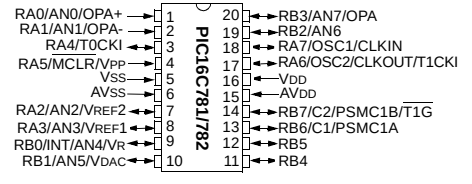
- 8-level deep hardware stack
- Interrupt capability (up to 8 internal/external interrupt sources)
- 16 I/O pins:
  - Individual direction control (13 pins)
  - Input only (3 pins), low leakage (2 pins)
  - Digital/Analog inputs (8 pins)
- Programmable PORTB interrupt-on-change (8 pins)
- Programmable PORTB weak pull-ups (8 pins)
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with a software enabled option and its own on-chip RC oscillator for reliable operation
- Programmable Brown-out Reset (BOR)
- Programmable Low Voltage Detection (LVD)
- Internal/external $\overline{\text{MCLR}}$
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options:
  HS, XT, LP, EC, RC, INTRC (4 MHz/37 kHz)
- In-Circuit Serial Programming™ (ISCP™)
- Program Memory Read (PMR) capability
- Four user programmable ID locations
- Wide operating voltage range:
  - 2.5V to 5.5V for commercial and industrial temperature ranges
  - Extended temperature range available

Microcontroller Core Features (Continued):

- Low power, high speed CMOS EPROM technology
- Fully static design
- Low power consumption:
  - < 2 mA @ 5V, 4 MHz
  - < 1 μA typical standby current.

Pin Diagram

PDIP, Windowed CERDIP, SOIC, SSOP



Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator, if INTRC oscillator mode selected
- Analog-to-Digital Converter (ADC):
  - 8-bit resolution
  - Programmable 8-channel input
  - Internal voltages available for self-diagnostics
- Digital-to-Analog Converter (DAC):
  - 8-bit resolution
  - Reference from AVDD, VREF1, or VR module
  - Output configurable to VDAC pin, Comparators, and ADC reference
- Operational Amplifier module (OPA):
  - Firmware initiated input offset voltage Auto Calibration module
  - Low leakage inputs
  - Programmable Gain Bandwidth Product (GBWP)

Peripheral Features (Continued):

- Dual Analog Comparator module with:
  - Individual enable and interrupt bits
  - Programmable speed and output polarity
  - Fully configurable inputs and outputs
  - Reference from DAC, or VREF1/VREF2
  - Low input offset voltage.
- VR voltage reference module:
  - 3.072V +/- 0.7% @25°C, AVDD = 5V
  - Configurable output to ADC reference, DAC reference, and VR pin
  - 5 mA sink/source
- Programmable Switch Mode Controller module:
  - PWM and PSM modes
  - Programmable switching frequency
  - Configurable for either single or dual feedback inputs
  - Configurable single or dual outputs
  - Slope compensation output available in single output mode

Key Features PIC® Mid-Range Reference Manual (DS33023)	PIC16C781	PIC16C782
Operating Frequency	DC - 20 MHz	DC - 20 MHZ
RESETS (and Delays)	POR, BOR, $\overline{\text{MCLR}}$, WDT (PWRT, OST)	POR, BOR, $\overline{\text{MCLR}}$, WDT (PWRT, OST)
Program Memory (14 bit words)	1K	2K
Data Memory (bytes)	128	128
Interrupts	8	8
I/O Ports	13 + 3 Input only	13 + 3 Input only
Timers	2	2
Programmable Switch Mode Controller	1	1
8-bit Analog-to-Digital Module	1	1
ADC channels	8 External, 2 Internal	8 External, 2 Internal
8-bit Digital-to-Analog Module	1	1
Comparators	2	2
Comparator Channels	4 (AN<7:4>)	4 (AN<7:4>)
Operational Amplifier	1	1
Voltage Reference	1	1
Brown-out Reset	Yes	Yes
Programmable Low Voltage Detect	Yes	Yes
Instruction Set	35 Instructions	35 Instructions

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NOTES:

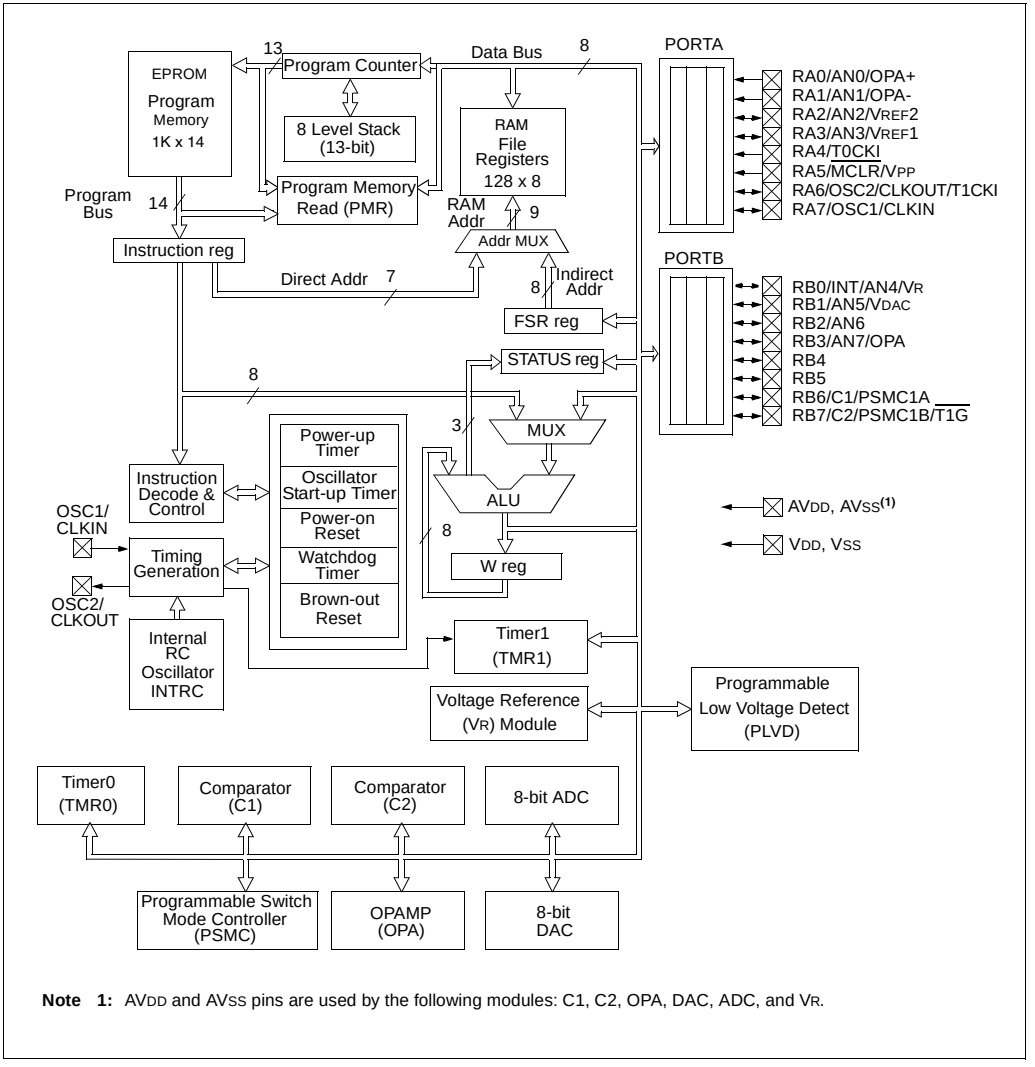
1.0 DEVICE OVERVIEW

This document contains device-specific information. Additional information may be found in the PIC Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip website. The Reference manual should be considered a complementary document to this data sheet. The Reference manual is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

This data sheet covers two devices: PIC16C781 and PIC16C782. Both devices come in a variety of 20-pin packages.

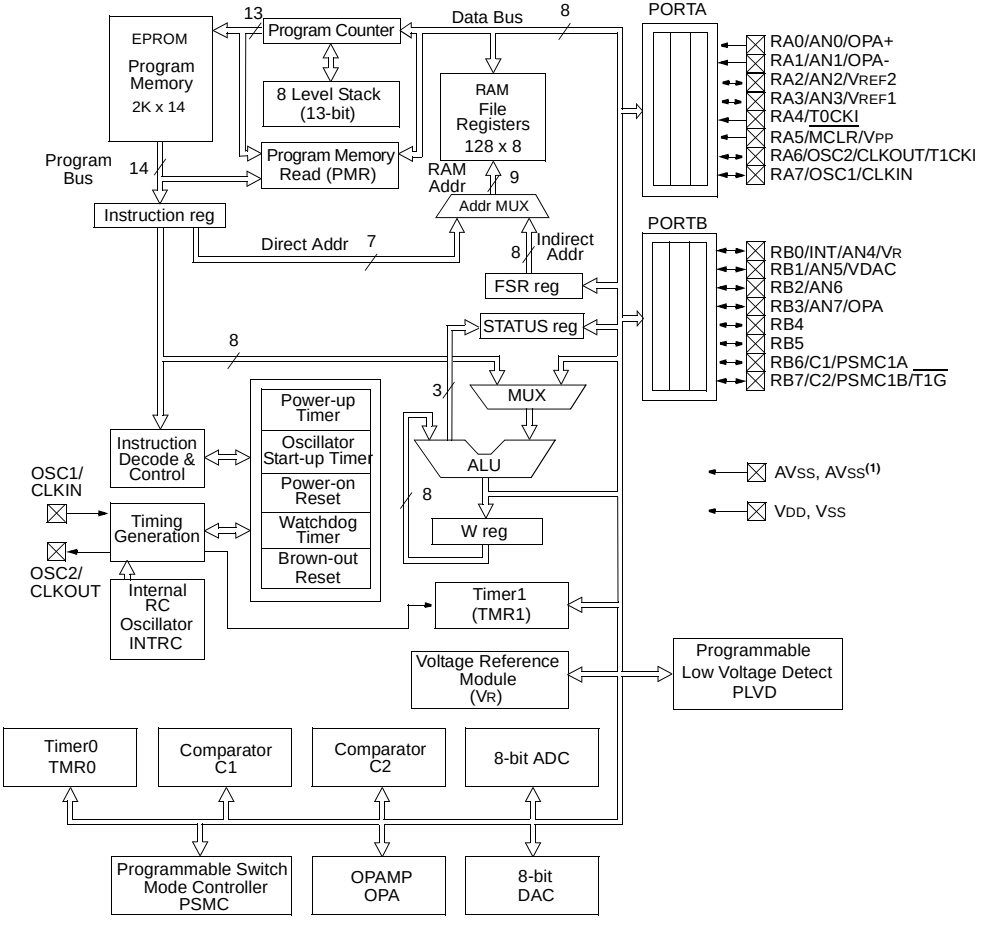
The following figures are block diagrams of the PIC16C781 and the PIC16C782.

FIGURE 1-1: PIC16C781 BLOCK DIAGRAM



Note 1: AVDD and AVSS pins are used by the following modules: C1, C2, OPA, DAC, ADC, and VR.

FIGURE 1-2: PIC16C782 BLOCK DIAGRAM



Note 1: AVDD and AVSS pins are used for the following modules: C1, C2, OPA, DAC, ADC, and VR.

FIGURE 1-3: ANALOG SIGNAL MULTIPLEXING DIAGRAM

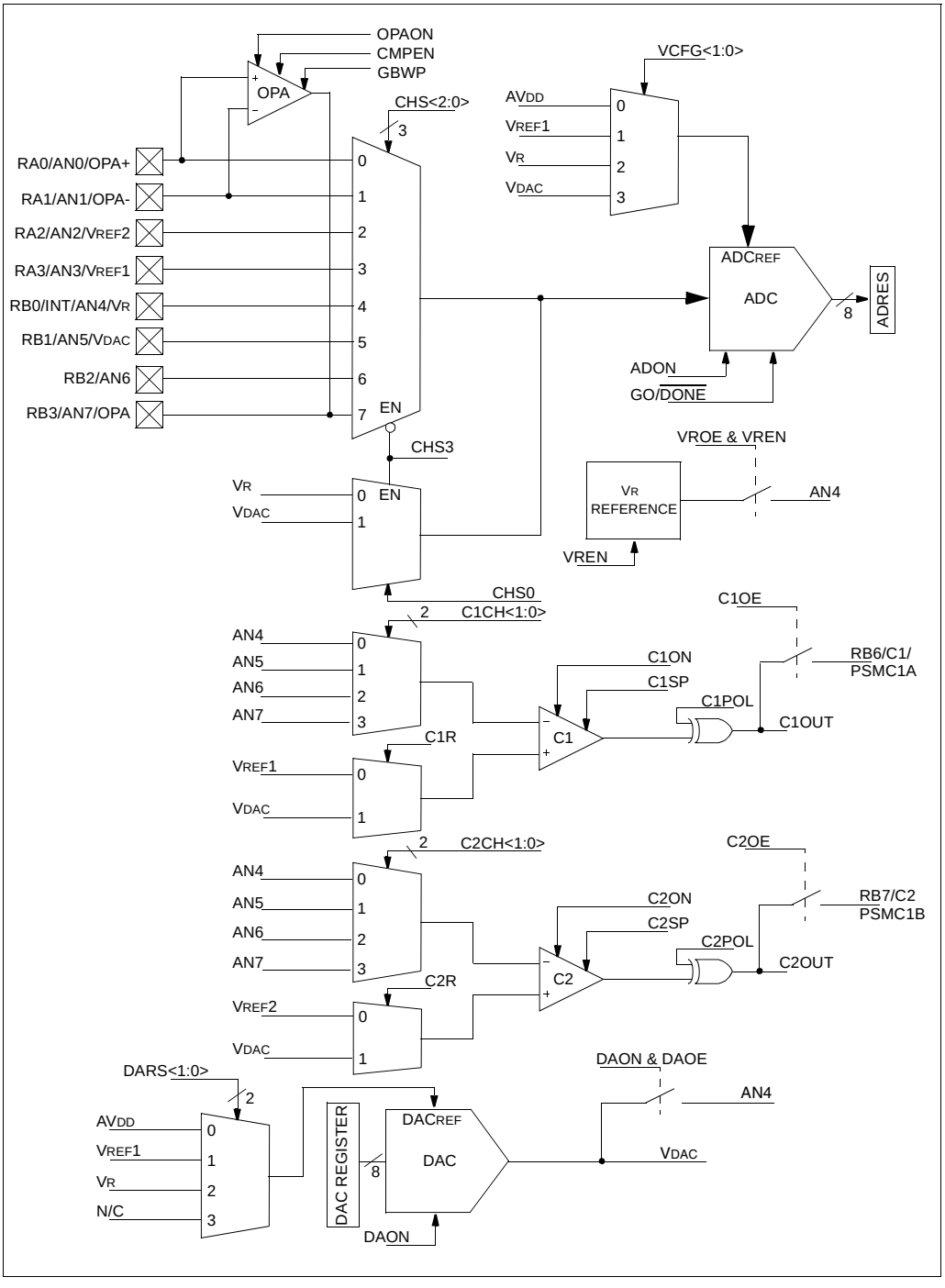


TABLE 1-1: PIC16C781/782 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/OPA+	RA0	ST	N/A	Port Input
	AN0	AN	—	ADC Input
	OPA+	AN	—	OPAMP Non-inverting Input
RA1/AN1/OPA-	RA1	ST	N/A	Port Input
	AN1	AN	—	ADC Input
	OPA-	AN	—	OPAMP Inverting Input
RA2/AN2/VREF2	RA2	ST	CMOS	Bi-directional I/O
	AN2	AN	—	ADC Input
	VREF2	AN	—	Comparator 2 Voltage Reference Input
RA3/AN3/VREF1	RA3	ST	CMOS	Bi-directional I/O
	AN3	AN	—	ADC Input
	VREF1	AN	—	Comparator 1, ADC, DACREF Input
RA4/T0CKI	RA4	ST	OD	Bi-directional I/O
	TOCKI	ST	—	Timer0 Clock Input
RA5/$\overline{\text{MCLR}}$/VPP	RA5	ST	N/A	Port Input
	$\overline{\text{MCLR}}$	ST	—	Master Clear Input
	VPP	Power	—	Programming Voltage
RA6/OSC2/CLKOUT/T1CKI	RA6	ST	CMOS	Bi-directional I/O
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	Fosc/4 Output
	T1CKI	ST	—	Timer1 Clock Input
RA7/OSC1/CLKIN	RA7	ST	CMOS	Bi-directional I/O
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External Clock Input
RB0/INT/AN4/VR	RB0	TTL	CMOS	Bi-directional I/O
	INT	ST	—	External Interrupt
	AN4	AN	—	ADC, Comparator Input
	VR	—	AN	Internal Voltage Reference Output
RB1/AN5/VDAC	RB1	TTL	CMOS	Bi-directional I/O
	AN5	AN	—	ADC, Comparator Input
	VDAC	—	AN	DAC Output
RB2/AN6	RB2	TTL	CMOS	Bi-directional I/O
	AN6	AN	—	ADC, Comparator Input
RB3/AN7/OPA	RB3	TTL	CMOS	Bi-directional I/O
	AN7	AN	—	ADC, Comparator Input
	OPA	—	AN	OPAMP Output
RB4	RB4	TTL	CMOS	Bi-directional I/O
RB5	RB5	TTL	CMOS	Bi-directional I/O
RB6/C1/PSMC1A	RB6	TTL	CMOS	Bi-directional I/O
	C1	—	CMOS	Comparator 1 Output
	PSMC1A	—	CMOS	PSMC Output 1A

TABLE 1-1: PIC16C781/782 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB7/C2/PSMC1B/$\overline{T1G}$	RB7	TTL	CMOS	Bi-directional I/O
	C2	—	CMOS	Comparator 2 Output
	PSMC1B	—	CMOS	PSMC Output 1B
	$\overline{T1G}$	ST	—	Timer 1 Gate Input
AVDD	AVDD	Power	—	Positive Supply for Analog
AVSS	AVSS	Power	—	Ground Reference for Analog
VDD	VDD	Power	—	Positive Supply for Logic and I/O pins
VSS	VSS	Power	—	Ground Reference for Logic and I/O pins

Legend: ST = Schmitt Trigger AN = Analog OD = open drain TTL = Logic Level
XTAL = Crystal CMOS = CMOS Output Power = Power Supply

NOTES:

2.0 MEMORY ORGANIZATION

There are two memory blocks in each of these PIC® microcontrollers. Each block (program and data memory) has its own bus, so that concurrent access can occur.

Additional information on device memory may be found in the PIC Mid-Range Reference Manual, (DS33023).

2.1 Program Memory Organization

The PIC16C781/782 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16C781 has 1K x 14 words of program memory. The PIC16C782 has 2K x 14 words of program memory. Accessing a location above the physically implemented address causes a wraparound.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PIC16C781 PROGRAM MEMORY MAP AND STACK

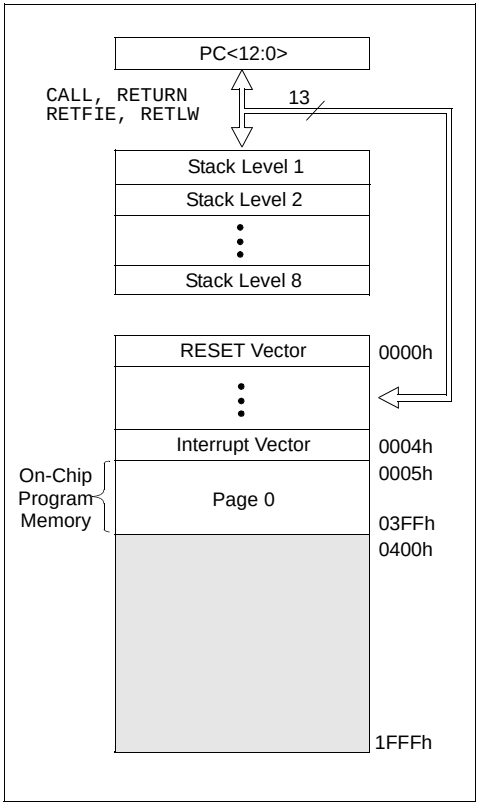
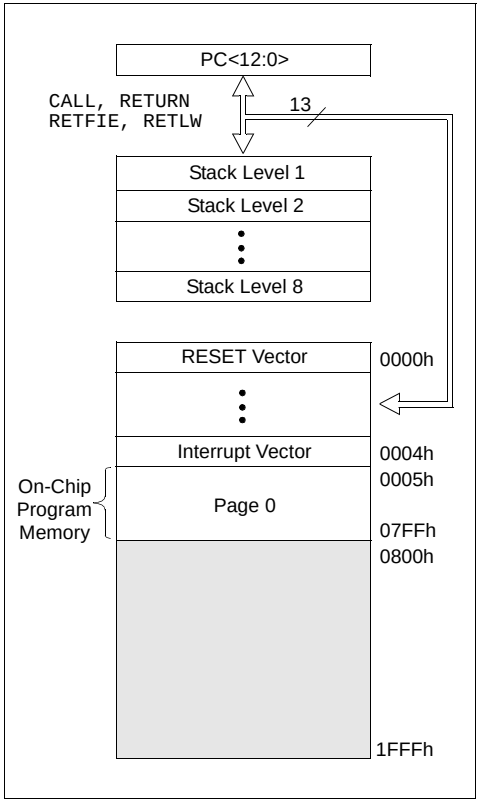


FIGURE 2-2: PIC16C782 PROGRAM MEMORY MAP AND STACK



2.2 Data Memory Organization

The data memory is partitioned into multiple banks, which contain the General Purpose Registers and the Special Function Registers. Bits RP0 and RP1 are bank select bits.

RP1	RP0	(STATUS<6:5>)

= 00 → Bank0

= 01 → Bank1

= 10 → Bank2

= 11 → Bank3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are the General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank are mirrored in another bank for code reduction and quicker access.

FIGURE 2-3: REGISTER FILE MAP

Bank 0 File Address		Bank 1 File Address		Bank 2 File Address		Bank 3 File Address	
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
	07h		87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
	0Dh		8Dh	PMADRL	10Dh		18Dh
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh		18Eh
TMR1H	0Fh		8Fh	PMADRH	10Fh		18Fh
T1CON	10h		90h	CALCON	110h		190h
	11h		91h	PSMCCON0	111h		191h
	12h		92h	PSMCCON1	112h		192h
	13h		93h		113h		193h
	14h		94h		114h		194h
	15h	WPUB	95h		115h		195h
	16h	IOCB	96h		116h		196h
	17h		97h		117h		197h
	18h		98h		118h		198h
	19h		99h	CM1CON0	119h		199h
	1Ah		9Ah	CM2CON0	11Ah		19Ah
	1Bh	REFCON	9Bh	CM2CON1	11Bh		19Bh
	1Ch	LVDCON	9Ch	OPACON	11Ch		19Ch
	1Dh	ANSEL	9Dh		11Dh		19Dh
ADRES	1Eh		9Eh	DAC	11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh	DACON0	11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 32 Bytes	A0h		120h		1A0h
			BFh				
			EFh				
accesses 70h-7Fh	7Fh	accesses 70h-7Fh	F0h FFh	accesses 70h-7Fh	170h 17Fh	accesses 70h-7Fh	1F0h 1FFh

☐ Unimplemented data memory locations, read as '0'.

* Not a physical register.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly, through the File Select Register (FSR).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1.

TABLE 2-1: PIC16C781/782 SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on Page:
Bank 0											
00h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
01h	TMR0	Timer0 Module's Register								xxxx xxxx	51
02h(2)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	23
03h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
04h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	23
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000	26
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx 0000	35
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah(1, 2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	23
0Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	19
0Ch	PIR1	LVDIF	ADIF	C2IF	C1IF	—	—	—	TMR1IF	0000 ---0	21
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	55
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	55
10h	T1CON	—	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	-000 0000	57
11h	—	Unimplemented								—	—
12h	—	Unimplemented								—	—
13h	—	Unimplemented								—	—
14h	—	Unimplemented								—	—
15h	—	Unimplemented								—	—
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	—	Unimplemented								—	—
19h	—	Unimplemented								—	—
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRES	ADC Result Register								xxxx xxxx	71
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	CHS3	ADON	0000 0000	70

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter. See Section 2.9 for more detail.

2: These registers can be addressed from any bank.

TABLE 2-1: PIC16C781/782 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on Page:
Bank 1											
80h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
81h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	18
82h(2)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	23
83h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
84h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	23
85h	TRISA	PORTA Data Direction Register								1111 1111	26
86h	TRISB	PORTB Data Direction Register								1111 1111	35
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	23
8Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	19
8Ch	PIE1	LVDIE	ADIE	C2IE	C1IE	—	—	—	TMR1IE	0000 ---0	20
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	WDTON	OSCF	—	$\overline{POR}$	$\overline{BOR}$	---q 1-qq	22, 120
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	—	Unimplemented								—	—
95h	WPUB	PORTB Weak Pull-up Control								1111 1111	36
96h	IOCB	PORTB Interrupt-on-Change Control								1111 0000	36
97h	—	Unimplemented								—	—
98h	—	Unimplemented								—	—
99h	—	Unimplemented								—	—
9Ah	—	Unimplemented								—	—
9Bh	REFCON	—	—	—	—	VREN	VROE	—	—	---- 00--	61
9Ch	LVDCON	—	—	BGST	LVDEN	LV3	LV2	LV1	LV0	--00 0101	66
9Dh	ANSEL	Analog Channel Select								1111 1111	25
9Eh	—	Unimplemented								—	—
9Fh	ADCON1	—	—	VCFG1	VCFG0	—	—	—	—	--00 ----	71

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter. See Section 2.9 for more detail.

2: These registers can be addressed from any bank.

TABLE 2-1: PIC16C781/782 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on Page:
Bank 2											
100h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
101h	TMR0	Timer0 Module's Register								xxxx xxxx	51
102h(2)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	23
103h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
104h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	23
105h	—	Unimplemented								—	—
106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx 0000	35
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	23
10Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	19
10Ch	PMDATL	PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	0000 0000	48
10Dh	PMADRL	PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0	xxxx xxxx	48
10Eh	PMDATH	—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8	--00 0000	47
10Fh	PMADRH	—	—	—	Reserved	Reserved	PMA10	PMA9	PMA8	---x xxxx	48
110h	CALCON	CAL	CALERR	CALREF	—	—	—	—	—	000- ----	85
111h	PSMCCON0	SMCCL1	SMCCL0	MINDC1	MINDC0	MAXDC1	MAXDC0	DC1	DC0	0000 0000	104
112h	PSMCCON1	SMCON	S1APOL	S1BPOL	—	SCEN	SMCOM	PWM/$\overline{PSM}$	SMCCS	000- 0000	104
113h	—	Unimplemented								—	—
114h	—	Unimplemented								—	—
115h	—	Unimplemented								—	—
116h	—	Unimplemented								—	—
117h	—	Unimplemented								—	—
118h	—	Unimplemented								—	—
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	91
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	93
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	—	C2SYNC	00-- ---0	94
11Ch	OPACON	OPAON	CMPEN	—	—	—	—	—	GBWP	00-- ---0	84
11Dh	—	Unimplemented								—	—
11Eh	DAC	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	0000 0000	79
11Fh	DACON0	DAON	DAOE	—	—	—	—	DARS1	DARS0	00-- --00	79

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter. See Section 2.9 for more detail.

2: These registers can be addressed from any bank.

TABLE 2-1: PIC16C781/782 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on Page:
Bank 3											
180h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	18
182h(2)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	23
183h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
184h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	23
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	35
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	23
18Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	19
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	47
18Dh	—	Unimplemented								—	—
18Eh	—	Unimplemented								—	—
18Fh	—	Unimplemented								—	—
190h	—	Unimplemented								—	—
191h	—	Unimplemented								—	—
192h	—	Unimplemented								—	—
193h	—	Unimplemented								—	—
194h	—	Unimplemented								—	—
195h	—	Unimplemented								—	—
196h	—	Unimplemented								—	—
197h	—	Unimplemented								—	—
198h	—	Unimplemented								—	—
199h	—	Unimplemented								—	—
19Ah	—	Unimplemented								—	—
19Bh	—	Unimplemented								—	—
19Ch	—	Unimplemented								—	—
19Dh	—	Unimplemented								—	—
19Eh	—	Unimplemented								—	—
19Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter. See Section 2.9 for more detail.

2: These registers can be addressed from any bank.

2.3 STATUS Register

The STATUS register, shown in Register 2-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC, or C bits, the write to these three bits is disabled. These bits are set or cleared according to the device logic. The $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as the destination may be different than intended.

For example, `CLRF STATUS` clears the upper three bits and sets the Z bit. This leaves the STATUS register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, since these instructions do not affect the Z, C, or DC bits from the STATUS register. For other instructions not affecting any status bits, see the "Instruction Set Summary."

Note:	The C and DC bits operate as a $\overline{borrow}$ and digit $\overline{borrow}$ bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1: STATUS REGISTER (STATUS: 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
`1` = Bank 2, 3 (100h - 1FFh)
`0` = Bank 0, 1 (00h - FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
`11` = Bank 3 (180h - 1FFh)
`10` = Bank 2 (100h - 17Fh)
`01` = Bank 1 (80h - FFh)
`00` = Bank 0 (00h - 7Fh)
Each bank is 128 bytes

bit 4 **$\overline{TO}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for $\overline{borrow}$, the polarity is reversed)
`1` = A carry-out from the 4th low order bit of the result occurred
`0` = No carry-out from the 4th low order bit of the result

bit 0 **C:** Carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

Note: For $\overline{borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.4 OPTION_REG Register

The OPTION_REG register is a readable and writable register which contains various control bits to configure:

- TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler)
- External INT interrupt
- TMR0
- Weak pull-ups on PORTB

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

REGISTER 2-2: OPTION REGISTER (OPTION_REG: 81h, 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

bit 7 **$\overline{\text{RBPU}}$:** PORTB Pull-up Enable bit(1)
1 = PORTB weak pull-ups are disabled
0 = PORTB weak pull-ups are enabled by the WPUB register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: Individual weak pull-ups on RB pins can be enabled/disabled from the weak pull-up PORTB register (WPUB).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.5 INTCON Register

The INTCON register is a readable and writable register which contains:

- Enable and interrupt flag bits for TMR0 register overflow
- Enable and interrupt flag bits for the external interrupt (INT)
- Enable and interrupt flag bits for PORTB Interrupt-on-Change (IOCB)
- Peripheral interrupt enable bit
- Global interrupt enable bit

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTERRUPT CONTROL REGISTER (INTCON: 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T01E	INTE	RBIE	T0IF	INTF	RBIF
bit 7							bit 0

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3 **RBIE:** RB Port Change Interrupt Enable bit(1)
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **T0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0 **RBIF:** RB Port Change Interrupt Flag bit(1)
1 = When at least one of the RB7:RB0 pins changed state (must be cleared in software)
0 = None of the RB7:RB0 pins have changed state

Note 1: Individual RB pin interrupt-on-change can be enabled/disabled from the Interrupt-on-Change PORTB register (IOCB).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.6 PIE1 Register

The PIE1 register contains the individual enable bits for the peripheral interrupts.

Note:	Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt (see Register 2-3).

REGISTER 2-4: PERIPHERAL INTERRUPT ENABLE REGISTER (PIE1: 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
LVDIE	ADIE	C2IE	C1IE	—	—	—	TMR1IE
bit7							bit0

bit 7 **LVDIE:** Low Voltage Detect Interrupt Enable bit
1 = LVD interrupt is enabled
0 = LVD interrupt is disabled

bit 6 **ADIE:** Analog-to-Digital Converter Interrupt Enable bit
1 = Enables the Analog-to-Digital Converter interrupt
0 = Disables the Analog-to-Digital Converter interrupt

bit 5 **C2IE:** Comparator C2 Interrupt Enable bit
1 = Enables the Comparator C2 interrupt
0 = Disables the Comparator C2 interrupt

bit 4 **C1IE:** Comparator C1 Interrupt Enable bit
1 = Enables the Comparator C1 interrupt
0 = Disables the Comparator C1 interrupt

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **TMR1IE:** TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.7 PIR1 Register

This register contains the individual flag bits for the peripheral interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PERIPHERAL INTERRUPT REGISTER (PIR1 0Ch)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
LVDIF	ADIF	C2IF	C1IF	—	—	—	TMR1IF
bit7							bit 0

bit 7 **LVDIF:** Low Voltage Detect Interrupt Flag bit
1 = The supply voltage has fallen below the specified LVD voltage (must be cleared in software)
0 = The supply voltage is greater than the specified LVD voltage

bit 6 **ADIF:** Analog-to-Digital Converter Interrupt Flag bit
1 = An ADC conversion completed (must be cleared in software)
0 = The ADC conversion is not complete

bit 5 **C2IF:** Comparator C2 Interrupt Flag bit
1 = Comparator C2 input has crossed the threshold (must be cleared in software)
0 = Comparator C2 input has not crossed the threshold

bit 4 **C1IF:** Comparator C1 Interrupt Flag bit
1 = Comparator C1 input has crossed the threshold (must be cleared in software)
0 = Comparator C1 input has not crossed the threshold

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.8 PCON Register

The Power Control (PCON) register contains two flag bits to allow determination of the source of the most recent RESET:

- Power-on Reset ($\overline{POR}$)
- External $\overline{MCLR}$ Reset
- Power Supply Brown-out ($\overline{BOR}$) Reset

The Power Control register also contains frequency select bits for the INTRC oscillator and the WDT software enable bit.

Note: $\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if $\overline{BOR}$ is clear, indicating a brown-out has occurred. The $\overline{BOR}$ status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

Direction of Change	Typical Time Inactive	
	Minimum	Maximum
4 MHz → 37 kHz	100 μs	300 μs
37 kHz→4 MHz	1.25 μs	3.25 μs

Note: When changing the internal oscillator speed (i.e., the OSCF bit, INTRC mode), the processor will be inactive during the oscillator frequency change.

REGISTER 2-6: POWER CONTROL REGISTER (PCON: 8Eh)

U-0	U-0	U-0	R/W-q	R/W-1	U-0	R/W-q	R/W-q
—	—	—	WDTON	OSCF	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **WDTON:** WDT Software Enable bit

If WDTE bit (Configuration Word <3>) = 1:
This bit is not writable, always reads '1'

If WDTE bit (Configuration Word <3>) = 0:
1 = WDT is enabled
0 = WDT is disabled

bit 3 **OSCF:** Oscillator Speed INTRC Mode bit

1 = 4 MHz typical
0 = 37 kHz typical
All other oscillator modes (X = Ignored)

bit 2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit

1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit

1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred

Legend:			
q = Value depends on conditions			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.9 PCL and PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13-bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. All updates to the PCH register occur through the PCLATH register.

2.9.1 PROGRAM MEMORY PAGING

PIC16C781/782 devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When performing a CALL or GOTO instruction, the upper 2 bits of the address are provided by PCLATH<4:3>. When performing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. A return instruction pops a PC address off the stack onto the PC register. Therefore, manipulation of the PCLATH<4:3> bits is not required for the return instructions (which POPs the address from the stack).

2.10 Stack

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Mid-range devices have an 8-level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed, or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW, or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

2.11 INDF

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is known as *indirect addressing*.

Reading INDF itself, indirectly (FSR = 0), produces 00h. Writing to the INDF register indirectly results in a no operation (although STATUS bits may be affected).

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
          movlw  0x20  ;initialize pointer
          movwf  FSR   ;  to RAM
NEXT      clrf   INDF  ;clear INDF register
          incf   FSR   ;inc pointer
          btfss  FSR,4 ;all done?
          goto   NEXT  ;NO, clear next
CONTINUE
          :            ;YES, continue
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-5.

FIGURE 2-4: LOADING OF PC IN DIFFERENT SITUATIONS

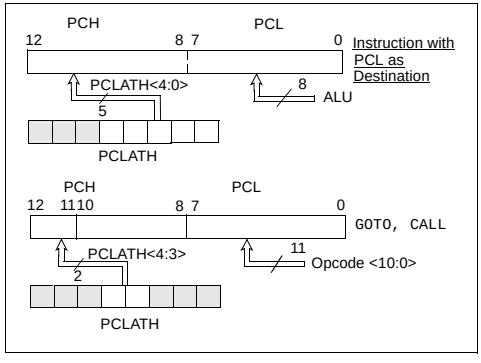
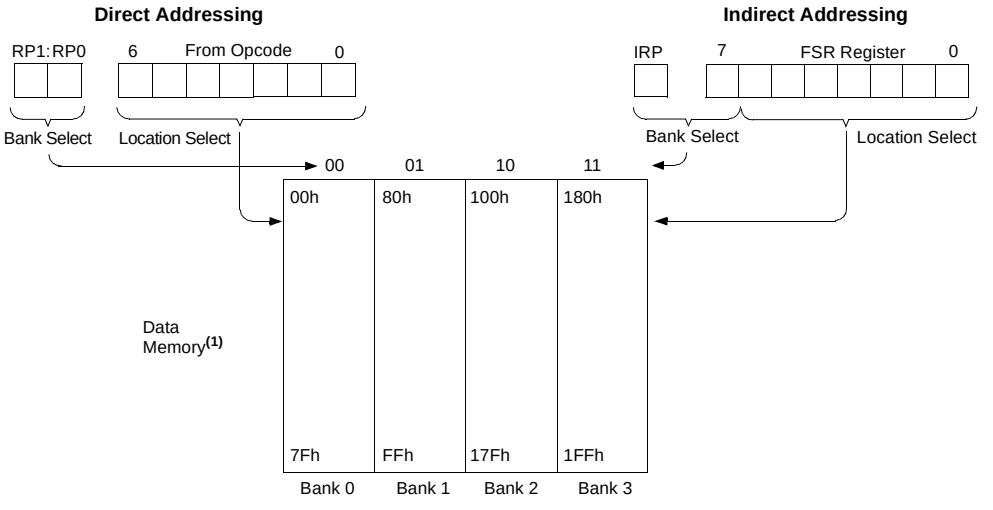


FIGURE 2-5: DIRECT/INDIRECT ADDRESSING



Note 1: For register file map detail, see Figure 2-3.

2.12 Effect of RESET on Core Registers

Refer to Table 2-2 for the effect of a RESET operation on core registers.

TABLE 2-2: EFFECT OF RESET ON CORE REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS(1)
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
0Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Ch	PIR1	LVDIF	ADIF	C2IF	C1IF	—	—	—	TMR1IF	0000 ---0	0000 ---0
Bank 1											
81h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	xxxx xxxx	1111 1111
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	LVDIE	ADIE	C2IE	C1IE	—	—	—	TMR1IE	0000 ---0	0000 ---0
8Eh	PCON	—	—	—	WDTON	OSCF	—	$\overline{POR}$	$\overline{BOR}$	---q 1-qq	---q 1-qq

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: Other (non power-up) RESETS include external RESET through $\overline{MCLR}$ and Watchdog Timer Reset.

3.0 I/O PORTS

Most pins for the I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PIC Mid-Range Reference Manual (DS33023)

3.1 I/O Port Analog/Digital Mode

The PIC16C781/782 has two I/O ports: PORTA and PORTB. Some of these port pins are mixed signal (can be digital or analog). When an analog signal is present on a pin, the pin must be configured as an analog input to prevent unnecessary current drawn from the power supply. The Analog Select register (ANSEL) allows the user to individually select the Digital/Analog mode on these pins. When the Analog mode is active, the port pin always reads as a logic 0.

Note 1: On a Power-on Reset, the ANSEL register configures these mixed signal pins as Analog mode: RA<3:0>, RB<3:0>.

2: If a pin is configured as Analog mode, the pin always reads '0', even if the digital output is active.

REGISTER 3-1: ANALOG SELECT REGISTER (ANSEL: 9Dh)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

bit 7-0 **ANS<7:0>:** Select Analog Input Function on AN<7:0> bits

1 = Analog input
0 = Digital I/O

Note: Setting a pin to an analog input disables the digital input buffer. The corresponding TRIS bit should be set to input mode when using pins as analog inputs.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

3.2 PORTA and the TRISA Register

PORTA is an 8-bit wide, bi-directional port with the exception of RA0, RA1 and RA5, which are inputs only. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) makes the corresponding PORTA pin an input (i.e., disables the digital output). Clearing a TRISA bit (= 0) makes the corresponding PORTA pin an output (i.e., disables the digital output).

Reading the PORTA register reads the status of the pins, whereas writing to it, writes to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is then modified and written to the port data latch.

Pins RA<3:0> are multiplexed with analog functions:

- Analog inputs AN<3:0> to the A/D Converter.
- VREF1 and VREF2 inputs to the comparators.
- OPAMP inverting/non-inverting inputs.

Note:	When the analog peripherals are using any of these pins as analog input/output, the ANSEL register must have the proper value to individually select the Analog mode of the corresponding pins.

Pins RA<7:4> are multiplexed with digital functions:

- Pin RA4 is multiplexed with the TMR0 module clock input.
- Pin RA5 is multiplexed with the device RESET ($\overline{MCLR}$) and programming input (VPP) function.
- Pins RA6 and RA7 are multiplexed with the oscillator/clock I/O functions. RA6 can also be configured as the TMR1 clock input.

PORTA has the following I/O characteristics:

- RA0, RA1, and RA5 are input only.
- RA4 is an open drain output. All other PORTA pins have full CMOS buffer outputs.
- All PORTA pins have Schmitt trigger inputs.

EXAMPLE 3-1: INITIALIZING PORTA

```
;*   This code block will configure PORTA
;*   as follows
;*    RA<7:4>   digital outputs
;*   RA<3:2>   digital inputs
;*   RA<1:0>   analog inputs
;*   RB<3:0>   digital I/O
;*  Note 1: RB<3:0> configured as digital I/O
;*  Note 2: RA<7:6> availability depends on
;*   the oscillator selection

    BANKSEL     PORTA       ; Select Bank 0
    CLRF        PORTA       ; Preset PORTA data
                            ;  reg
    BANKSEL     TRISA       ; Select Bank 1
    MOVLW       B'00001111'; Digital I/O
                            ;  config data
    MOVWF       TRISA       ; Configure PORTA
                            ;  digital
    MOVLW       B'00000011'; Analog I/O config
                            ;  data
    MOVWF       ANSEL       ; Configure PORTA
                            ;  analog
```

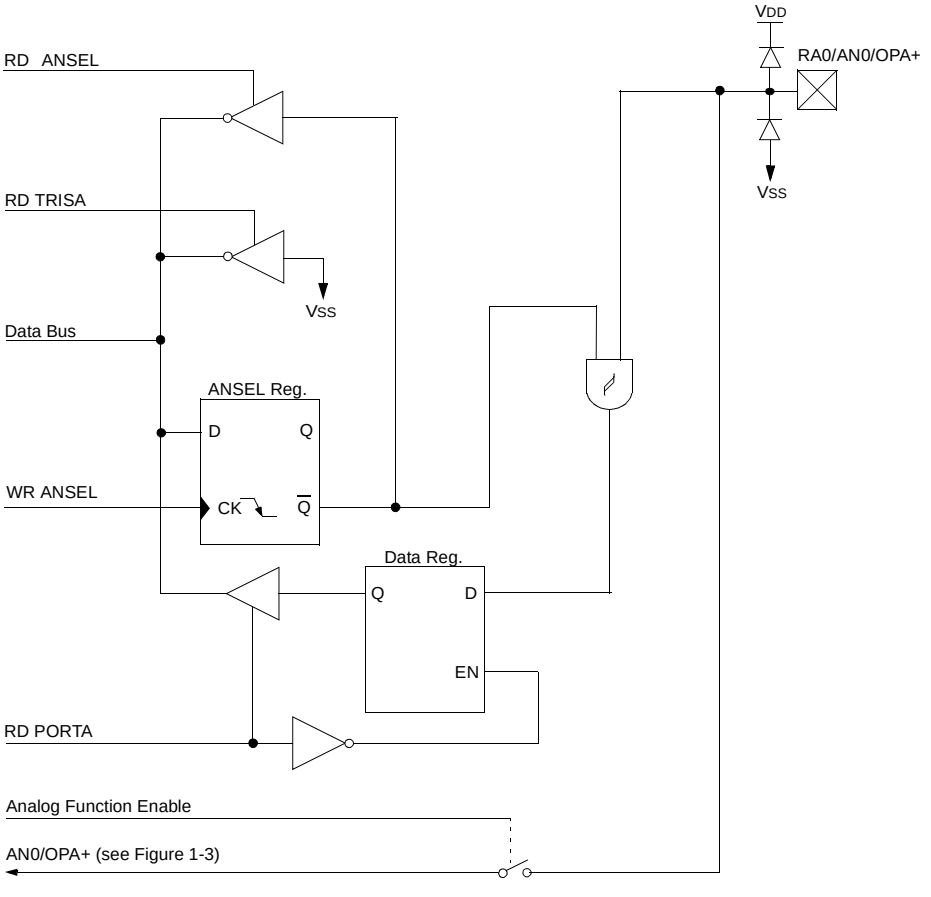
3.2.1 TRISA, ANSEL, AND CONTROL PRECEDENCE

The ANSEL and TRISA registers are the primary software controls for the configuration of PORTA pins. TRISA bits tri-state the output drivers of PORTA, and ANSEL register bits control the digital input buffers. It is important to program both registers when configuring a mixed signal port pin, as most peripherals cannot override the TRISA and ANSEL registers control. Even if a peripheral has the ability to override control of the TRISA and ANSEL registers, it is good programming practice to program both registers appropriately.

There are specific cases in which the TRISA and ANSEL registers can be overridden by a peripheral or a configuration bit, see Figures 3-1 through 3-8 for details.

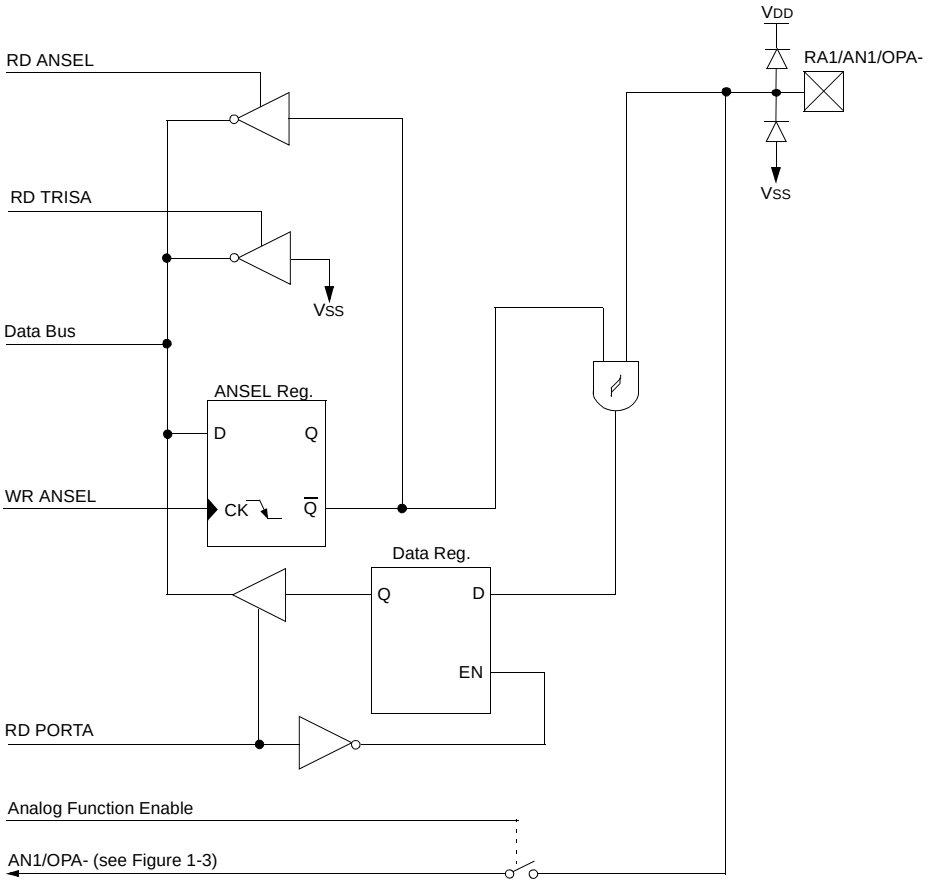
Note:	Crystal (LP, XT and HS) oscillator configurations use pin RA6/OSC2/CLKOUT/T1CKI as OSC2. In these modes, setting or clearing TRISA<6> will have no effect and the pin will read as a zero (0).

FIGURE 3-1: BLOCK DIAGRAM OF RA0/AN0/OPA+ PIN



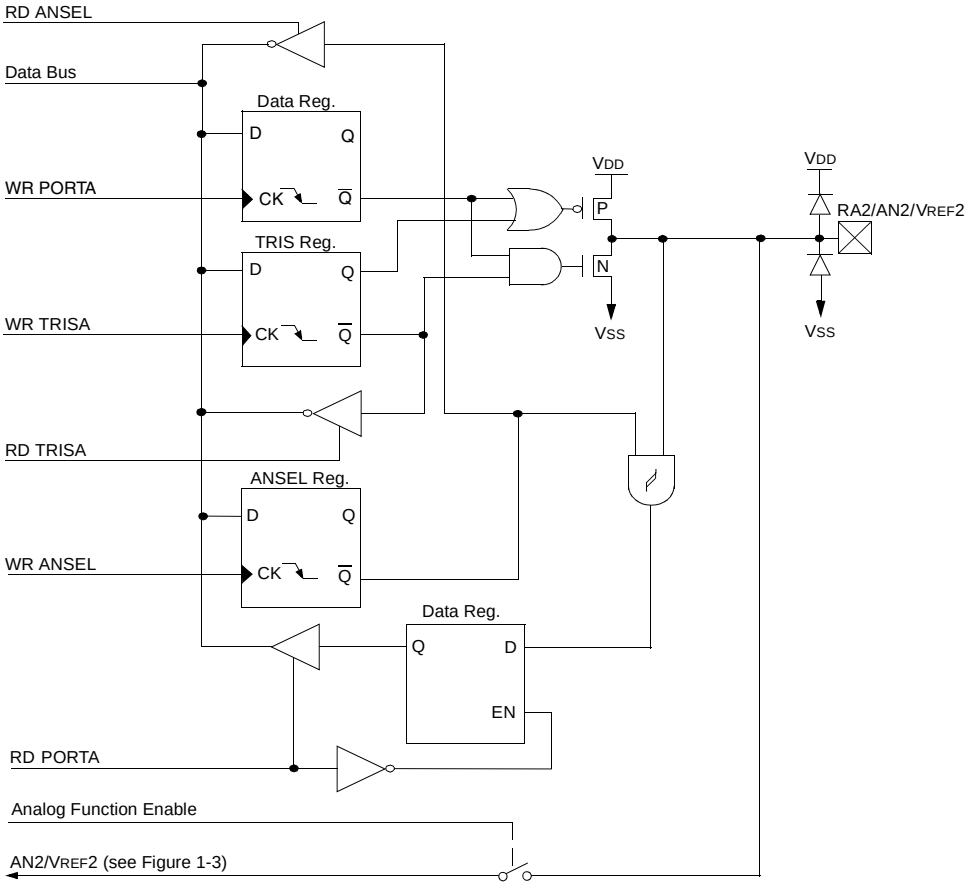
ANSEL<0>	TRISA<0>	FUNCTION	PORTA<0> READ
0	x	Digital In	Pin
1	x	Analog In	0

FIGURE 3-2: BLOCK DIAGRAM OF RA1/AN1/OPA- PIN



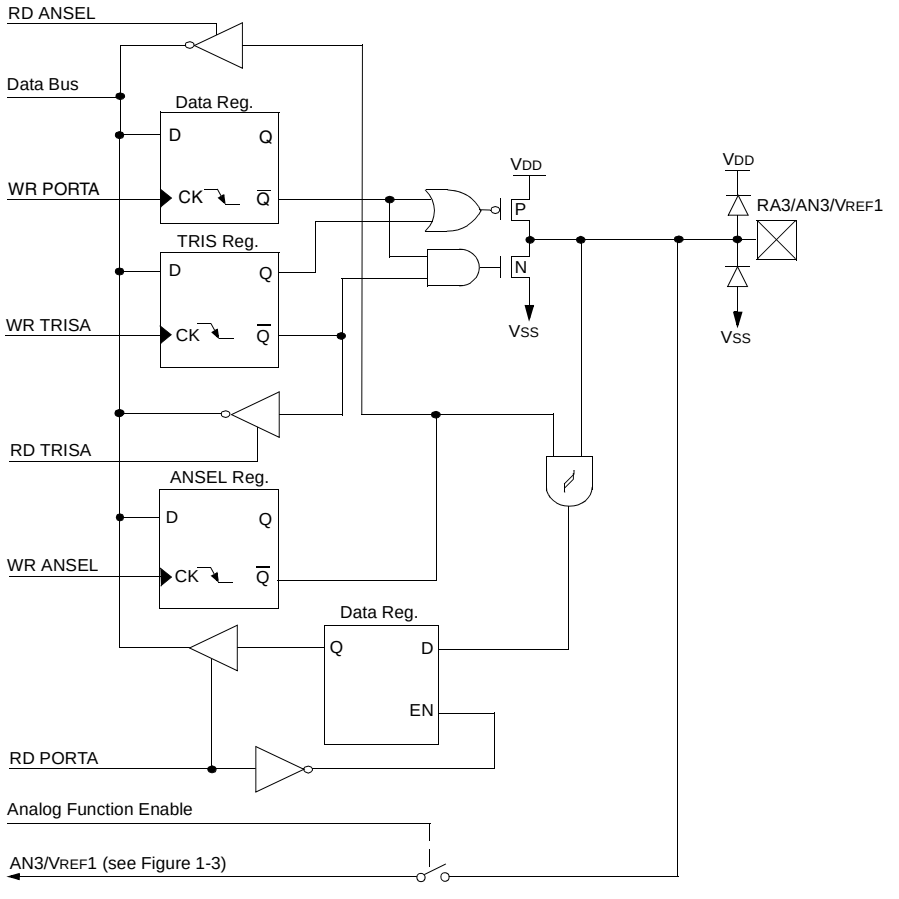
ANSEL<1>	TRISA<1>	FUNCTION	PORTA<1> READ
0	x	Digital In	Pin
1	x	Analog In	0

FIGURE 3-3: BLOCK DIAGRAM OF RA2/AN2/VREF2 PIN



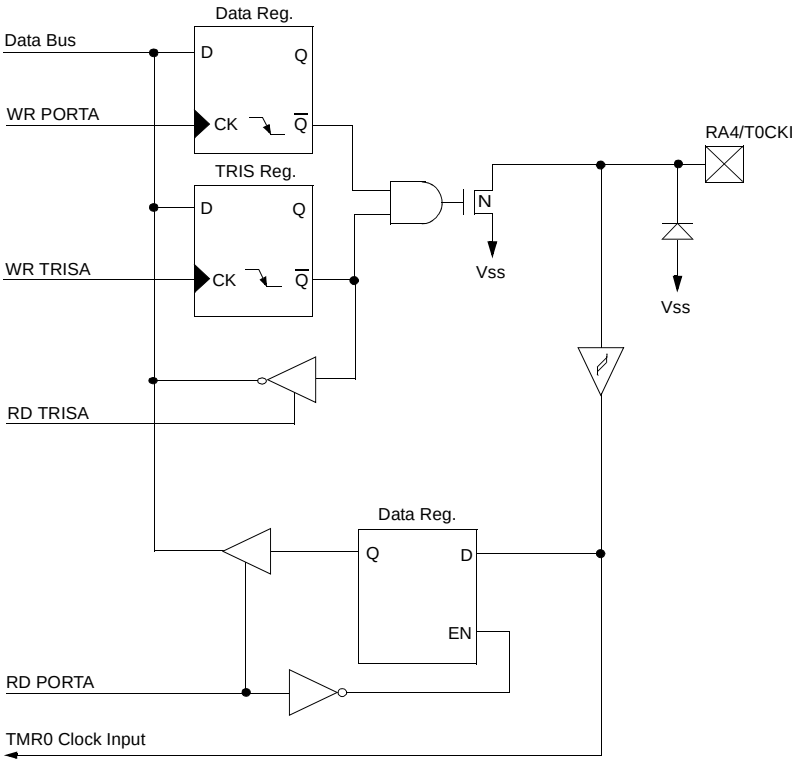
ANSEL<2>	TRISA<2>	FUNCTION	PORTA<2> READ
0	1	Digital In	Pin
0	0	Digital Out	Pin
1	x	Analog In	0

FIGURE 3-4: BLOCK DIAGRAM OF RA3/AN3/VREF1 PIN



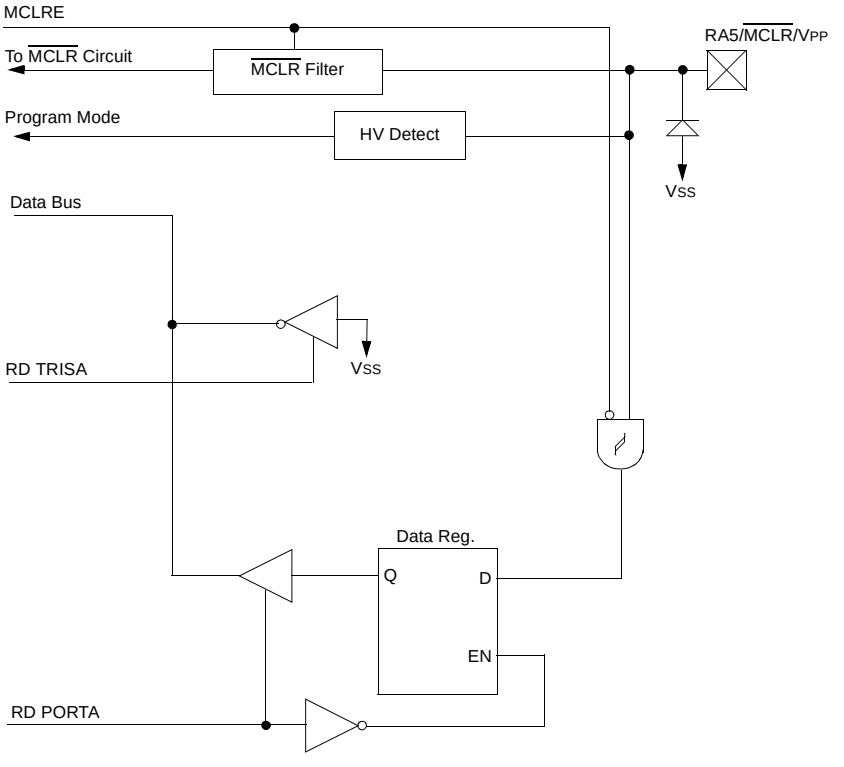
ANSEL<3>	TRISA<3>	FUNCTION	PORTA<3> READ
0	1	Digital In	Pin
0	0	Digital Out	Pin
1	x	Analog In	0

FIGURE 3-5: BLOCK DIAGRAM OF RA4/T0CKI PIN



TRISA<4>	PORTA<4>	FUNCTION	PORTA<4> READ
1	x	Digital In	Pin
0	0	0 Output	Pin
0	1	Hi-Z Output	Pin

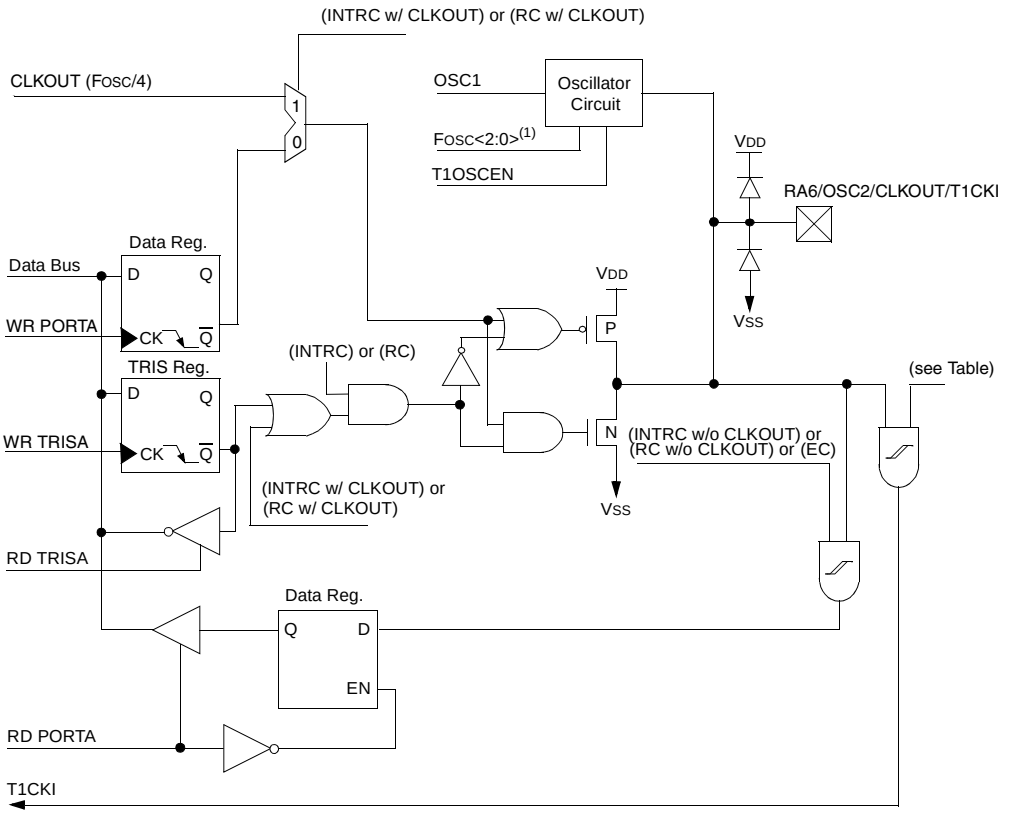
FIGURE 3-6: BLOCK DIAGRAM OF RA5/$\overline{\text{MCLR}}$/VPP PIN



MCLRE(1)	TRISA<5>	FUNCTION	PORTA<5> READ
Internal	x	Digital In	Pin
External	x	$\overline{\text{MCLR}}$	0

Note 1: See Configuration Word <5>, Register 14-1.

FIGURE 3-7: BLOCK DIAGRAM OF RA6/OSC2/CLKOUT/T1CKI PIN

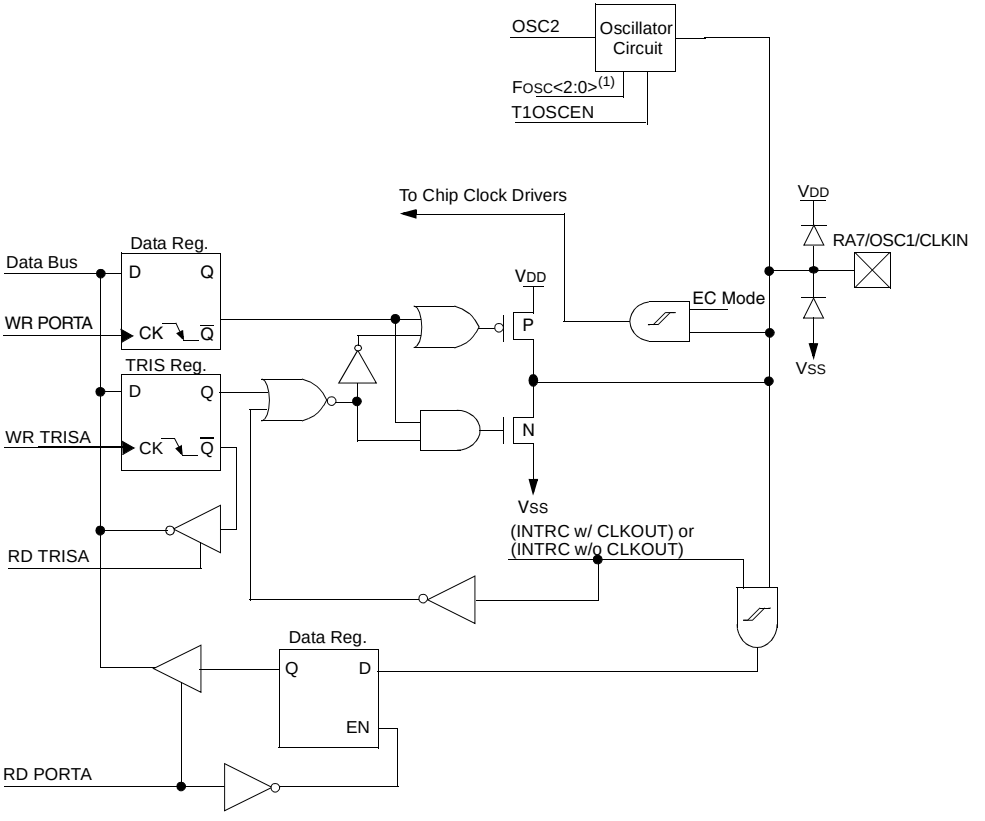


OSC MODE(1)	TMR1 OSCILLATOR	PIN FUNCTION	T1CKI	PORTA<6> READ
LP, XT, HS	N/A	OSC2	N/A	0
RC, INTRC w/ CLKOUT	N/A	CLKOUT	N/A	0
INTRC w/o CLKOUT	Enabled	OSC2 (TMR1)	N/A	0
INTRC w/o CLKOUT	Disabled	Digital I/O	Available	Pin
RC w/o CLKOUT	N/A	Digital I/O	Available	Pin
EC	N/A	Digital I/O	Available	Pin

N/A = Not Available w/ = with w/o = without

Note 1: See Configuration Word Fosc<2:0>, Register 14-1.

FIGURE 3-8: BLOCK DIAGRAM OF RA7/OSC1/CLKIN PIN



OSC MODE(1)	TMR1 OSCILLATOR	PIN FUNCTION	PORTA<7> READ
LP, XT, HS	N/A	OSC1	0
RC	N/A	OSC1	0
EC	N/A	CLKIN	0
INTRC	Enabled	OSC1 (TMR1)	0
INTRC	Disabled	Digital I/O	Pin

N/A = Not Available

Note 1: See Configuration Word FOSC<2:0>, Register 14-1.

TABLE 3-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000	uuuu 0000
85h	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
9Dh	ANSEL	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTA.

3.3 PORTB and the TRISB Register

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) makes the corresponding PORTB pin an input (i.e., puts the corresponding output driver into a Hi-Impedance mode). Clearing a TRISB bit (= 0) makes the corresponding PORTB pin an output (i.e., puts the contents of the output latch on the selected pin.

EXAMPLE 3-2: INITIALIZING PORTB

```
;* This code block will configure PORT B
;* as follows
;*  RB<7:6> analog inputs
;*  RB<5:4> digital inputs
;*  RB<3:2> digital inputs
;*  RB<1:0> digital inputs
;*  RA<3:0> digital I/O

    BANKSEL     PORTB       ; Select Bank 0
    CLRF        PORTB       ; Preset PORTB data
                            ; reg.
    BANKSEL     TRISB       ; Select Bank 1
    MOVLW       B'11001111' ; Digital I/O
                            ;   config data
    MOVWF       TRISB       ; Configure PORTB
                            ; digital
    MOVLW       B'00000011' ; Analog I/O config
                            ; data
    MOVWF       ANSEL       ; Configure PORTB
                            ; analog
```

The RB0 pin can be configured as:

- Digital I/O
- ADC/Comparator Analog Input (AN4)
- External Interrupt (INT)
- Voltage Reference Output (V_R)

When the pin is used as an analog I/O, the ANSEL register must have bit 4 set to configure the RB0 pin as an analog input.

Pin RB1 is multiplexed with two analog functions: ADC/Comparator Analog Input AN5, and the output of the DAC. When the pin is used as an analog I/O, the ANSEL register must have bit 5 set to configure the RB1 pin as an analog I/O.

Pin RB2 is multiplexed with the analog function ADC/Comparator Input AN6. When the pin is used as an analog input, the ANSEL register must have bit 6 to select the Analog mode for the pin.

The RB3 pin is multiplexed with two analog functions: ADC/Comparator Analog Input AN7, and the output of the OPA module. When the pin is used as analog I/O, the ANSEL register must have bit 7 set to select the Analog mode of the pin.

Pins RB<7:6> are multiplexed with the outputs of the two on-board comparators, the outputs of the PSMC module, and the clock gate input for Timer1. Note, when enabled, these peripherals override the PORTB data register; however, TRISB retains control of output drivers. Therefore, TRISB<7:6> must be programmed appropriately for Comparator and PSMC outputs to operate.

3.3.1 PORTB WEAK PULL-UP

Each of the PORTB pins has an internal weak pull-up resistance, which can be individually enabled from the WPUB register. A single global enable bit, $\overline{\text{RBPU}}$ (OPTION_REG<7>), can turn on/off all of the selected pull-ups. Clearing the $\overline{\text{RBPU}}$ bit (OPTION_REG<7>) enables the weak pull-up resistors (see Register 3-2). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

3.3.2 PORTB INTERRUPT-ON-CHANGE

Each of the PORTB pins, if configured as input, has the ability to generate an interrupt-on-change. To enable the interrupt-on-change feature, the corresponding bit must be set in the IOCB register (see Register 3-3). The RBIE bit in the INTCON register functions as a global enable bit to turn on/off the interrupt-on-change feature. The selected inputs are compared to the old value latched on the last read of PORTB. The "mismatch" outputs are OR-ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

The IOCB interrupt can also awaken the device from SLEEP. The user, in the Interrupt Service Routine, must clear the interrupt in the following manner:

a) A read or write to PORTB. This copies the current state into the latch and ends the mismatch condition.

b) Clear flag bit RBIF.

REGISTER 3-2: WEAK PULL-UP PORTB REGISTER (WPUB: 95h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0
bit7							bit0

bit 7-0 **WPUB<7:0>:** PORTB Weak Pull-Up Control bits

1 = Weak pull-up enabled for corresponding pin

0 = Weak pull-up disabled for corresponding pin

Note 1: For the WPUB register setting to take effect, the $\overline{\text{RBPU}}$ bit in the OPTION_REG register must be cleared.

2: The weak pull-up device is automatically disabled if the pin is in output mode, i.e., (TRISB = 0) for corresponding pin.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 3-3: INTERRUPT-ON-CHANGE PORTB REGISTER (IOCB: 96h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
bit7							bit0

bit 7-0 **IOCB<7:0>:** Interrupt-on-Change PORTB Control bits

1 = Interrupt-on-change enabled for corresponding pin

0 = Interrupt-on-change disabled for corresponding pin

Note 1: The interrupt enable bits, GIE and RBIE in the INTCON register, must be set for individual interrupts to be recognized.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

3.3.3 TRISB, ANSEL, AND CONTROL PRECEDENCE

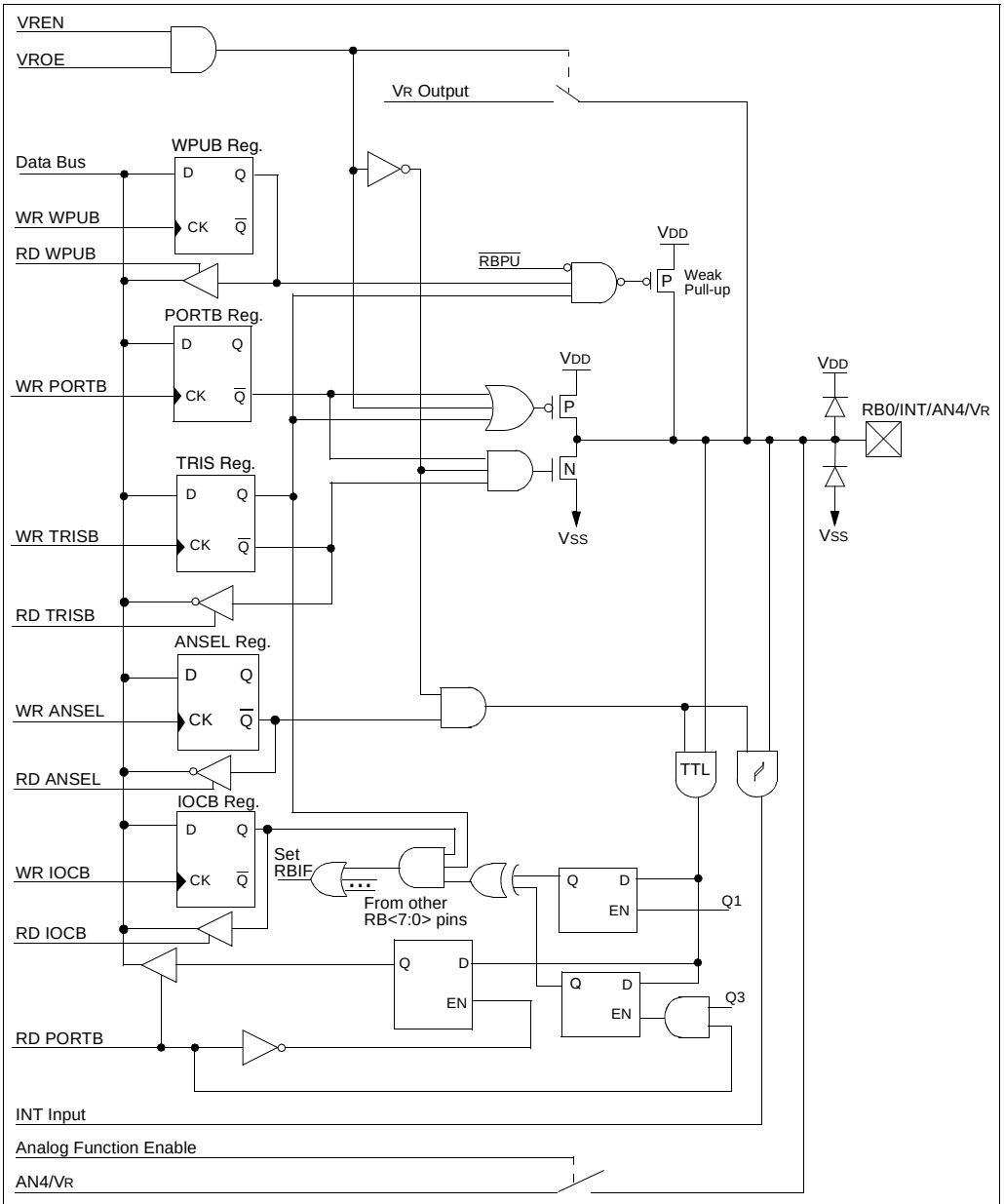
The ANSEL and TRISB registers are the primary controls for the configuration of PORTB pins. TRISB tri-states the output drivers of PORTB, and the ANSEL register disables the input buffers. It is important to program both registers when configuring a port pin, since most peripherals do not have precedence over the TRISB and ANSEL registers' control of the pin. Even if a peripheral has the ability to override the control of the TRISB and ANSEL registers, it is good practice to program both registers appropriately.

Note 1: Upon RESET, the ANSEL register configures the RB<3:0> pins as analog inputs.

2: When programmed as analog inputs, RB<3:0> pins will read as '0'.

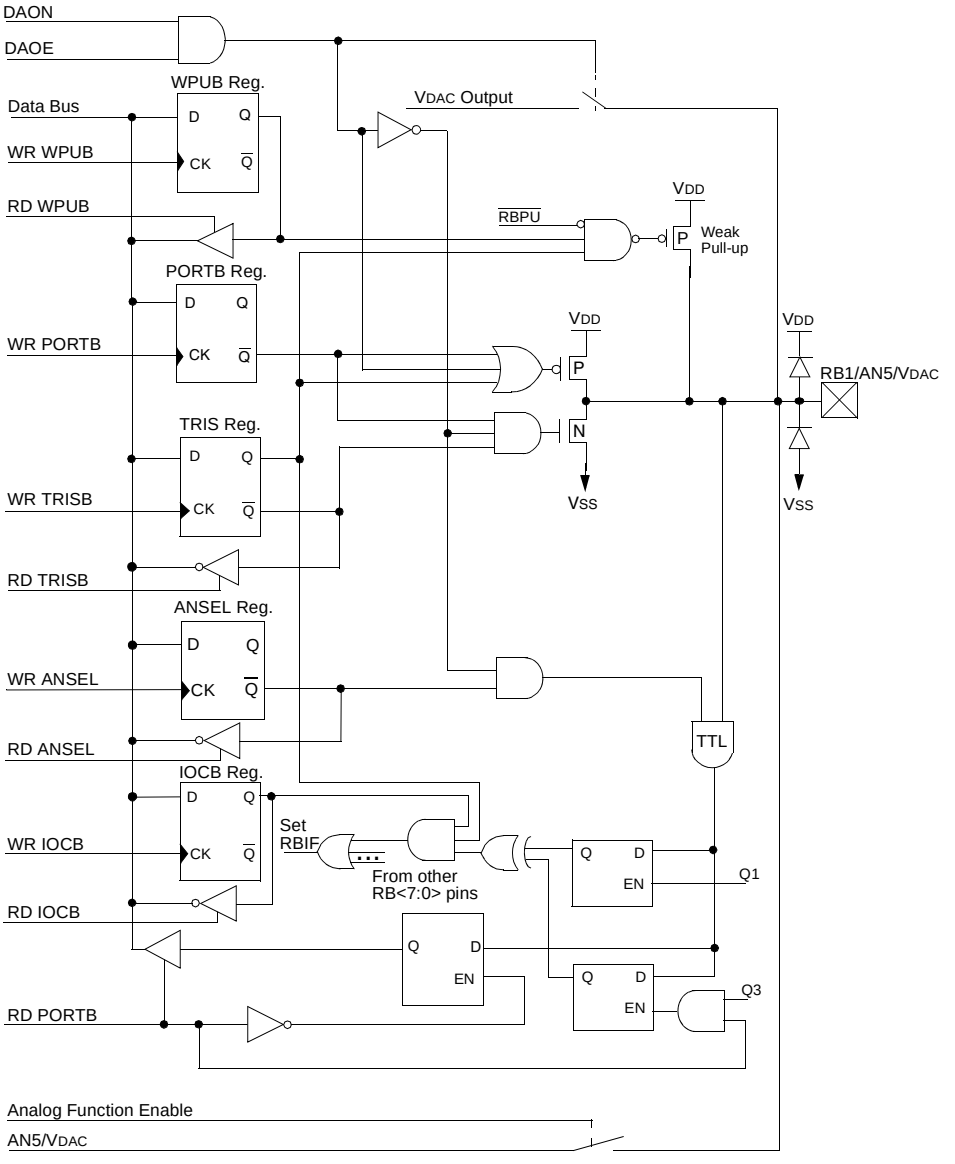
3: There are specific cases in which the functions of the TRISB and ANSEL registers can be overridden by a peripheral or configuration word (see Figure 3-9 through Figure 3-16 for details).

FIGURE 3-9: BLOCK DIAGRAM OF RB0/INT/AN4/VR PIN



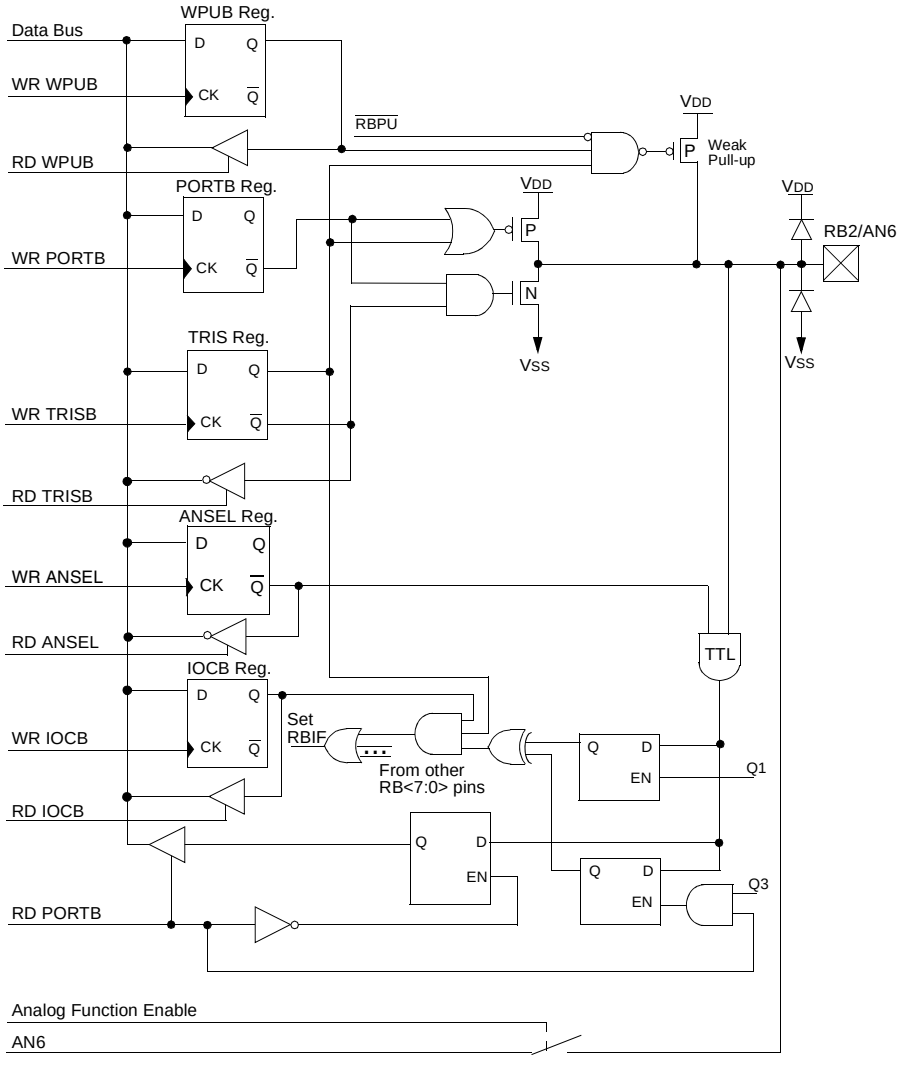
VREN & VROE	ANSEL<4>	TRISB<0>	FUNCTION	PORTB<0> READ
0	0	1	Digital In	Pin
0	0	0	Digital Out	Pin
0	1	x	Analog In	0
1	x	x	Analog Out	0

FIGURE 3-10: BLOCK DIAGRAM OF RB1/AN5/VDAC PIN



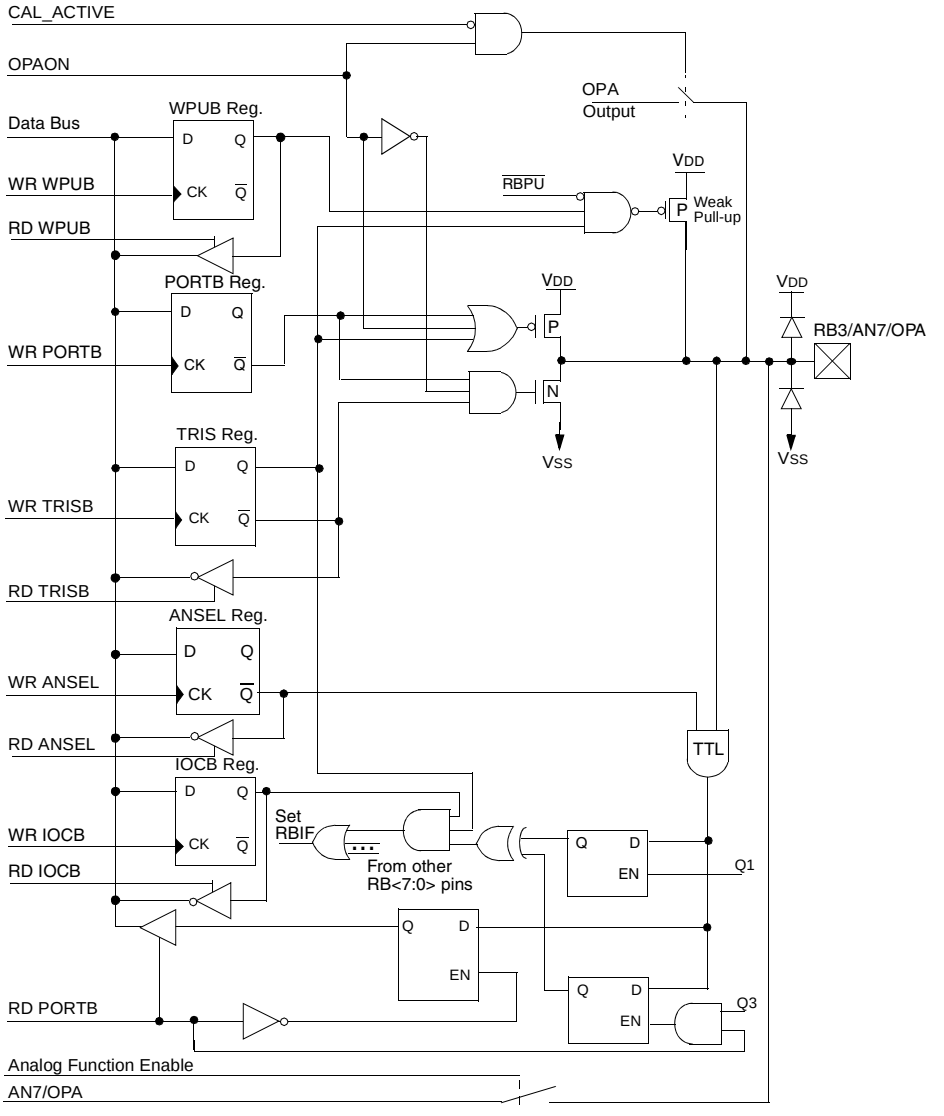
DAON & DAOE	ANSEL<5>	TRISB<1>	FUNCTION	PORTB<1> READ
0	0	1	Digital In	Pin
0	0	0	Digital Out	Pin
0	1	x	Analog In	0
1	x	x	Analog Out	0

FIGURE 3-11: BLOCK DIAGRAM OF RB2/AN6 PIN



ANSEL<6>	TRISB<2>	FUNCTION	PORTB<2> READ
0	1	Digital In	Pin
0	0	Digital Out	Pin
1	x	Analog In	0

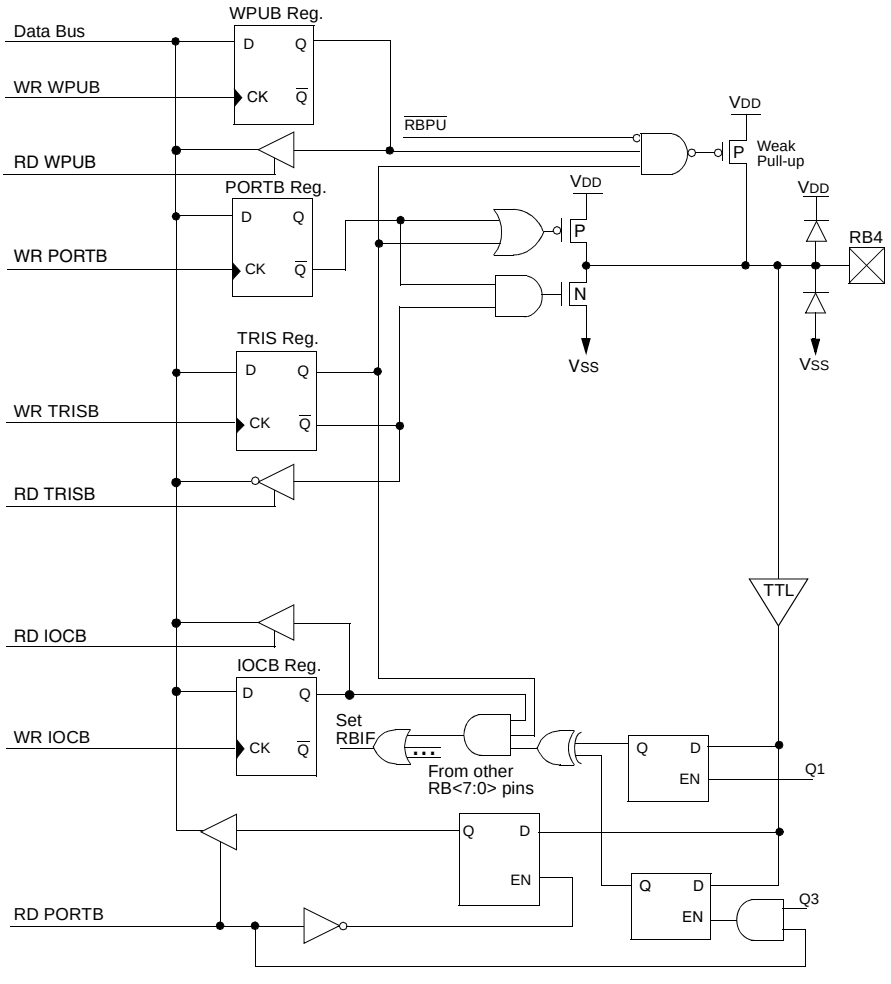
FIGURE 3-12: BLOCK DIAGRAM OF RB3/AN7/OPA PIN



OPA MODULE		ANSEL<7>	ADC/C1/C2 INPUT	FUNCTION	PORTB<3> READ
OPAON	CAL_ACTIVE				
0	x	0	Digital	Digital I/O	Pin
0	x	1	Analog	Analog In	0
1	0	1	Analog	OPA Output	0
1	1	1	Analog HI-Z	Calibration	0

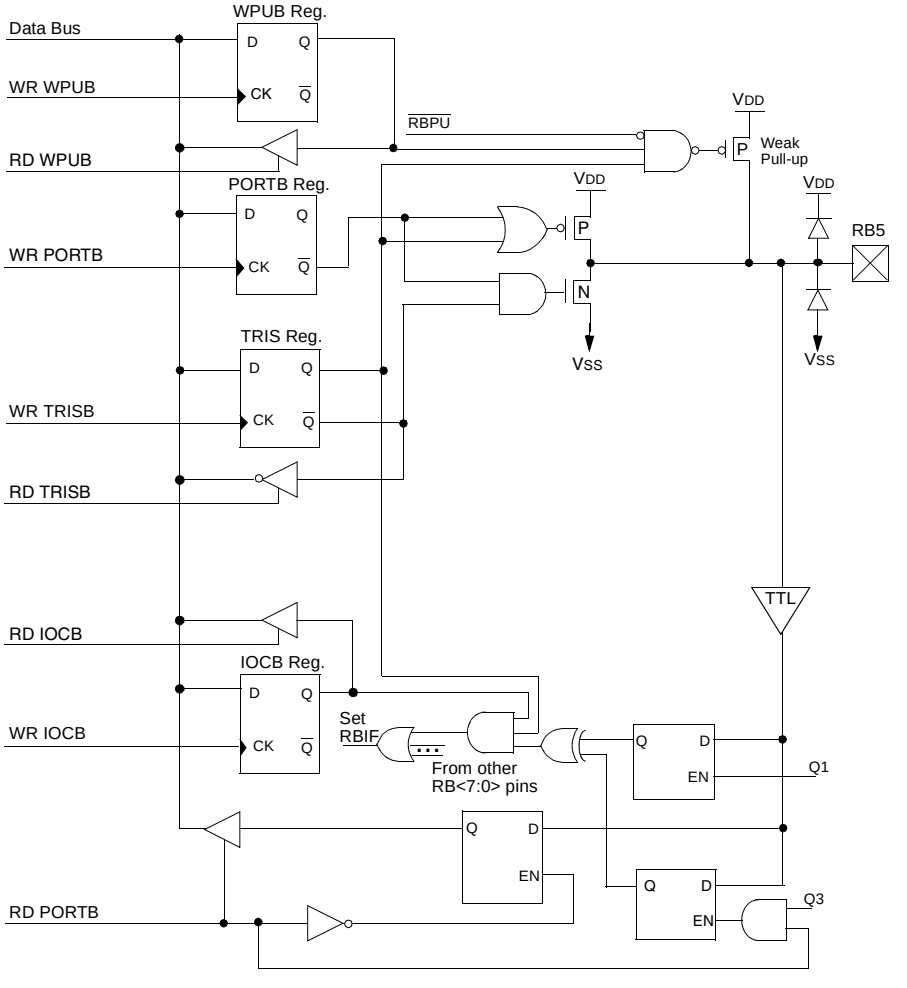
Analog HI-Z = No internal drive on pin (analog input) during calibration.

FIGURE 3-13: BLOCK DIAGRAM OF RB4 PIN



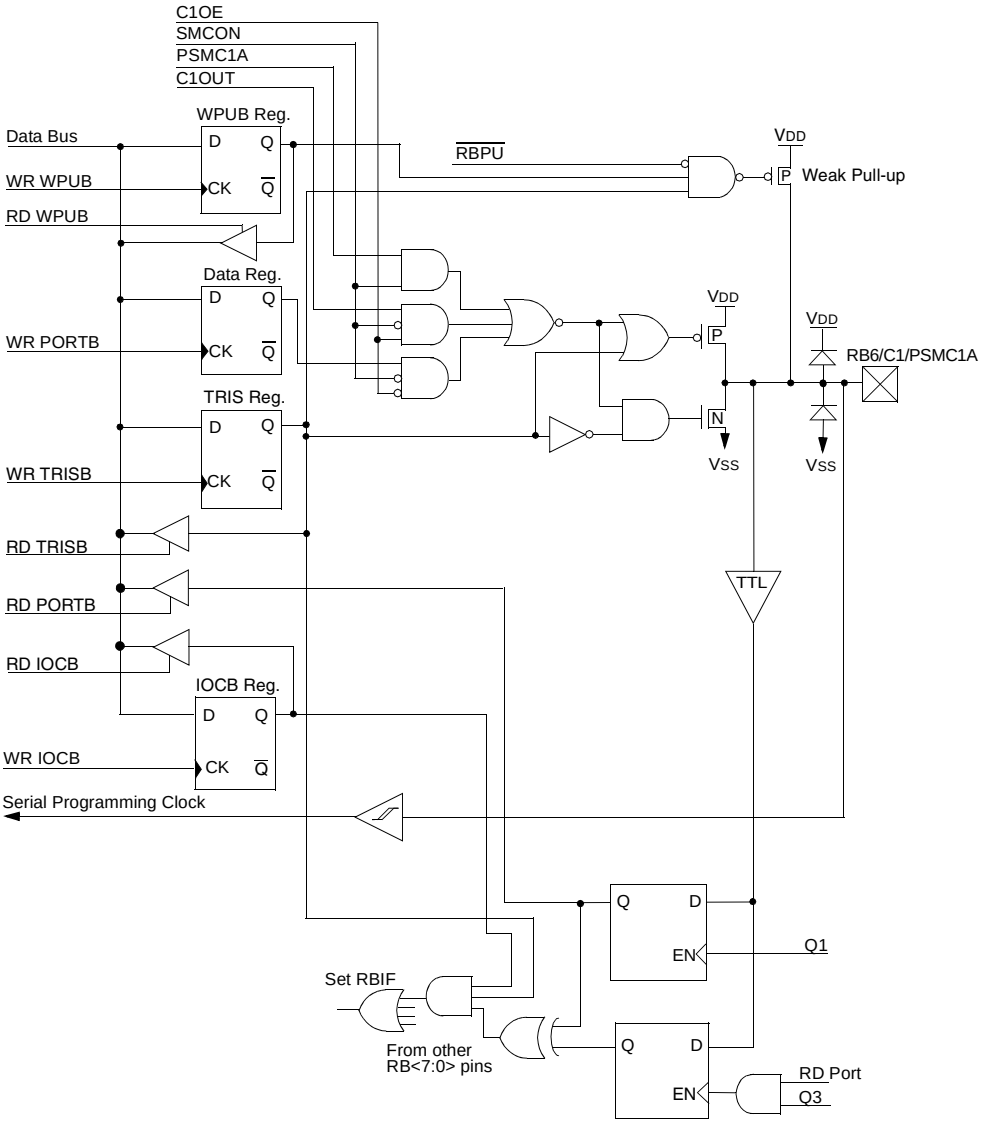
TRISB<4>	FUNCTION	PORTB<4> READ
0	Digital Out	Pin
1	Digital In	Pin

FIGURE 3-14: BLOCK DIAGRAM OF RB5 PIN



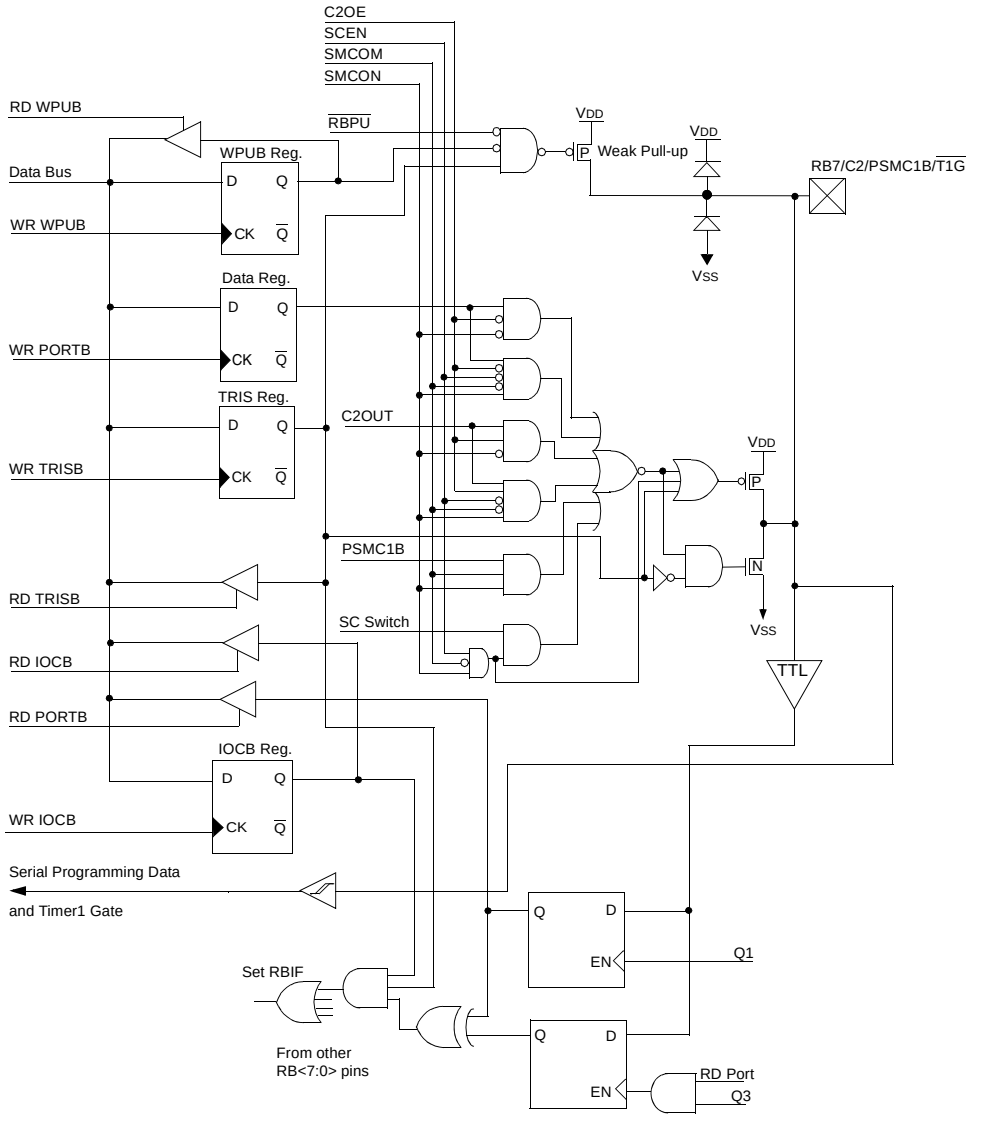
TRISB<5>	FUNCTION	PORTB<5> READ
0	Digital Out	Pin
1	Digital In	Pin

FIGURE 3-15: BLOCK DIAGRAM OF RB6/C1/PSMC1A PIN



PSMC SMCON	COMPARATOR C1OE	PORTB TRISB<6>	FUNCTION
x	x	1	Digital In
0	0	0	Digital Out
0	1	0	C1OUT
1	x	0	PSMC1A

FIGURE 3-16: BLOCK DIAGRAM OF RB7/C2/PSMC1B/$\overline{T1G}$ PIN



PSMC MODULE			COMPARATOR C2OE	PORTB TRISB<7>	FUNCTION
SMCON	SMCOM	SCEN			
x	x	x	x	1	Digital In
0	x	x	0	0	Digital Out
1	0	0	0	0	Digital Out
0	x	x	1	0	C2OUT
1	0	0	1	0	C2OUT
1	0	1	x	0	Slope Compensation
1	1	x	x	0	PSMC1B

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx 0000	uuuu 0000
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h	OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
95h	WPUB	PORTB Weak Pull-up Control								1111 1111	1111 1111
96h	IOCB	PORTB Interrupt-on-Change Control								1111 0000	1111 0000
9Dh	ANSEL	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTB.

NOTES:

4.0 PROGRAM MEMORY READ (PMR)

Program memory is readable during normal operation (full VDD range). It is read by indirect addressing through the following Special Function Registers:

- PMCON1: Control
- PMDATH: Data High
- PMDATL: Data Low
- PMADRH: Address High
- PMADRL: Address Low

When interfacing to the program memory block, the PMDATH and PMDATL registers form a 2-byte word, which holds the 14-bit data. The PMADRH and PMADRL registers form a 2-byte word, which holds the 12-bit address of the program memory location being accessed. Mid-range devices have up to 8K words of program EPROM with an address range from 0h to 3FFFh. When the device contains less memory than the full address range of the PMADRH:PMARDL registers, the Most Significant bits of the PMADRH register are ignored.

4.1 PMCON1 Register

PMCON1 is the control register for program memory accesses.

Control bit RD initiates a read operation. This bit cannot be cleared, only set, in software. It is cleared in hardware at completion of the read operation.

4.2 PMDATH and PMDATL Registers

The PMDATH:PMDATL registers are loaded with the contents of program memory addressed by the PMADRH and PMADRL registers upon completion of a Program Memory Read command.

REGISTER 4-1: PROGRAM MEMORY READ CONTROL REGISTER 1 (PMCON1: 18Ch)

R-1	U-0	U-0	U-0	U-0	U-0	U-0	R/S-0
Reserved	—	—	—	—	—	—	RD
bit7							bit0

bit 7 **Reserved:** Read as ‘1’

bit 6-1 **Unimplemented:** Read as '0

bit 0 **RD**: Read Control bit

1 = Initiates a Program memory read (read takes 2 cycles, RD is cleared in hardware)
0 = Reserved

Legend:			
S = Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

REGISTER 4-2: PROGRAM MEMORY DATA HIGH (PMDATH: 10Eh)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8
bit7							bit0

bit 7-6 **Unimplemented:** Read as '0

bit 5-0 **PMD<13:8>:** Program Memory Data bits
The value of the program memory word pointed to by PMADRH and PMADRL after a program memory read command.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

REGISTER 4-3: PROGRAM MEMORY DATA LOW (PMDATL: 10Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0
bit7							bit0

bit 7-0 **PMD<7:0>:** Program Memory Data bits
The value of the program memory word pointed to by PMADRH and PMADRL after a program memory read command.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 4-4: PROGRAM MEMORY ADDRESS HIGH (PMADRH: 10Fh)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	Reserved	Reserved	PMA10	PMA9	PMA8
bit7							bit0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-3 **Reserved:** Read state is not guaranteed

bit 2-0 **PMA<10:8>**: PMR Address bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 4-5: PROGRAM MEMORY ADDRESS LOW (PMADRL: 10Dh)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0
bit7							bit0

bit 7-0 **PMA<7:0>:** PMR Address bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.3 Reading the EPROM Program Memory

To read a program memory location, the user must write 2 bytes of the address to the PMADRH and PMADRL registers, then set control bit RD (PMCON1<0>). Once the read control bit is set, the Program Memory Read (PMR) controller uses the second instruction cycle after to read the data. This causes the second instruction immediately following the "BSF PMCON1,RD" instruction to be ignored. The data is available, in the very next cycle, in the PMDATH and PMDATL registers. Therefore, it can be read as 2 bytes in the following instructions. PMDATH and PMDATL registers hold this value until another read or until RESET.

Note 1: Interrupts must be disabled during the time from setting PMCON1<0> (RD) to the second instruction thereafter.

2: The following instructions should not be used following the start of a PMR read cycle: CALL, GOTO, BTFSS, BTFSC, RETFIE, RETURN, SLEEP.

EXAMPLE 4-1: OTP PROGRAM MEMORY READ

```
;* This code block will read 1 word of program
;* memory at the memory address:
;* PROG_ADDR_HI : PROG_ADDR_LO
;*  data will be returned in the variables;
;*     PROG_DATA_HI, PROG_DATA_LO


    BANKSEL     PMADRL          ; Select Bank 2
    MOVLW       PROG_ADDR_LO    ;
    MOVWF       PMADRL          ; Store LSB of address
    MOVLW       PROG_ADDR_HI    ;
    MOVWF       PMADRH          ; Store MSB of address

    BANKSEL     PMCON1          ; Select Bank 3
    CLEAR GIE
    BCF         INTCON, GIE     ; Turn off INTs
    BSF         PMCON1,RD       ; Initiate read
    NOP                         ; Executed (Fig 4-1)
     NOP                        ; Ignored (Fig 4-1)
    BSF         INTCON, GIE     ; Turn on INTs
    MOVF        PMDATL,W        ; Get LSB of word
    MOVWF       PROG_DATA_LO
    MOVF        PMDATH,W        ; Get MSB of word
    MOVWF       PROG_DATA_HI
```

4.4 Program Memory Read With Code Protect Set

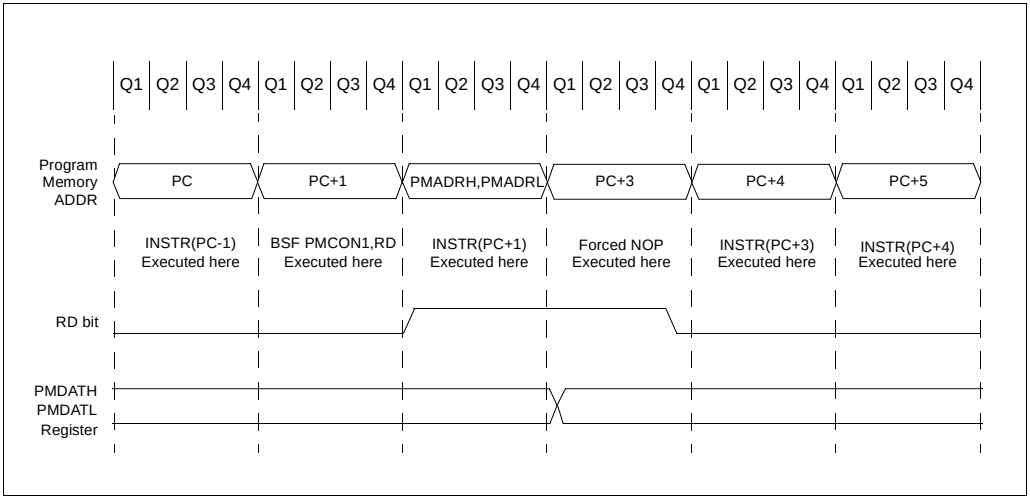
When the device is code protected, the CPU can still perform the program memory read function.

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH PMR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
10Ch	PMDATL	PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	0000 0000	0000 0000
10Dh	PMADRL	PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0	xxxx xxxx	uuuu uuuu
10Eh	PMDATH	—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8	--00 0000	--00 0000
10Fh	PMADRH	—	—	—	Reserved	Reserved	PMA10	PMA9	PMA8	---x xxxx	---u uuuu
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	1--- ---0

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PMR.

FIGURE 4-1: PROGRAM MEMORY READ CYCLE EXECUTION



5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt on overflow from FFh to 00h

Figure 5-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PIC Mid-Range Reference Manual, (DS33023).

5.1 Timer0 Operation

Timer0 can operate as either a timer or a counter.

Programming Timer0 is via the OPTION register (see Register 2-2).

Timer0 mode is selected by clearing/setting the bit T0CS (OPTION_REG<5>). In Timer mode (T0CS = 0), the Timer0 module increments every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In Counter mode, Timer0 increments either on every rising, or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge, setting selects the falling edge. Restrictions on the external clock input are discussed below.

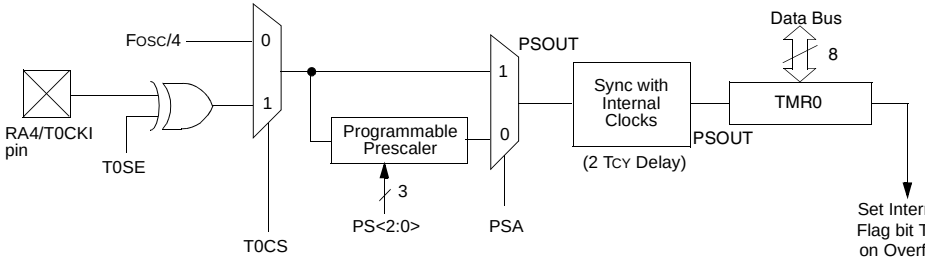
When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal system clock. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

Additional information on external clock requirements is available in the PIC Mid-Range Reference Manual, (DS33023).

EXAMPLE 5-1: INITIALIZING TIMER0

```
;* This code block will configure Timer0
;* for Polling, internal clock & 1:16
;*  prescaler
;*
;* Wait for TMR0 overflow code included
    BANKSEL     TMR0            ; Select Bank 0
    CLRF        TMR0            ; Clear Timer0
                                ; Register

    BANKSEL     OPTION_REG      ; Select Bank 1

    MOVLW       B'11000011'     ; INT on L2H
    MOVWF       OPTION_REG      ; Internal clk,
                                ; pscaler 1:16
*****************************************
;*  Wait for TMR0 overflow
;*
T0_OVFL_WAIT
    TBFSS       INTCON,T0IF     ; Check for TMR0
                                ; overflow
    GOTO        T0_OVFL_WAIT    ; If clear, test
                                ; again
    BCF         INTCON,T0IF     ; Clear interrupt
```

FIGURE 5-1: TIMER0 BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS<2:0> (OPTION_REG<5:0>).
2: The prescaler is shared with Watchdog Timer (refer to Figure 5-2 for detailed block diagram).

5.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 5-2). For simplicity, this counter is referred to as “prescaler” throughout this data sheet.

Note:	There is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS<2:0> bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

Clearing bit PSA assigns the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA assigns the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF TMR0, MOVWF TMR0, BSF TMR0, x....etc`.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction clears the prescaler along with the WDT.

Note:	Writing to TMR0 when the prescaler is assigned to Timer0 clears the prescaler count, but does not change the prescaler assignment.

5.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed “on-the-fly” during program execution.

Note:	To avoid an unintended device RESET, a specific instruction sequence (shown in the PIC Mid-Range Reference Manual, DS33023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

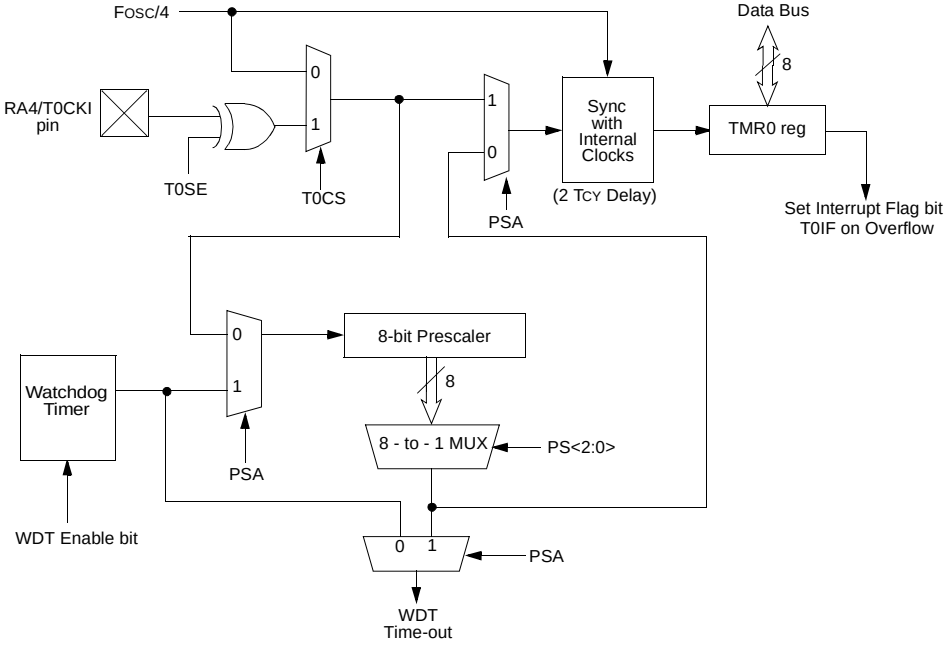
5.3 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP, since the timer is shut-off during SLEEP.

5.4 Effects of RESET

A device RESET will program Timer0 for an external clock input on RA4/T0CKI, Hi-Low edge, and no prescaler. The TMR0 register is not cleared.

FIGURE 5-2: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS<2:0> are (OPTION_REG<5:0>).

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
01h,101h	TMR0	Timer0 Register								xxxx xxxx	uuuu uuuu
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	ADIF	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h,181h	OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Timer0.

NOTES:

6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter
  (two 8-bit registers:TMR1H and TMR1L)
- Readable and writable (both registers)
- Internal or external clock select
- Interrupt on overflow from FFFFh to 0000h
- External enable input ($\overline{T1G}$ pin with TMR1GE bit = 1)
- Option for Timer1 to use LP oscillator if device is configured to use INTRC w/o CLKOUT

Timer1 Control register (T1CON) is shown in Register 6-1.

Figure 6-2 is a simplified block diagram of the Timer1 module.

6.1 Timer1 Operation

Timer1 can operate in one of three modes:

1. 16-bit timer with prescaler.
2. 16-bit synchronous counter.
3. 16-bit asynchronous counter.

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI (RA6/OSC2/CLKOUT/T1CKI). In addition, the Counter mode clock can be synchronized to the microcontroller clock or run asynchronously.

In Counter and Timer modes, the counter/timer clock can be gated by the $\overline{T1G}$ input.

If an external clock oscillator is needed (and the microcontroller is using INTRC w/o CLKOUT), Timer1 can use the LP oscillator as a clock source.

Note 1: In Counter mode, the counter increments on the rising edge of the clock.

EXAMPLE 6-1: TIMER1 INITIALIZATION

```
;* This code block will configure Timer1 for
;* Polling, Ext gate of int clk (Fosc/4), &
;* 1:1 prescaler.
;*
;* Wait for TMR1 overflow code included
;*
   BANKSEL  TMR1L           ; Select Bank 0
   CLRF     TMR1L           ; Clear TMR1 LSB
   CLRF     TMR1H           ; Clear TMR1 MSB
   MOVLW    B'01000000'     ; Gate, Ps 1:1
   MOVWF    T1CON           ; Int clk
   BSF      T1CON,TMR1ON    ; Enable timer

;*****************************************
;* Wait for TMR1 overflow

T1_OVFL_WAIT
   BANKSEL  PIR1            ; Select Bank 0
   T1_WAIT                  ;
   TBFSS    PIR1,TMR1IF     ; Overflow?
   GOTO     T1_WAIT         ; If 0, again

   BCF      PIR1,TMR1IF     ; Clear flag
```

6.2 Control Register T1CON

Control and configuration of Timer1 is by means of the T1CON register shown in Register 6-1.

Timer1 is enabled by setting the TMR1ON bit (T1CON<0>). Clearing TMR1ON stops the timer, but does not clear the Timer1 register.

The TMR1CS bit (T1CON<1>) determines the Timer mode. When TMR1CS is set, the timer is configured as a counter and receives its clock from RA6/OSC2/CLKOUT/T1CKI. When cleared, the timer is configured as a timer and its clock is derived from FOSC/4.

The $\overline{\text{T1SYNC}}$ bit (T1CON<2>) determines Timer1's synchronization. If cleared, the timer clock is synchronized to the system clock. If set, the timer is asynchronous.

The Timer1 clock gate function is enabled by setting the TMR1GE bit (T1CON<6>). When TMR1GE is set, the $\overline{\text{T1G}}$ input will control the clock input to the timer/counter. A low on the $\overline{\text{T1G}}$ input will cause Timer1 to increment at the clock rate, a high will hold the timer at its present value.

The T1OSCEN bit (T1CON<3>) enables the LP oscillator as a clock source for Timer1. This mode is a replacement for the regular external oscillator.

T1CKPS<1:0> determines the prescaler value for the timer. Available prescaler values are:

T1CKPS<1:0>		Prescaler Value
Bit 1	Bit 0	
1	1	1:8
1	0	1:4
0	1	1:2
0	0	1:1

Note: To use the LP oscillator as the Timer1 oscillator:
1. TMR1CS must be set.
2. T1OSCEN must be set.
3. The Configuration Word must select INTRC w/o CLKOUT.

REGISTER 6-1: TIMER1 CONTROL REGISTER (T1CON: ADDRESS 10h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6 **TMR1GE:** Timer1 Gate Enable bit

If TMR1ON = 0:
This bit is ignored

If TMR1ON = 1:
1 = Timer1 is on if $\overline{\text{T1G}}$ pin is low
0 = Timer1 is on

bit 5-4 **T1CKPS<1:0>**: Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T1OSCEN**: LP Oscillator Enable Control bit

If INTRC w/o CLKOUT is selected in the configuration word, oscillator is active:
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off

Else:
This bit is ignored

bit 2 **$\overline{\text{T1SYNC}}$**: Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input

TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1 **TMR1CS**: Timer1 Clock Source Select bit

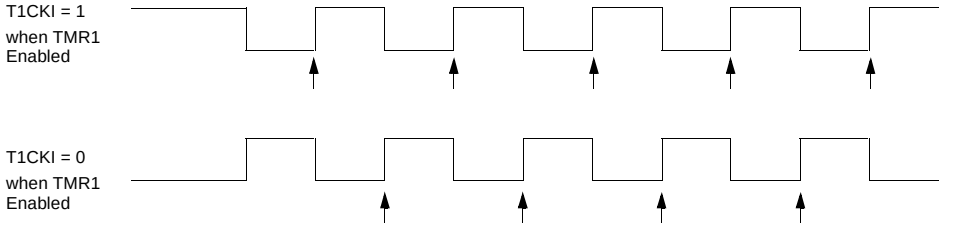
1 = External clock from pin RA6/OSC2/CLKOUT/T1CKI (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON**: Timer1 On bit

1 = Enables Timer1
0 = Stops Timer1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

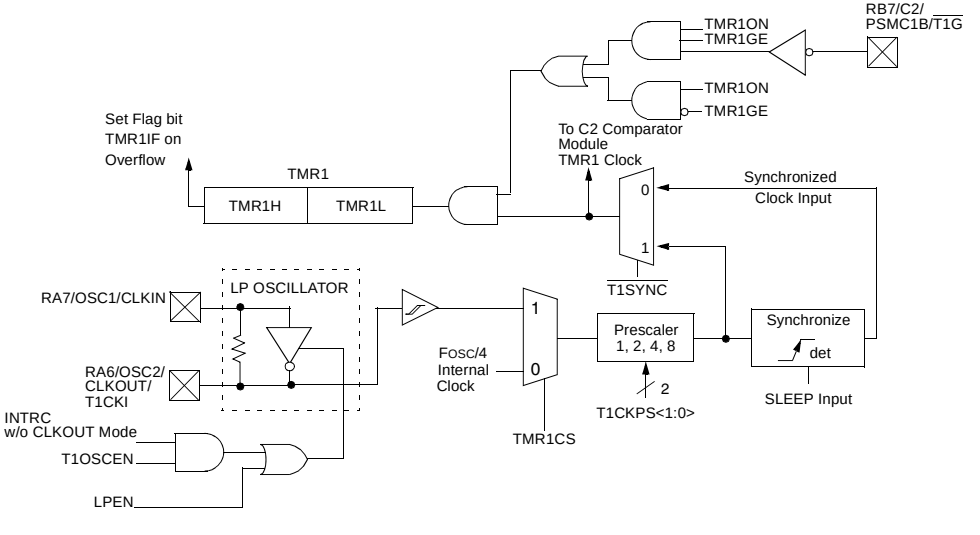
FIGURE 6-1: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

FIGURE 6-2: TIMER1 ON THE PIC16C781/782 BLOCK DIAGRAM



6.3 Timer1 Oscillator for the PIC16C781/782

When the microcontroller is using INTRC w/o CLKOUT, Timer1 can enable and use the LP oscillator as the Timer1 oscillator. When enabled, Timer1 oscillator operation is solely controlled by the T1OSCEN bit. The oscillator will operate independently of the TMR1ON bit, allowing the programmer to start and stop the Timer/Counter using the TMR1ON bit. The oscillator will also operate during SLEEP, allowing continuous timekeeping with Timer1. The electrical requirements for the LP oscillator, when used as the Timer1 oscillator, are the same as when the oscillator is used in LP mode.

Note:	The oscillator requires a startup and stabilization time before use. Therefore, T1OSCEN should be set, and a suitable delay observed, prior to enabling Timer1 (see Section 14.2).

6.4 Timer1 Interrupt

The TMR1 register pair (TMR1H and TMR1L) increments from 0000h to FFFFh and then rolls over to 0000h. When Timer1 rolls over, the TMR1IF bit (PIR1<0>) is set. To enable an interrupt, the TMR1IE bit (PIE1<0>), the GIE (INTCON<7>) and the PEIE bit (INTCON<6>) must be set prior to rollover. To clear the interrupt, the TMR1IF must be cleared by software prior to re-enabling interrupts.

Note:	When enabling the Timer1 interrupt, the user should clear both TMR1 registers and the TMR1IF prior to enabling interrupts.

6.5 Effects of RESET

Only POR and BOR Resets clear T1CON, disabling Timer1. All other RESETS do not affect Timer1.

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000X	0000 000u
0Ch	PIR1	LVDIF	ADIF	C2IF	C1IF	—	—	—	TMRIF	0000 ---0	0000 ---0
8Ch	PIE1	LVDIE	ADIE	C2IE	C1IE	—	—	—	TMRIE	0000 ---0	0000 ---0
0Eh	TMR1L	Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	-000 0000	-uuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Timer1.

NOTES:

7.0 VOLTAGE REFERENCE MODULE (VR)

The Voltage Reference module provides an on-chip nominal 3.072V reference voltage for the following:

- ADC converter
- DAC converter
- VR output on the RB0/INT/AN4/VR pin

The source for the reference voltage comes from a bandgap reference.

The control register for this module is the REFCON register shown in Register 7-1.

Note 1: If the VR module is to be used by the DAC, ADC, or VR output:, the VR module must be enabled using VREN (REFCON<3>).

2: When VREN = 1 and VROE = 1, the output driver for RB0/INT/AN4/VR will be driven tri-state and the analog driver for the VR output will be enabled. A read of RB0 will return a '0'.

Setting the VREN flag (REFCON<3>), enables the module. Following initial start-up, the module should be allowed to stabilize for best accuracy. See Section 17.0 for information concerning stabilization times and conditions.

To route the reference voltage to the external RB0/INT/AN4/VR pin, the VROE flag (REFCON<2>) must be set.

7.1 Effects of RESET

A device RESET clears the REFCON register, disabling the voltage reference.

7.2 Registers Associated with VR

A summary of the registers associated with VR is shown in Table 7-1.

REGISTER 7-1: VOLTAGE REFERENCE CONTROL REGISTER (REFCON: 9Bh)

U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	—	—	VREN	VROE	—	—
bit 7							bit 0

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **VREN:** Voltage Reference Enable bit (VR = 3.072V nominal)
1 = VR reference is enabled
0 = VR reference is disabled

bit 2 **VROE:** Voltage Reference Output Enable bit
If VREN = 1:
1 = Enabled, VR voltage reference is output on RB0
0 = Voltage reference is not available externally
If VREN = 0:
This bit is ignored

bit 1-0 **Unimplemented:** Read as '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH VR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
09Bh	REFCON	—	—	—	—	VREN	VROE	—	—	---- 00--	---- 00--

NOTES:

8.0 PROGRAMMABLE LOW VOLTAGE DETECT MODULE (PLVD)

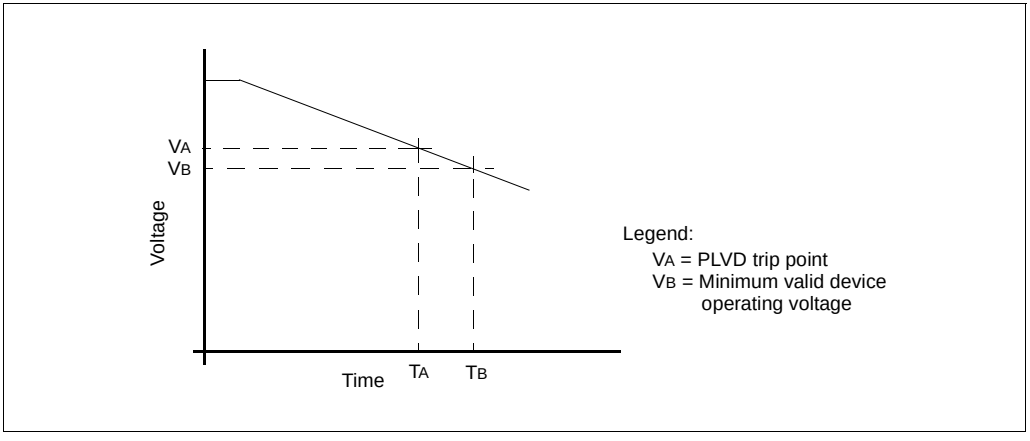
The PLVD module monitors the VDD power supply of the microcontroller and signals the microcontroller whenever VDD drops below its trip voltage. The signal acts as an 'early warning' of power-down, allowing the microcontroller to finish any critical 'housekeeping' tasks prior to completing power-down.

Figure 8-1 demonstrates a potential application of the PLVD module (typical battery operation). At time TA, the VDD supply voltage (VA) has fallen below the PLVD reference voltage. The PLVD voltage comparator then sets the LVDIF bit (PIR<7>), indicating a low voltage condition. The time between TA and TB is then available to the microcontroller for completing a 'graceful' power-down before VDD falls below VB.

Figure 8-2 is a simplified block diagram for the PLVD module, showing the VDD resistor ladder, control register, and voltage comparator.

Note:	For low power applications, current drain can be minimized by enabling the module only during regular polled testing. When not in use, the module is disabled by clearing the LVDEN bit (LVDCON<4>), which also powers down the resistor ladder between VDD and Vss.

FIGURE 8-1: TYPICAL LOW VOLTAGE DETECT APPLICATION



8.1 Control Register

The PLVD module is controlled via the LVDCON register shown in Register 8-1.

To enable the module for testing, the LVDEN bit (LVDCON<4>) must be set. This will enable the on-board voltage reference and connect the resistor ladder between VDD and Vss. Clearing LVDEN will disable the module and disconnect the resistor ladder from Vss.

The trip voltage is set by programming the LVDL<3:0> bit (LVDCON<3.0>). The voltages available are listed in Register 8-1. Note that voltages below 2.5V and above 4.75V are not available and should not be used.

The BGST bit (LVDCON<5>) is a status bit indicating that the internal reference voltage bandgap has stabilized. No test should be performed until this bit is set.

The low voltage output flag for the PLVD module is the LVDIF bit (PIR1<6>).

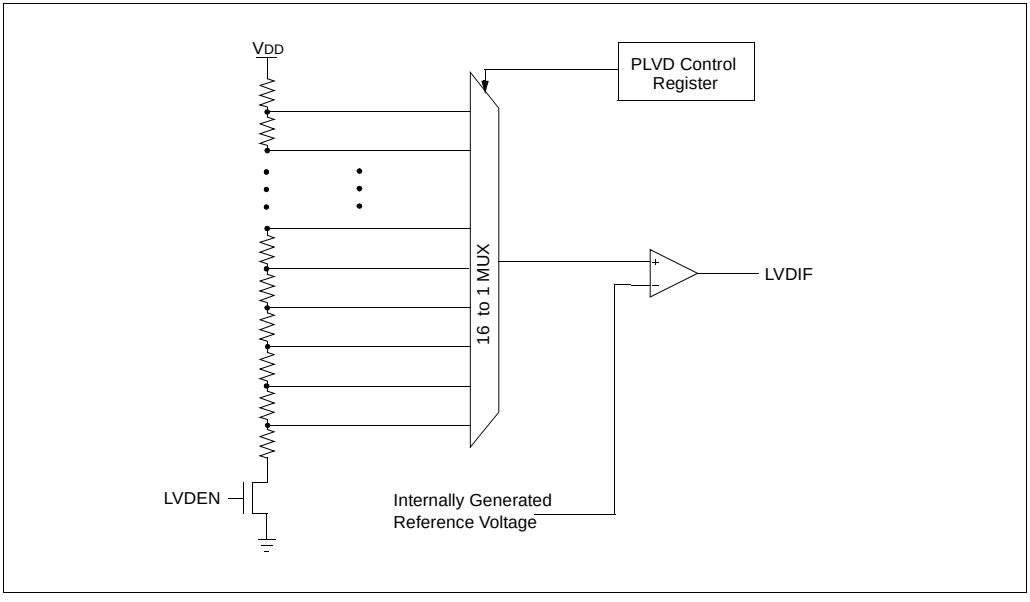
8.2 Operation

The PLVD indicates a low voltage condition by setting the LVDIF bit in the PIR1 register. Once set by the PLVD module, the LVDIF bit will remain set until cleared by software. For proper indication of a low voltage condition, the user should clear this bit prior to testing.

To test for a low voltage condition, the PLVD module compares the divided output of VDD against an internal bandgap reference. The PLVD module automatically enables this reference whenever it is enabled and provides a stability bit, BGST, to indicate when it has stabilized. The bandgap reference is also enabled by other modules within the PIC16C781/782 as part of their operation. Other modules using the bandgap include the following:

- VR module
- BOR module
- OPA calibration module

FIGURE 8-2: LOW VOLTAGE DETECT BLOCK DIAGRAM



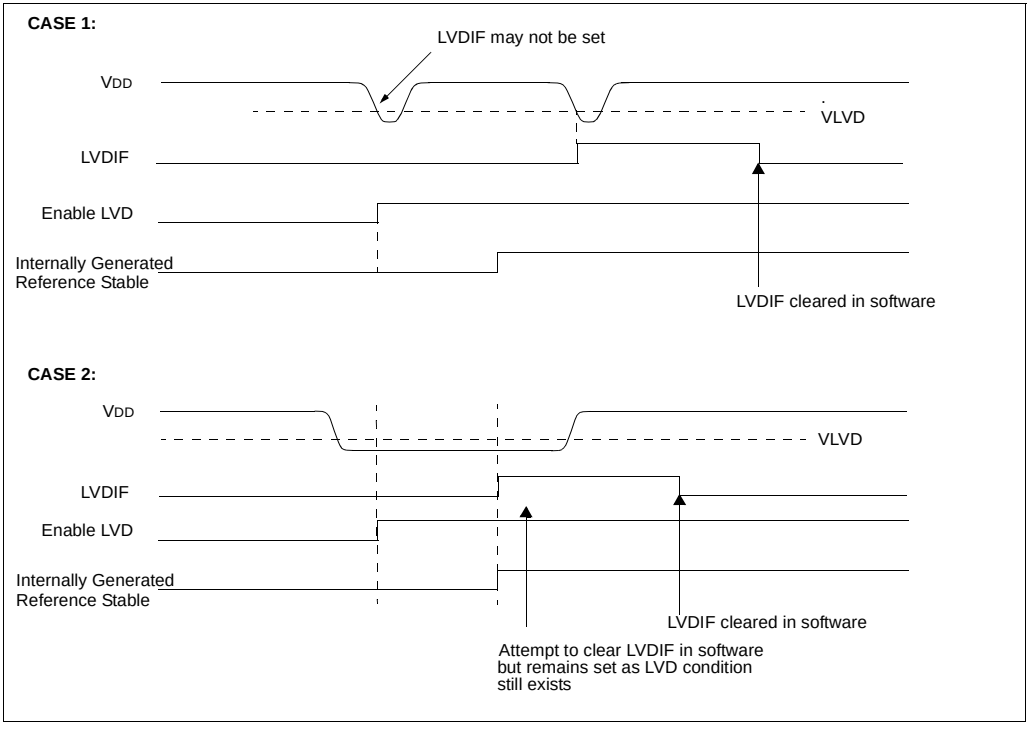
If another module has enabled the bandgap, then the reference will be stable when the PLVD module is enabled and the BGST flag can be ignored. However, if the bandgap has not been previously enabled, the LVDIF bit will not be valid until the BGST bit is set (see Figure 8-3). Systems using the PLVD interrupt should not enable the interrupt until after the reference is stable to prevent spurious interrupts.

8.2.1 SETTING UP THE PLVD MODULE

The following steps are needed to set up the PLVD Module:

1. Write the value to the LV3:LV0 bits (LVDCON register), which selects the desired PLVD Trip Point.
2. Ensure that PLVD interrupts are disabled (the LVDIE bit is cleared, or the GIE bit is cleared).
3. Enable the PLVD module (set the LVDEN bit in the LVDCON register).
4. Wait for the PLVD module to stabilize (the BGST bit to become set).
5. Clear the PLVD interrupt flag, which may have falsely become set until the PLVD module has stabilized (clear the LVDIF bit).
6. Enable the PLVD interrupt (set the LVDIE and the GIE bits).

FIGURE 8-3: LOW VOLTAGE DETECT WAVEFORMS



REGISTER 8-1: PROGRAMMABLE LOW VOLTAGE DETECT REGISTER (LVDCON: 9Ch)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
—	—	BGST	LVDEN	LV3	LV2	LV1	LV0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **BGST:** Internal Reference Voltage Stable Flag bit
1 = Reference is stable
0 = Reference is not stable

bit 4 **LVDEN:** Low Voltage Detect Power Enable bit
1 = Enables PLVD, powers up LVD circuit
0 = Disables PLVD, powers down LVD circuit.

bit 3-0 **LV<3:0>:** Low Voltage Detection Limit bits
1111 = Reserved
1110 = 4.5V typical
1101 = 4.2V typical
1100 = 4.0V typical
1011 = 3.8V typical
1010 = 3.6V typical
1001 = 3.5V typical
1000 = 3.3V typical
0111 = 3.0V typical
0110 = 2.8V typical
0101 = 2.7V typical
0100 = 2.5V typical
0011 = Below valid operating voltage
0010 = Below valid operating voltage
0001 = Below valid operating voltage
0000 = Below valid operating voltage

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

Example 8-1 shows the configuration of the PLVD module and a sample polling routine to monitor for low voltage conditions.

EXAMPLE 8-1: PLVD EXAMPLE

```
;*************************************************
;*  This code block will configure the PLVD for polling
;*  and set the trip point for 4.2 to 4.4 volts
;*  Includes polling routine
;*

    BANKSEL     LVDCON              ; Select Bank 1
    BCF         PIE1,LVDIE          ; Disable PLVD interrupt
    MOVLW       B'00011101'
    MOVWF       LVDCON              ; Enable PLVD, 4.2-4.4V trip

WRM_UP
    BTFSS       LVDCON,BGST         ;
    GOTO        WRM_UP              ;
    BANKSEL     PIR1                ; Select Bank 0
    BCF         PIR1,LVDIF          ; Clear PLVD interrupt flag

;*************************************************
;* Test for PLVD trip

    BANKSEL     PIR1                ; Select Bank 0
    BTFSC       PIR1,LVDIF          ; Test for PLVD trip
    GOTO        LO_V_DET            ; If tripped save 4 pwrfail
```

8.3 Operation During SLEEP

When enabled, the PLVD circuitry continues to operate during SLEEP. If the device voltage crosses the trip point, the LVDIF bit is set and the device awakens from SLEEP. Device execution continues from the interrupt vector address, if interrupts have been globally enabled.

8.4 Effects of a RESET

A device RESET forces all registers to their RESET state. This forces the PLVD module to be disabled.

8.5 Low Voltage Detect Registers

The registers associated with Programmable Low Voltage Detect are shown in Table 8-1.

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH LOW VOLTAGE DETECT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
09Ch	LVDCON	—	—	BGST	LVDEN	LV3	LV2	LV1	LV0	--00 0101	--00 0101
08Ch	PIE1	LVDIE	ADIE	C2IE	C2IE	—	—	—	TMR1IE	0000 ---0	0000 ---0
08Ch	PIR1	LVDIF	ADIF	C2IF	C2IF	—	—	—	TMR1IF	0000 ---0	0000 ---0

NOTES:

9.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The 8-bit ADC module, shown in Figure 9-1, has 10 inputs in the PIC16C781/782:

- 8 external channels, AN<7:0> (RA<3:0> and RB<3:0>)
- 2 internal channels, VR and VDAC

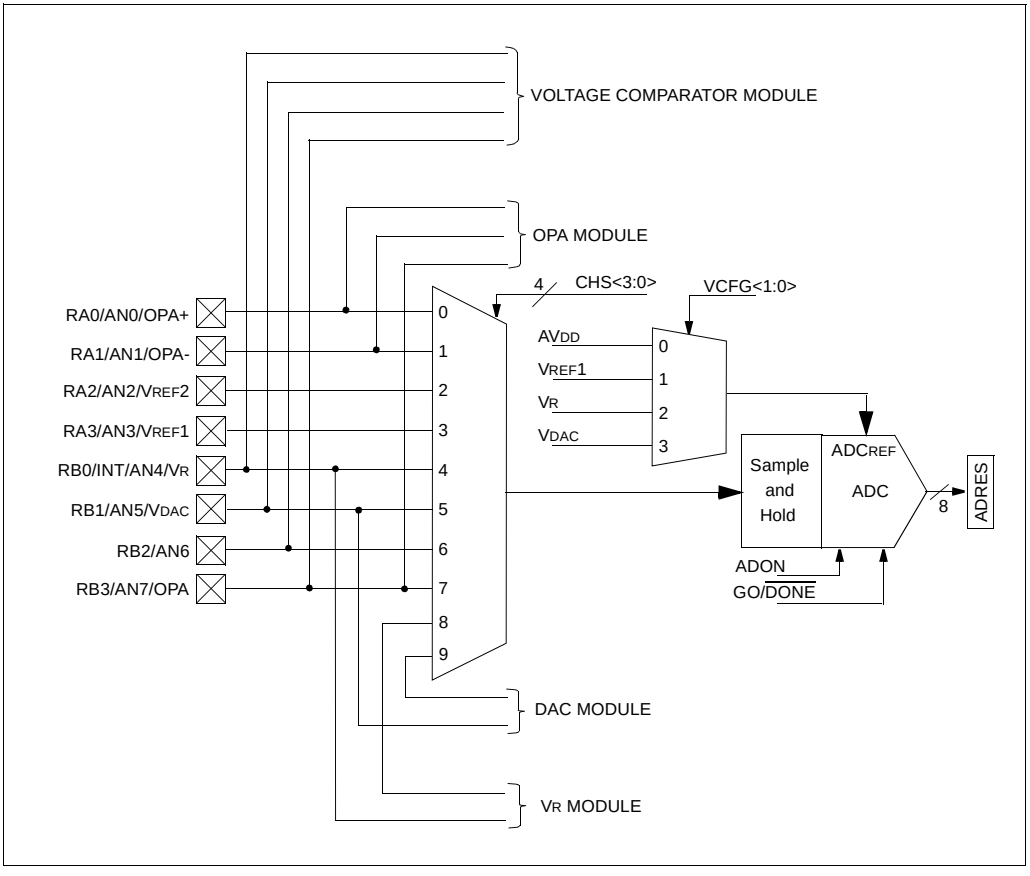
The ADC allows conversion of an analog input signal to a corresponding 8-bit digital value. The desired channel is connected to a Sample-and-Hold by the input multiplexers. The output of the Sample-and-Hold captures a snapshot of the voltage and holds it for the ADC. The ADC then generates the 8-bit result via successive approximation.

The analog reference voltage (ADCREF) is software selectable from the following options:

- The analog positive supply: AVDD
- The reference input for Comparator C1: VREF1
- The Voltage Reference module output: VR
- The DAC Converter module output: VDAC

The ADC has the unique feature of being able to operate while the device is in SLEEP mode. To operate in SLEEP, the ADC conversion clock must be derived from the ADC's dedicated internal RC oscillator.

FIGURE 9-1: ADC MODULE BLOCK DIAGRAM



9.1 Control Registers

The ADC module has three registers. These registers are:

- ADC Result Register: ADRES
- ADC Control Register 0: ADCON0
- ADC Control Register 1: ADCON1

The ADCON0 register, shown in Register 9-1, controls the operations and input channel selection for the ADC module. The ADCON1 register, shown in Register 9-3, selects the voltage reference used by the ADC module. The ADRES register, shown in Register 9-2, holds the 8-bit result of the conversion.

Additional information on using the ADC module can be found in the PIC Mid-Range MCU Family Reference Manual (DS33023) and in Application Note AN546 (DS00546).

9.1.1 ADCON0 REGISTER

The ADCON0 register, shown in Register 9-1, controls the following:

- Clock source and prescaler
- Input channel
- Conversion start/stop
- Enabling of the ADC module

Setting the ADON bit, ADCON0<0>, enables the ADC module. Clearing ADON disables the module and terminates any conversion in process.

The ADCS<1:0> bits (ADCON0<7:6>) determine the clock source used by the ADC module.

The CHS<3:0> bits (ADCON0<5:3,1>) determine the input channel to the ADC module. CHS<3> specifically determines whether the source is internal or external.

Setting the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) initiates the conversion process. The ADC clears this bit at the completion of the conversion process.

REGISTER 9-1: ADC CONTROL REGISTER 0 (ADCON0: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/S-0	R/W-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	CHS3	ADON
bit 7							bit 0

bit 7-6 **ADCS<1:0>:** ADC Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = ADRC (clock derived from a dedicated RC oscillator)

bit 5-3 **CHS<2:0>:** Analog Channel Select bits (select which channel to convert)

If CHS3 = 0:	If CHS3 = 1:
000 = channel 0 (AN0)	000 = VR
001 = channel 1 (AN1)	001 = VDAC
010 = channel 2 (AN2)	010 = Reserved. Do not use.
011 = channel 3 (AN3)	011 = Reserved. Do not use.
100 = channel 4 (AN4)	100 = Reserved. Do not use.
101 = channel 5 (AN5)	101 = Reserved. Do not use.
110 = channel 6 (AN6)	110 = Reserved. Do not use.
111 = channel 7 (AN7)	111 = Reserved. Do not use.

bit 2 **GO/$\overline{\text{DONE}}$:** ADC Conversion Status bit
1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle.
0 = ADC conversion is not in progress (this bit is cleared by hardware when conversion is complete)

bit 1 **CHS3:** Analog Channel Select bit
1 = Internal channel selected for conversion
0 = External channel selected for conversion

bit 0 **ADON:** ADC On bit
1 = ADC enabled
0 = ADC disabled

Legend:			
S = Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

9.1.2 ADCON1 REGISTER

The ADCON1 register, shown in Register 9-3, controls the reference voltage selection for the ADC module.

Bits VCFG<1:0> select the reference voltage (ADCREF).

9.1.3 ADRES REGISTER

The ADRES register, shown in Register 9-2, contains the 8-bit result of the conversion. At the completion of the ADC conversion:

- 8-bit result is loaded into ADRES.
- GO/$\overline{\text{DONE}}$ bit (ADOCN0<2>) is cleared.
- ADC interrupt flag bit ADIF (INTCON<6> and PIR1<6>) are set.
- If the ADC interrupt is enabled, an interrupt is also generated.

REGISTER 9-2: ADC RESULT REGISTER (ADRES: 1Eh)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
bit 7							bit 0

bit 7-0 **AD<7:0>:** ADC Conversion Results bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

REGISTER 9-3: ADC CONTROL REGISTER 1 (ADCON1: 9Fh)

U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	—	VCFG1	VCFG0	—	—	—	—
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as ’0’

bit 5-4 **VCFG<1:0>:** Voltage Reference Configuration bits

00 = AVDD
01 = VREF1
10 = VR
11 = VDAC

bit 3-0 **Unimplemented:** Read as ’0’

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

9.2 Configuring the ADC Module

9.2.1 CONFIGURING ANALOG PORT PINS

The ANSEL and TRISB registers control the operation of the ADC port pins. The port pins to be used as analog inputs must have their corresponding TRISB bits set (= 1). The proper ANSEL bits must also be set (analog input) to disable the digital input buffer.

Note 1: The ADC operation is independent of the state of the TRISB or ANSEL bits. These bits must be configured by the firmware prior to initiation of an ADC conversion.

2: When reading the PORTA or PORTB registers, all pins configured as analog input channels will read as a '0'.

3: Analog levels on any pin that is defined as a digital input, including AN<7:0>, may cause the input buffer to consume excess supply current.

9.2.2 CONFIGURING THE REFERENCE VOLTAGES

The VCFG<5:4> bits in the ADCON1 register configure the ADC module reference voltage input, ADCREF. The reference input can come from any of the following:

- Internal voltage reference (VR)
- External comparator C1 reference (VREF1)
- DAC output (VDAC)
- Analog positive supply (AVDD)

If an external reference is chosen for the ADCREF input, the port pin that multiplexes with the incoming external reference must also be configured as an analog input.

9.2.3 SELECTING THE ADC CONVERSION CLOCK

The ADC conversion cycle requires 9.5TAD. The source of the ADC conversion clock is software selectable. The four possible options for ADC clock are:

- FOSC/2
- FOSC/8
- FOSC/32
- ADRC (clock derived from a dedicated internal RC oscillator)

For correct ADC conversion, the ADC conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μsec. Table 9-1 shows the resultant TAD times derived from the device operating frequencies and the ADC clock source selected.

TABLE 9-1: TAD vs. DEVICE OPERATING FREQUENCIES: PIC16C781/782

ADC Clock Source (TAD)		Device Frequency			
Operation	**ADCS1:ADCS0**	**20 MHz**	**5 MHz**	**1.25 MHz**	**333.33kHz**
2 TOSC	00	100 ns(2)	400 ns(2)	1.6 s	6 μs
8 TOSC	01	400 ns	1.6 μs	6.4 μs	24 μs(3)
32 TOSC	10	1.6 μs	6.4 μs	25.6 μs(3)	96 μs(3)
RC	11	2 - 6 μs(1,4)	2 - 6 μs(1,4)	2 - 6 μs(1,4)	2 - 6 μs(1)

Legend: Shaded cells are outside of recommended range.

Note 1: The RC source has a typical TAD time of 4 μs.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When device frequency is greater than 1 MHz, the RC ADC conversion clock source is recommended for SLEEP operation only.

9.2.4 INITIATING A CONVERSION

The Analog-to-Digital conversion is initiated by setting the GO/$\overline{\text{DONE}}$ bit in ADCON0 register. When the conversion is complete, the ADC module:

- Clears the GO/$\overline{\text{DONE}}$ bit
- Sets the ADIF flag in the PIR1 register
- Generates an interrupt if the ADIE, PEIE, and GIE bits are set.

If the conversion must be aborted, the GO/$\overline{\text{DONE}}$ bit can be cleared in software. The ADRES register will not be updated with the partially completed ADC conversion sample. Instead, the ADRES will contain the value from the last completed conversion. After an aborted conversion, a 2TAD delay is required before another acquisition/conversion can be initiated. Following the delay, an input acquisition is automatically started on the selected channel.

Note:	The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the ADC.

9.3 ADC Acquisition Requirements

For the ADC module to meet its specified accuracy, the internal Sample-and-Hold capacitor (CHOLD) must be allowed to charge to within ½ LSb of the voltage present on the input channel (see analog input model in Figure 9-2). The analog source resistance (RS) and the internal sampling switch resistance (RSS) will directly affect the time required to charge CHOLD. In addition, RSS will vary over the power supply voltage range (AVDD), and RS will affect the input offset voltage at the analog input (due to pin leakage current). Therefore:

1. The maximum recommended impedance for any analog sources is 10 kOhms.
2. Following any change in the analog input channel selection, a minimum acquisition delay must be observed before another conversion can begin (see Equation 9-1).

To calculate the minimum acquisition time, Equation 9-1 may be used. This equation calculates the acquisition time to within ½ LSb error, assuming an 8-bit conversion (512 steps for the PIC16C781/782 ADC). The ½ LSb error is the maximum error allowed for the ADC to meet its specified accuracy.

EQUATION 9-1: ADC MINIMUM CHARGING TIME

$$V_{HOLD} = (ADC_{REF} - (ADC_{REF}/512)) \bullet (1 - e^{-T_{CAP}/C_{HOLD}(R_{IC}+R_{SS}+R_S)})$$

Given: $V_{HOLD} = (ADC_{REF}/512)$, for 1/2LSb resolution

The above equation reduces to:

$$T_{CAP} = -(51.2\ pF)(1\ k\Omega + R_{SS} + R_S)\ Ln(1/511)$$

Example 9-1 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following system assumptions.

CHOLD = 51.2 pF

RS = 10kΩ

1/2 LSb error

RSS = 7kΩ @ VDD = 5V

Note 1:	The reference voltage (ADCREF) has no effect on the equation, since it cancels itself out.
2:	The charge holding capacitor (CHOLD) is not discharged after each conversion.
3:	The maximum recommended impedance for analog sources is 10kΩ. This is required to meet the pin leakage specification.
4:	After a conversion has completed, a 1.0TAD delay must be completed before acquisition can begin again. During this time the holding capacitor is not connected to the selected ADC input channel.

EXAMPLE 9-1: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

T_{ACQ} = Amplifier Setting Time +
Holding Capacitor Charging Time +
Temperature Coefficient

$T_{ACQ} = 5\ \mu s + T_{CAP} + [(Temp - 25°C)(0.05\ \mu s/°C)]$

$T_{CAP} = -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ In(1/511)$

$-51.2\ pF\ (1\ k\Omega + 7k\Omega + 10k\Omega)\ In(0.0020)$

$-51.2\ pF\ (18\ k\Omega)\ In(0.0020)$

$-0.921\ \mu s\ (-6.2364)$

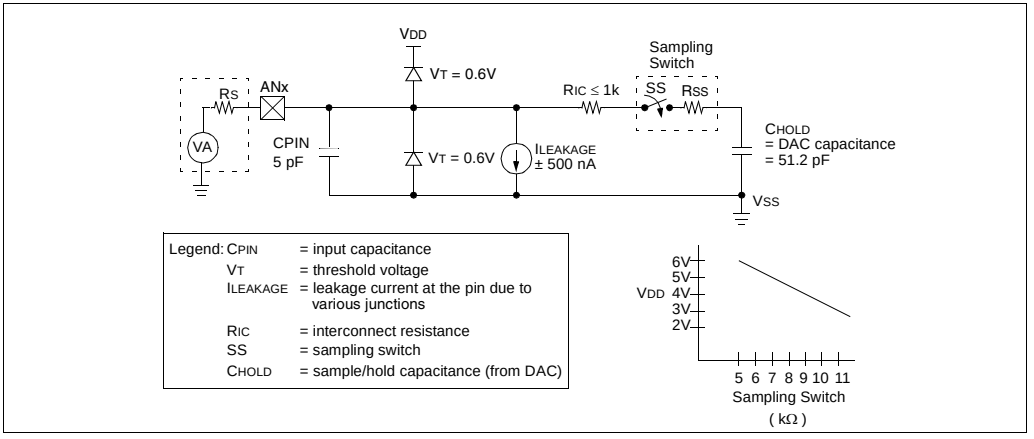
$5.747\ \mu s$

$T_{ACQ} = 5\ \mu s + 5.747\ \mu s + [(50°C - 25°C)(0.05 \mu s/°C)]$

$10.747\ \mu s + 1.25\ \mu s$

$11.997\ \mu s$

FIGURE 9-2: ANALOG INPUT MODEL



9.4 ADC Configuration and Conversion

Example 9-2 demonstrates an ADC conversion. The RA0/AN0 pin is configured as the analog input. The reference voltage selected is the device AVDD. The ADC interrupt is enabled, and the ADC conversion clock is ADRC.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion aborts the current conversion. The ADRES register is NOT updated with the partially completed ADC conversion sample. That is, the ADRES register continues to contain the value of the last completed conversion (or the last value written to the ADRES register). After the ADC conversion is aborted, a 2TAD wait period is required before the next acquisition is started. After this 2TAD wait period, an acquisition is automatically started on the selected channel.

EXAMPLE 9-2: ADC CONVERSION

```
;*****************************************
;*  This code block will configure the ADC
;*  for polling, AVDD as reference, RC clock
;*  and RA0 input.
;*
;*  Conversion start & wait for complete
;*  polling code included.
;*
    BANKSEL    ADCON1      ; Select Bank 1
    CLRF       ADCON1      ; AVDD as VREF
    BSF        TRISA,0     ; Set RA0 as input
    BSF        ANSEL,0     ; Set RA0 as analog

    BANKSEL    ADCON0      ; Select Bank0
    MOVLW      B'11000001'
    MOVWF      ADCON0      ; RC, Ch 0, ADC on

;*****************************************
;*  Start & Wait for ADC complete, assumes
;*  minimum acquisition delay from
;*  configuration.

ADC_CNVRT
    BANKSEL    ADCON0      ; Select Bank 0
    BSF        ADCON0,GO   ; Start convert
ADC_CN_LOOP
    BTFSC      ADCON0,GO   ; Test for end
    GOTO       ADC_CN_LOOP ; If not, wait
    MOVF       ADRES,W     ; Get result
```


9.4.1 FASTER CONVERSION/LOWER RESOLUTION TRADE-OFF

Not all applications require a result having 8-bits of resolution. Some may instead, require a faster conversion time. The ADC module allows users to make a trade-off of conversion speed for resolution. Regardless of the resolution required, the acquisition time is the same. To speed up the conversion, the clock source of the ADC module may be switched during the conversion, so that the TAD time violates the minimum specified time (see the applicable Electrical Specification). Once the switch is made, all the following ADC result bits are invalid (see ADC Conversion Timing in the Electrical Specifications section). The clock source may only be switched between the three oscillator options (it cannot be switched from/to RC). The equation to determine the time before the oscillator must be switched for a desired resolution is as follows:

Conversion time = $2T_{AD} + N \bullet T_{AD} + (8 - N)(2T_{OSC})$

Where: N = number of bits of resolution required.

Since the TAD is based on the device oscillator, the user must employ some method (such as a timer, software loop, etc.) to determine when the ADC oscillator must be changed.

9.5 ADC Operation During SLEEP

The ADC module can operate during SLEEP mode. This requires that the ADC clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the ADC module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise from the conversion. When the conversion is completed the GO/DONE bit is cleared, and the result is loaded into the ADRES register. If the ADC interrupt is enabled, the device awakens from SLEEP. If the ADC interrupt is not enabled, the ADC module is turned off, although the ADON bit remains set.

When the ADC clock source is another clock option (not RC), a SLEEP instruction causes the present conversion to be aborted and the ADC module to be turned off. The ADON bit remains set.

Turning off the ADC places the ADC module in its lowest current consumption state.

Note:	For the ADC module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To perform an ADC conversion in SLEEP, ensure the SLEEP instruction immediately follows the instruction that sets the GO/DONE bit.

9.6 ADC Accuracy/Error

The absolute accuracy (absolute error) specified for the ADC converter includes the sum of all contributions for:

- Offset error
- Gain error
- Quantization error
- Integral non-linearity error
- Differential non-linearity error
- Monotonicity

The **absolute error** is defined as the maximum deviation from an actual transition versus an ideal transition for any code. The absolute error of the ADC converter is specified as < ±1 LSb for $ADC_{REF} = V_{DD}$ (over the device's specified operating range). However, the accuracy of the ADC converter degrades as V_{DD} diverges from V_{REF}.

For a given range of analog inputs, the output digital code will be the same. This is due to the quantization of the analog input to a digital code. **Quantization error** is typically ± 1/2 LSb and is inherent in the analog to digital conversion process. The only way to reduce quantization error is to use an ADC with greater resolution of the ADC converter.

Offset error measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function. Offset error can be calibrated out of a system, or introduced into a system, through the interaction of the total leakage current and source impedance at the analog input.

Gain error measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in slope of the transfer function. The difference in gain error to full scale error is that full scale does not take offset error into account. Gain error can be calibrated out in software.

Linearity error refers to the uniformity of the code changes. Linearity errors cannot be calibrated out of the system. **Integral non-linearity error** measures the actual code transition versus the ideal code transition, adjusted by the gain error for each code. **Differential non-linearity** measures the maximum actual code width versus the ideal code width. This measure is unadjusted.

If the linearity errors are very large, the ADC may become **non-monotonic**. This occurs when the digital values for one or more input voltages are less than the value for a lower input voltage.

9.6.1 CLOCK NOISE

In systems where the device frequency is low, use of the ADC RC clock is preferred. At moderate to high frequencies, TAD should be derived from the device oscillator. TAD must not violate the minimum and should be ≤ 8 μs for preferred operation. This is because TAD, when derived from TOSC, is kept away from on-chip phase clock transitions. This reduces, to a large extent, the effects of digital switching noise. This is not possible with the RC derived clock. The loss of accuracy due to digital switching noise can be significant if many I/O pins are active.

In systems where the device enters SLEEP mode after the start of the ADC conversion, the RC clock source selection is required. In this mode, the digital noise from the modules in SLEEP is stopped. This method gives high accuracy.

9.7 Effects of a RESET

A device RESET forces all registers to their RESET state. This forces the ADC module to be turned off, and any conversion is aborted.

The value that is in the ADRES register is not modified for a Power-on Reset. The ADRES register contains unknown data after a Power-on Reset.

9.8 Connection Considerations

If the input voltage exceeds the rail values (VSS or VDD) by greater than 0.2V, then the accuracy of the conversion is out of specification.

Note:	Care must be taken when using the RB2/AN6 pin in ADC conversions due to its proximity to the OSC1 pin.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the total source impedance is kept under the 10 kΩ recommended specification. Any external components connected (via hi-impedance) to an analog input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

9.9 Transfer Function

The ideal transfer function of the ADC converter is as follows: the first transition occurs when the analog input voltage (VAIN) is Analog ADCREF/256 (Figure 9-3).

9.10 References

A good reference for ADC converters is the "*Analog-Digital Conversion Handbook*" third edition, published by Prentice Hall (ISBN 0-13-03-2848-0).

FIGURE 9-3: ADC TRANSFER FUNCTION

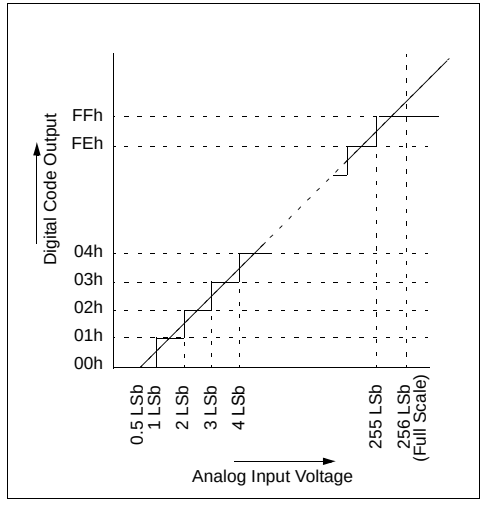


FIGURE 9-4: FLOW CHART OF ADC OPERATION

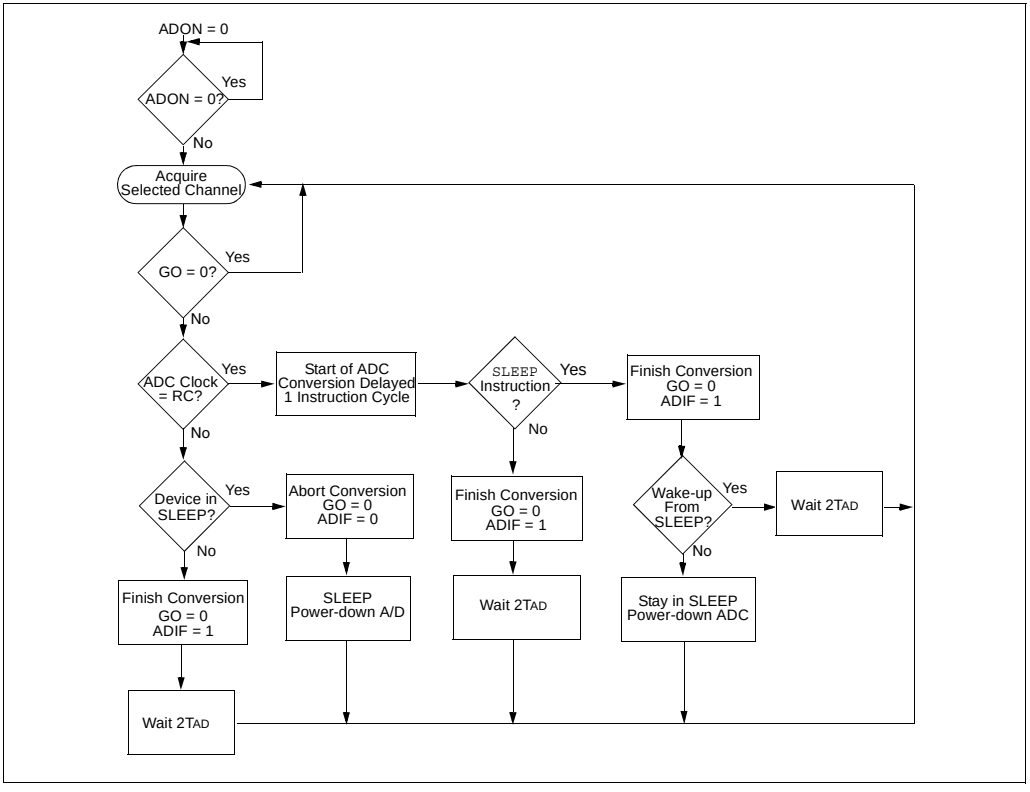


TABLE 9-2: REGISTERS/BITS ASSOCIATED WITH ADC, PIC16C781/782

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	LVDIE	ADIE	C2IE	C1IE	—	—	—	TMR1IE	0000 ---0	0000 ---0
0Ch	PIR1	LVDIF	ADIF	C2IF	C1IF	—	—	—	TMR1IF	0000 ---0	0000 ---0
1Eh	ADRES	ADC Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	CHS3	ADON	0000 0000	0000 0000
9Fh	ADCON1	—	—	VCFG1	VCFG0	—	—	—	—	--00 ----	--00 ----
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000	uuuu 0000
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx 0000	uuuu 0000
9Dh	ANSEL	Analog Channel Select								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for ADC conversion.

NOTES:

10.0 DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter (DAC) module generates an output voltage proportional to the value in the 8-bit DAC register (see Figure 10-1).

The output of the DAC module can be configured to drive:

- The reference input to the ADC module
- The reference input to Comparators C1 and C2
- An analog output on pin RB1/AN5/V_{DAC}

The voltage reference input to the DAC can be selected from:

- Analog supply AV_{DD}
- Comparator C1 $V_{REF}1$
- Voltage reference V_R

10.1 Control Registers

The DAC module is controlled via two special function registers: DACON0 and DAC. The DACON0 register, shown in Register 10-1:

- Enables DAC
- Enables output on RB1/AN5/V_{DAC}
- Selects reference voltage

The DAC register, shown in Register 10-2, sets the output of the DAC.

REGISTER 10-1: DIGITAL-TO-ANALOG CONVERTER CONTROL REGISTER0 (DACON0: 11Fh)

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
DAON	DAOE	—	—	—	—	DARS1	DARS0
bit 7							bit 0

bit 7 **DAON:** Digital-to-Analog Converter Enable bit
1 = DAC enabled
0 = DAC disabled

bit 6 **DAOE:** Digital-to-Analog Converter Output Enable bit
1 = Output on the V_{DAC} pin
0 = Output is not available for external use

bit 5-2 **Unimplemented:** Read as '0'

bit 1-0 **DARS<1:0>:** Digital-to-Analog Converter Voltage Reference Select bits, DAC_{REF}
00 = Analog supply, AV_{DD}
01 = Comparator reference, $V_{REF}1$ pin
10 = Voltage reference, V_R
11 = Reserved, do not use

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 10-2: DIGITAL-TO-ANALOG CONVERTER REGISTER (DAC: 11Eh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
bit 7							bit 0

bit 7-0 **DA<7:0>:** Digital-to-Analog Converter Digital Input bits

Legend:		
R = Readable bit	W = Writable bit	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

10.2 Control Register

The DAC module is enabled by setting the DAON bit (DACON0<7>).

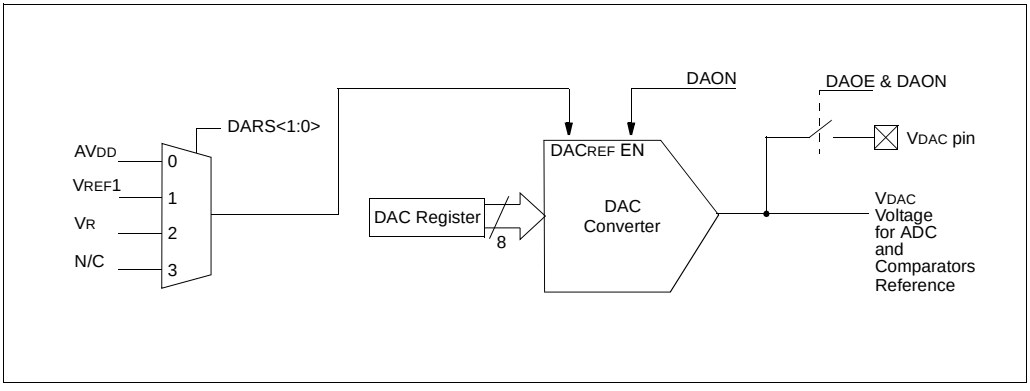
Bits DARS<1:0> (DACON0<1:0>) determine the voltage reference for the DAC module.

To output the DAC voltage, the DAOE bit (DACON0<6>) and DAON must be set. To use the DAC output internally, the appropriate reference select bits in the destination module must be set.

Note 1: To enable the DAC output as a reference for the ADC module, VCFG<1:0> in ADCON1 must be set.

2: To enable the DAC output as a reference for the Comparator module, C1R/C2R bits (CM1CON0<2>/CM2CON0<2>) must be set.

FIGURE 10-1: DAC CONVERTER BLOCK DIAGRAM



10.3 DAC Configuration

Example 10-1 shows a sample configuration for the DAC module. The port pin is configured, AVDD is selected for the voltage reference, and the DAC output is enabled.

EXAMPLE 10-1: DAC CONFIGURATION

```
;*  This code block will configure the DAC
;*  for AVDD Voltage Ref, and RB1/AN5/VDAC as
;*  output.

    BANKSEL TRISB          ; Select bank 1
    BSF     TRISB,1        ; Set RB1 input
    BSF     ANSEL,1        ; Set RB1 as analog

    BANKSEL DACON0         ; Select Bank 2
    CLRF    DAC            ; DAC to 00
    MOVLW   B'11000000'    ; Enable DAC output
    MOVWF   DACON0         ; Set REF = VDD

    MOVLW   DAC_VALUE
    MOVWF   DAC            ; Set DAC output
```

10.4 Effects of RESET

A device RESET forces all registers to their RESET state. This forces the following conditions:

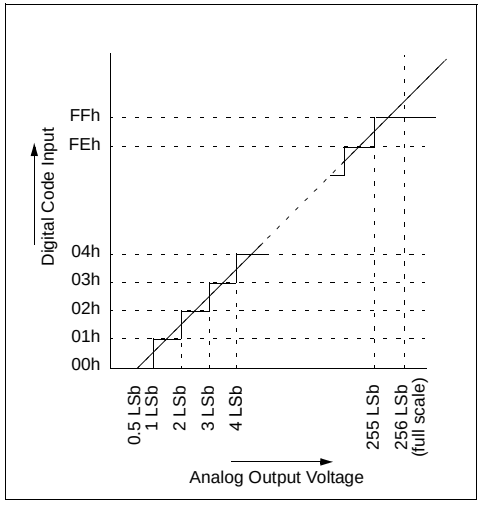
- DAC module is off
- Reference input to AVDD
- Output disabled
- DAC register is cleared

10.5 DAC Module Accuracy/Error

The accuracy/error specified for the DAC includes:

- Integral non-linearity error
- Differential non-linearity error
- Gain error
- Offset error
- Monotonicity

FIGURE 10-2: DAC TRANSFER FUNCTION



Offset error measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function. Offset error can be calibrated out of a system or introduced into a system through the interaction of the output drive capability with the load impedance.

Gain error measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in slope of the transfer function. The difference in gain error to full scale error is that full scale does not take offset error into account. Gain error can be calibrated out by adjusting the reference voltage.

Linearity error refers to the uniformity of the voltage change with code change. Linearity errors cannot be calibrated out of the system. **Integral non-linearity error** measures the actual voltage output versus the ideal voltage output adjusted by the gain error for each code.

Differential non-linearity error measures the maximum actual voltage step versus the ideal voltage step. This measure is unadjusted.

TABLE 10-1: REGISTERS/BITS ASSOCIATED WITH DAC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on All Other RESETS
11Fh	DACON0	DAON	DAOE	—	—	—	—	DARS1	DARS0	00-- --00	00-- --00
11Eh	DAC	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	0000 0000	0000 0000
86h	TRISB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	1111 1111	1111 1111
9Dh	ANSEL	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for DAC conversion.

NOTES:

11.0 OPERATIONAL AMPLIFIER (OPA) MODULE

The Operational Amplifier (OPA) Module can be configured as either an OPAMP or Voltage Comparator. The OPA module has the following features:

- External connections to all ports
- Gain Bandwidth Product selectable:
  - 70 kHz nom.
  - 2 MHz nom.
- Low leakage inputs
- Input Offset Voltage Automatic Calibration Module (ACM)
- Input Offset Voltage calibration at a programmable common mode voltage using the DAC
- Interrupt-on-change in Comparator mode using IOCB

11.1 Control Registers

The OPACON register, shown in Register 11-1, controls the OPA module. The CALCON register, shown in Register 11-2, controls the Automatic Calibration Module.

11.1.1 OPACON REGISTER

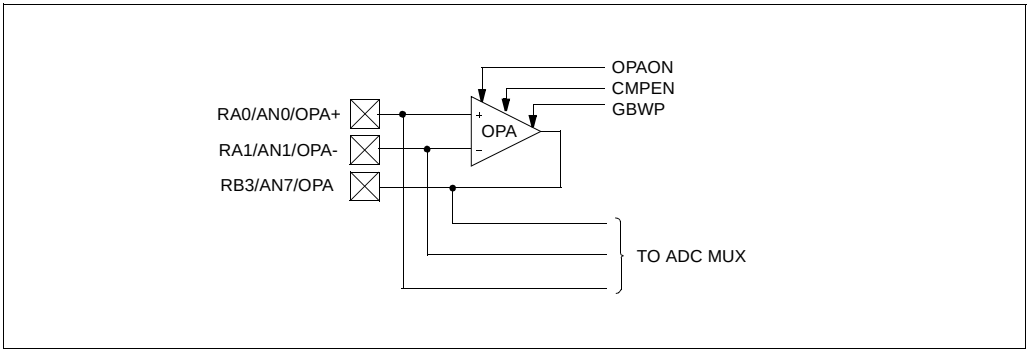
The OPA module is enabled by setting the OPAON bit (OPACON<7>). When enabled, the OPA forces the output driver of RB3/AN7/OPA into tri-state to prevent contention between the driver and the OPA output.

Clearing the CMPEN bit (OPACON,6>) configures the module as an OPAMP. Setting CMPEN configures the module as a voltage comparator.

The GBWP bit (OPACON<0>) controls the speed of the module in both comparator and OPAMP configurations. Setting GBWP results in a Gain Bandwidth Product (GBWP) of 2 MHz typical. Clearing GBWP0 results in a GBWP of the OPA of 70 kHz typical.

Note 1:	When the OPA module is enabled, the RB3/AN7/OPA pin is driven by the OPAMP output, not by the PORTB driver. Refer to the Electrical specifications for the OPAMP output drive capability.
2:	In Comparator mode (CMPEN = 1), an interrupt can be generated using the IOCB feature of RB3. RB3 must be programmed as a digital input with IOCB enabled.

FIGURE 11-1: OPA MODULE BLOCK DIAGRAM



REGISTER 11-1: OPAMP CONTROL REGISTER (OPACON: 11Ch)

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0
OPAON	CMPEN	—	—	—	—	—	GBWP
bit 7							bit 0

bit 7 **OPAON:** OPAMP Enable bit
1 = OPAMP is enabled
0 = OPAMP is disabled

bit 6 **CMPEN:** Comparator Mode Enable bit
1 = Comparator mode
0 = OPAMP mode

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **GBWP:** Gain Bandwidth Product Select bits
1 = 2 MHz typ. (fast mode)
0 = 70 kHz typ. (slow mode)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

11.1.2 CALCON REGISTER

The Automatic Calibration Module (ACM) is an internal state machine which performs an input offset voltage calibration (trim) on the OPA module (see Figure 11-2). Calibration is initiated by setting the CAL bit (CALCON<7>). Upon completion of the calibration sequence, the ACM will clear the CAL bit.

If a problem arises in the calibration process, the CALERR flag (CALCON<6>) will be set to indicate the failure to calibrate.

Setting CALREF (CALCON<5>) forces calibration at a common mode voltage specified by the output of the DAC module. The DAC module must be enabled prior to calibration. Clearing CALREF will perform the calibration with a common mode voltage of 1.2V. The output pin floats during calibration.

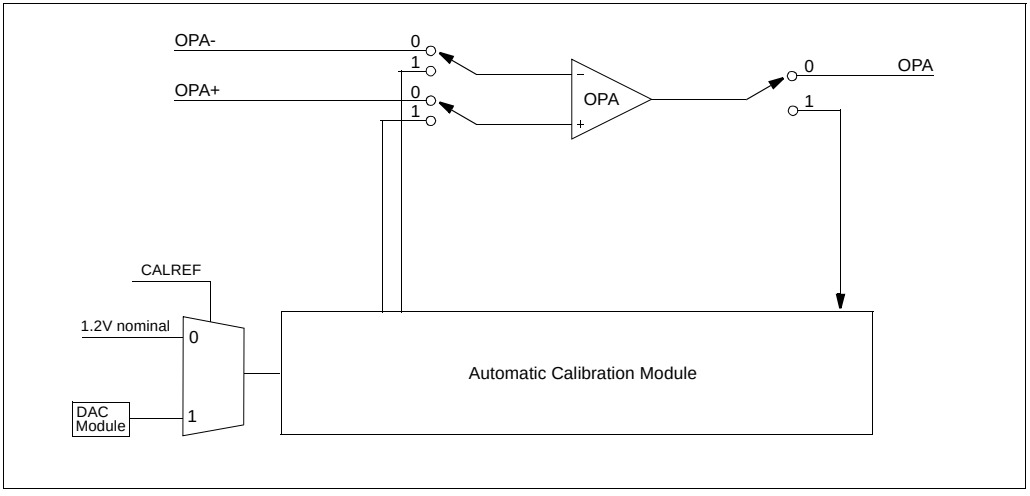
Note 1: Auto Calibration must be performed while the module is configured as an OPAMP (CMPEN = 0). Performing Auto Calibration function in the Comparator mode may yield unpredictable results.

2: If the internal 1.2V reference is used for the common mode voltage during Auto Calibration, CALREF = 0 (CALCON<5>), a delay for reference stabilization must be observed before start of calibration.

3: The OPA module shares pins with the ADC module. Performing ADC conversions on the OPA+ or OPA- pins may affect OPAMP stability.

4: When using the DAC as a reference for calibration, CALREF = 1 (CALCON<5>), the V_{DAC} voltage must be within the specified common mode voltage for the OPAMP.

FIGURE 11-2: AUTO CALIBRATION MODULE BLOCK DIAGRAM



REGISTER 11-2: CALIBRATION CONTROL REGISTER (CALCON: 110h)

R/S-0	R-0	R/W-0	U-0	U-0	U-0	U-0	U-0
CAL	CALERR	CALREF	—	—	—	—	—
bit 7							bit 0

bit 7 **CAL:** Start and Status bit
1 = Initiates a calibration
0 = Reserved (CAL is cleared by hardware)

bit 6 **CALERR:** Calibration Error Indicator bit
1 = Error occurred, OPAMP failed
0 = No error

bit 5 **CALREF:** Calibration Voltage Select bit
1 = V_{DAC} set to desired common voltage reference
0 = 1.2V nominal source (internal voltage source)

Note: V_{DAC} must not exceed OPAMP maximum common mode voltage.

bit 4-0 **Reserved:** Do not use

Legend:			
S = Cleared by hardware			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

11.2 Configuration as OPAMP or Comparator

The following example demonstrates calibration of the OPA module as an Operational Amplifier.

EXAMPLE 11-1: CALIBRATION FOR OPAMP MODE

```
;*  This code block will configure the OPA
;*  module as an Op Amp, 2 MHz GBWP, and
;*  calibrated for a common mode voltage of
;*  1.2V. Routine returns w=0 if
;*  calibration good.

    BANKSEL     OPACON       ; Select Bank 2
    MOVLW       B'10000001'  ; Op Amp mode &
    MOVWF       OPACON       ; 2 MHz GBWP

    BCF         CALCON,CALREF; Set 1.2V
    BSF         CALCON,CAL   ; Start

CAL_LOOP
    BTFSC       CALCON,CAL   ; Test for end
    GOTO        CAL_LOOP     ; If not, wait
    MOVLW       ERROR_FLAG
    BTFSS       CALCON,CALERR; Test for error
    CLRW                     ; If no, return 0
    RETURN
```

The following example demonstrates how to configure and calibrate the OPA module as a Voltage Comparator.

EXAMPLE 11-2: CALIBRATION FOR COMPARATOR MODE

```
;*  This code block will configure the OPA
;*  module as a voltage comparator, slow
;*  speed, and calibrated for a common mode
;*  voltage of 2.5 V (assumes VDD=5V).
;*  Routine returns w=0 if calibration good.

    BANKSEL     OPACON       ; Select Bank 2
    MOVLW       B'10000000'
    MOVWF       OPACON       ; Op Amp mode,
                             ; slow
    BSF         CALCON,CALREF; Common mode=DAC

    MOVLW       H'0x80'
    MOVWF       DAC          ; DAC at VDD/2
    MOVLW       B'10000000'
    MOVWF       DACON0       ; enable DAC,
                             ; VDD ref
    BSF         CALCON,CAL   ; Start
CAL_LOOP
    BTFSC       CALCON,CAL   ; Test for end
    GOTO        CAL_LOOP     ; If not, wait

    MOVLW       ERROR_FLAG
    BTFSS       CALCON,CALERR; Test for error
    CLRW                     ; If no, return 0
    BSF         OPACON,CMPEN ; Comparator mode
    RETURN
```

11.3 Effects of RESET

A device RESET forces all registers to their RESET state. This disables the OPA module and clears any calibration.

11.4 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product

Common mode voltage range is the specified voltage range for the OPA+ and OPA- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between 0 and V_{DD}-1.4V. Behavior for Common mode voltages greater than V_{DD}-1.4V, or below 0V, are not guaranteed.

Leakage current is a measure of the small source or sink currents on the OPA+ and OPA- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPA+ and OPA- inputs should be kept as small as possible and equal.

Input offset voltage is a measure of the voltage difference between the OPA+ and OPA- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the Common mode voltage. The OPA has an automatic calibration module which can minimize the input offset voltage of the module.

Open loop gain is the ratio of the output voltage to the differential input voltage, (OPA+) - (OPA-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open loop gain falls off to 0 dB. The lower GBWP is optimized for systems requiring low frequency response and low power consumption.

TABLE 11-1: REGISTERS ASSOCIATED WITH THE OPA MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
11Ch	OPACON	OPAON	CMPEN	—	—	—	—	—	GBWP	00-- ---0	00-- ---0
110h	CALCON	CAL	CALERR	CALREF	—	—	—	—	—	000- ----	000- ----
9Dh	ANSEL	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	1111 1111	1111 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
85h	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
11Eh	DAC	DA7	DA6	DA5	DA4	DA3	DA1	DA1	DA0	0000 0000	0000 0000
11Fh	DACON0	DAON	DAOE	—	—	—	—	DARS1	DARS0	00-- --00	00-- --00

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for the OPA module.

NOTES:

12.0 COMPARATOR MODULE

The comparator module has two separate voltage comparators: Comparator C1 and Comparator C2 (see Figure 12-1).

Each comparator offers the following list of features:

- Control and configuration register
- Comparator output available externally
- Programmable output polarity
- Interrupt-on-change flags
- Wake-up from SLEEP
- Configurable as feedback input to the PSMC
- Programmable four input multiplexer
- Programmable reference selections
- Programmable speed
- Output synchronization to Timer1 clock input (Comparator C2 only)

12.1 Control Registers

Both comparators have separate control and configuration registers: CM1CON0 for C1 and CM2CON0 for C2. In addition, Comparator C2 has a second control register, CM2CON1, for synchronization control and simultaneous reading of both comparator outputs.

12.1.1 COMPARATOR C1 CONTROL REGISTER

The CM1CON0 register (shown in Register 12-1) contains the control and status bits for the following:

- Comparator enable
- Comparator input selection
- Comparator reference selection
- Output mode
- Comparator speed

Setting C1ON (CM1CON0<7>) enables Comparator C1 for operation.

Bits C1CH<1:0> (CM1CON0<1:0>) select the comparator input from the four analog pins AN<7:4>.

Note:	To use AN<7:4> as analog inputs, the appropriate bits must be programmed in the ANSEL register.

Setting C1R (CM1CON0<2>) selects the output of the DAC module as the reference voltage for the comparator. Clearing C1R selects the VREF1 input on the RA3/AN3/VREF1 pin.

The output of the comparator is available internally via the C1OUT flag (CM1CON0<6>). To make the output available for an external connection, the C1OE flag (CM1CON0<5>) must be set. If the module is disabled with C1OE set, the output will be driven as shown in Table 12-2:

The polarity of the comparator output can be inverted by setting the C1POL flag (CM1CON0<4>). Clearing C1POL results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 12-2.

TABLE 12-1: OUTPUT STATE VERSUS INPUT CONDITIONS

Input Condition	C1POL	C1OUT
C1VN > C1VP	0	0
C1VN < C1VP	0	1
C1VN > C1VP	1	1
C1VN < C1VP	1	0

Note 1:	The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.
2:	The C1 interrupt will operate correctly with C1OE set or cleared.
3:	For the output of C1 on RB6/C1/PSMC1A, the PSMC must be disabled and TRISB<6> must be '0'.

C1SP (CM1CON0<3>) configures the speed of the comparator. When C1SP is set, the comparator operates at its normal speed. Clearing C1SP operates the comparator in a slower, low power mode.

FIGURE 12-1: COMPARATOR C1 SIMPLIFIED BLOCK DIAGRAM

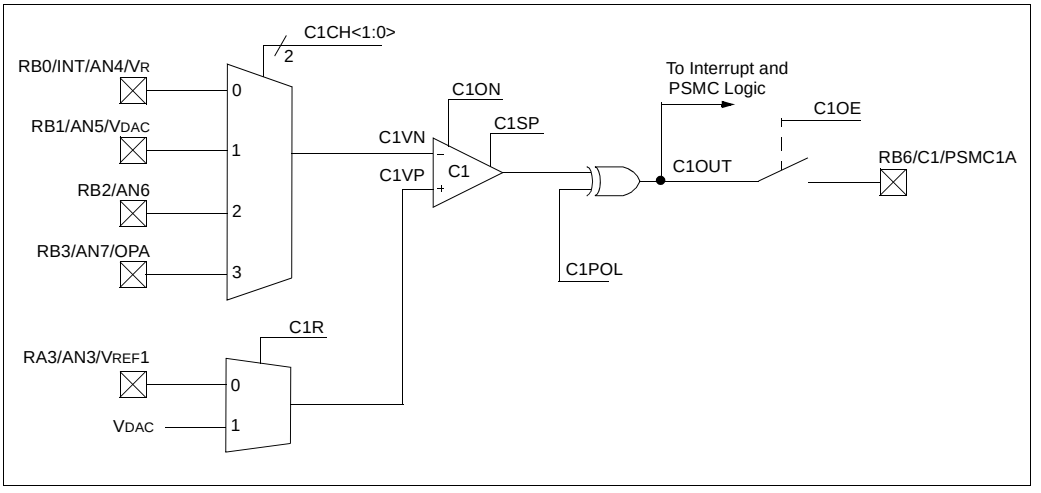
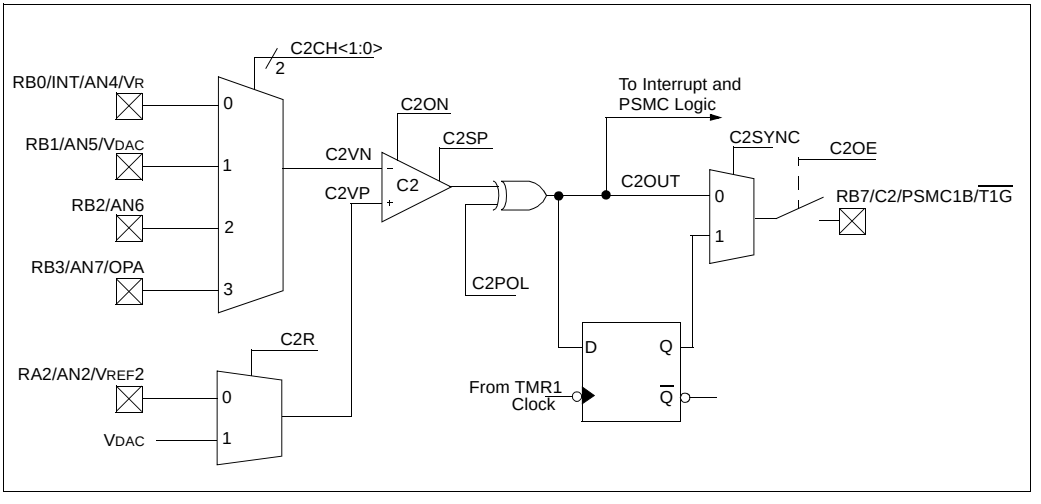


FIGURE 12-2: COMPARATOR C2 SIMPLIFIED BLOCK DIAGRAM



REGISTER 12-1: COMPARATOR C1 CONTROL REGISTER0 (CM1CON0: 119h)

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0
bit 7							bit 0

bit 7 **C1ON:** Comparator C1 Enable bit
1 = C1 Comparator is enabled
0 = C1 Comparator is disabled

bit 6 **C1OUT:** Comparator C1 Output bit
If C1POL = 1 (inverted polarity):
C1OUT = 1, C1VP < C1VN
C1OUT = 0, C1VP > C1VN
If C1POL = 0 (non-inverted polarity):
C1OUT = 1, C1VP > C1VN
C1OUT = 0, C1VP < C1VN

bit 5 **C1OE:** Comparator C1 Output Enable bit
1 = C1OUT is present on the RB6/C1/PSMC1A pin(1)
0 = C1OUT is internal only

bit 4 **C1POL:** Comparator C1 Output Polarity Select bit
1 = C1OUT logic is inverted
0 = C1OUT logic is not inverted

bit 3 **C1SP:** Comparator C1 Speed Select bit
1 = C1 operates in normal speed mode
0 = C1 operates in low power, slow speed mode

bit 2 **C1R:** Comparator C1 Reference Select bits (non-inverting input)
1 = C1VP connects to V_{DAC} output
0 = C1VP connects to $V_{REF}1$

bit 1-0 **C1CH<1:0>:** Comparator C1 Channel Select bits
00 = C1VN of C1 connects to AN4
01 = C1VN of C1 connects to AN5
10 = C1VN of C1 connects to AN6
11 = C1VN of C1 connects to AN7

Note 1: C1OUT will only drive RB6/C1/PSMC1A if:
(C2OE = 1) & (C2ON = 1) & (TRISB<7> = 0) & ((SMCON = 0)
or ((SMCOM = 0) & (SCEN = 0))).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

12.1.2 COMPARATOR C2 CONTROL REGISTERS

The CM2CON0 register is a functional copy of the CM1CON0 register described in Section 12.1.1. A second control register, CM2CON1, is also present for control of an additional synchronizing feature, as well as mirrors of both comparator outputs.

12.1.2.1 Control Register CM2CON0

The CM2CON0 register, shown in Register 12-2, contains the control and status bits for Comparator C2.

Setting C2ON (CM2CON0<7>) enables Comparator C2 for operation.

Bits C2CH<1:0> (CM2CON0<1:0>) select the comparator input from the four analog pins, AN<7:4>.

Note 1: To use AN<7:4> as analog inputs, the appropriate bits must be programmed in the ANSEL register.

C2R (CM2CON0<2>) selects the reference to be used with the comparator. Setting C2R (CM2CON0<2>) selects the output of the DAC module as the reference for the comparator. Clearing C2R selects the VREF2 input on the RA2/AN2/VREF2 pin.

The output of the comparator is available internally via the C2OUT bit (CM2CON0<6>). To make the output available for an external connection, the C2OE bit (CM2CON0<5>) must be set.

Note 1: The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.

2: The C2 interrupt will operate correctly with C2OE set or cleared. An external output is not required for the C2 interrupt.

3: For C2 output on RB7/C2/PSMC1B/$\overline{T1G}$: (C2OE=1) & (C2ON=1) & (TRISB<7>=0) & ((SMCON=0) or ((SMCOM=0) & (SCEN=0))).

The comparator output, C2OUT, can be inverted by setting the C2POL bit (CM2CON0<4>). Clearing C2POL results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 12-3.

C2SP (CM2CON0<3>) configures the speed of the comparator. When C2SP is set, the comparator operates at its normal speed. Clearing C2SP operates the comparator in low power mode.

REGISTER 12-2: COMPARATOR C2 CONTROL REGISTER0 (CM2CON0: 11Ah)

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0
bit 7							bit 0

bit 7 **C2ON:** Comparator C2 Enable bit
1 = C2 Comparator is enabled
0 = C2 Comparator is disabled

bit 6 **C2OUT:** Comparator C2 Output bit
If C2POL = 1 (inverted polarity):
C2OUT = 1, C2VP < C2VN
C2OUT = 0, C2VP > C2VN
If C2POL = 0 (non-inverted polarity):
C2OUT = 1, C2VP > C2VN
C2OUT = 0, C2VP < C2VN

bit 5 **C2OE:** Comparator C2 Output Enable bit
1 = C2OUT is present on RB7/C2/PSMC1B/$\overline{T1G}$(1)
0 = C2OUT is internal only

bit 4 **C2POL:** Comparator C2 Output Polarity Select bit
1 = C2OUT logic is inverted
0 = C2OUT logic is not inverted

bit 3 **C2SP:** Comparator C2 Speed Select bit
1 = C2 operates in normal speed mode
0 = C2 operates in low power, slow speed mode.

bit 2 **C2R:** Comparator C2 Reference Select bits (non-inverting input)
1 = C2VP connects to VDAC
0 = C2VP connects to VREF2

bit 1-0 **C2CH<1:0>:** Comparator C2 Channel Select bits
00 = C2VN of C2 connects to AN4
01 = C2VN of C2 connects to AN5
10 = C2VN of C2 connects to AN6
11 = C2VN of C2 connects to AN7

Note 1: C2OUT will only drive RB7/C2/PSMC1B/$\overline{T1G}$ if:
(C2OE = 1) & (C2ON = 1) & (TRISB<7> = 0) & ((SMCON = 0) or
((SMCOM = 0) & (SCEN = 0))).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

12.1.2.2 Control Register CM2CON1

Comparator C2 has one additional feature: its output can be synchronized to the Timer1 clock input. Setting C2SYNC (CM2CON1<0>) synchronizes the output of Comparator 2 to the falling edge of Timer 1's clock input (see Figure 12-1 and Register 12-3).

The CM2CON1 register also contains mirror copies of both comparator outputs, MC1OUT and MC2OUT (CM2CON1<7:6>). The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

REGISTER 12-3: COMPARATOR C2 CONTROL REGISTER1 (CM2CON1: 11Bh)

R-0	R-0	U-0	U-0	U-0	U-0	U-0	R/W-0
MC1OUT	MC2OUT	—	—	—	—	—	C2SYNC
bit 7							bit 0

bit 7 **MC1OUT:** Mirror Copy of C1OUT (CM1CON0<6>)

bit 6 **MC2OUT:** Mirror Copy of C2OUT (CM2CON0<6>)

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **C2SYNC:** C2 Output Synchronous Mode bit

1 = C2 output is synchronous to falling edge of TMR1 clock

0 = C2 output is asynchronous

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

12.2 Comparator Configuration

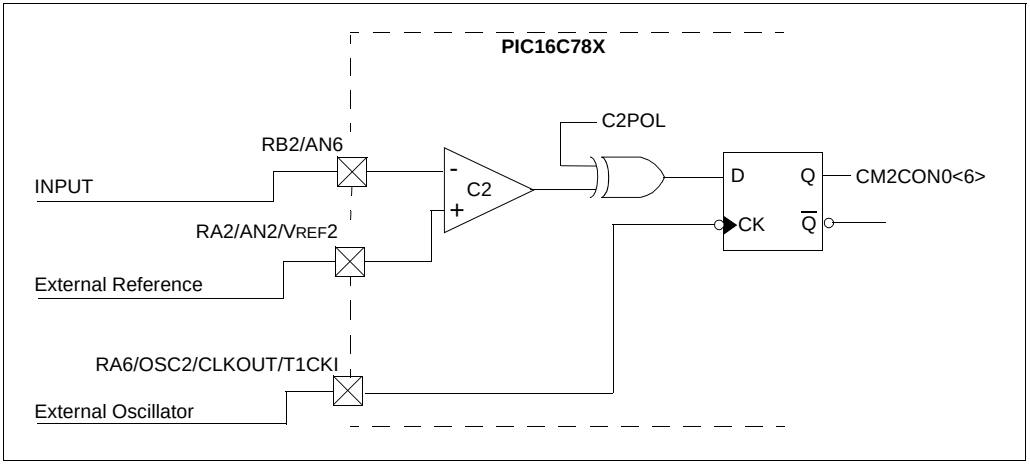
The following examples show the use of the Comparator module in:

- A simple voltage comparator configuration synchronized to the Timer 1 clock input.
- A comparator input to the PSMC with a programmable DAC reference.
- A low power window comparator configuration with interrupt-on-change.

12.2.1 EXAMPLE: C2 SYNCHRONIZED TO T1CKI

In this example, Comparator C2 is configured as a normal voltage comparator synchronized to the T1CKI input. A block diagram of the comparator with external connections is shown in Figure 12-2.

FIGURE 12-3: COMPARATOR C2 CONFIGURATION WITH OUTPUT SYNCHRONIZED TO T1CKI



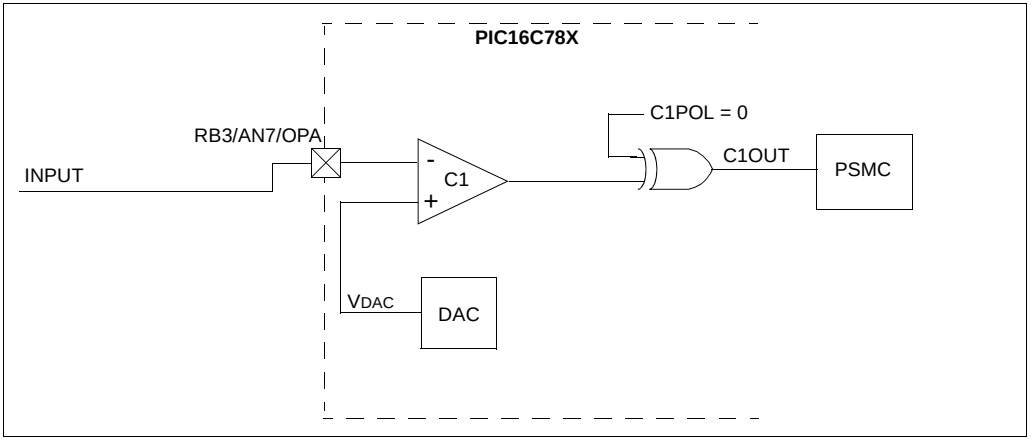
EXAMPLE 12-1: C2 CONFIGURATION PROGRAM

```
;*  This code block will configure C2
;*  for normal speed and output polarity,
;*  input on AN6, Reference from VREF2, and
;*  output synchronization to TMR1 clock.
;*
    BANKSEL TRISA          ; Select Bank 1
    BSF     TRISA,RA2      ; RA2 as input
    BSF     TRISA,RA6      ; RA6 as input
    BSF     TRISB,RB2      ; RB2 as input

    BSF     ANSEL,AN2      ; AN2 as analog
    BSF     ANSEL,AN6      ; AN6 as analog

    BANKSEL CM2CON0        ; Select Bank 2
    MOVLW   B'10001010'    ; Set C2; no out
    MOVWF   CM2CON0        ; VREF2, AN6

    BSF     CM2CON1,C2SYNC ; CLK sync
```

12.2.2 EXAMPLE: C1 INPUT TO PSMC W/ DAC AS REFERENCE

In this example, Comparator C1 is configured as a non-inverting normal speed voltage comparator input to the PSMC, with a programmable reference voltage. A block diagram of the comparator with external connections is shown in Figure 12-3.

FIGURE 12-4: CONFIGURATION OF COMPARATOR C1 WITH DAC



EXAMPLE 12-2: PROGRAMMING C1 FOR PSMC FEEDBACK

```
;*  This code block will configure Comparator
;*  C1 for normal speed and output polarity,
;*  input on AN7, and Reference from the DAC

    BANKSEL     TRISA       ; Select Bank 1
    BSF         TRISB,RB3   ; RB3 as input
    BSF         ANSEL,AN7   ; Set RB3 as analog

    BANKSEL     DACON0      ; Select Bank 2
    CLRF        DAC         ; DAC=00h
    MOVLW       B'10000000' ; Enable, no out
    MOVWF       DACON0      ; DACREF = VDD
    MOVLW       DAC_VALUE
    MOVWF       DAC         ; Trip Level

    MOVLW       B'10001111' ; C1; no out,
    MOVWF       CM1CON0     ; VREF1, AN7
```

12.2.3 EXAMPLE: LOW POWER WINDOW COMPARATOR WITH INTERRUPT

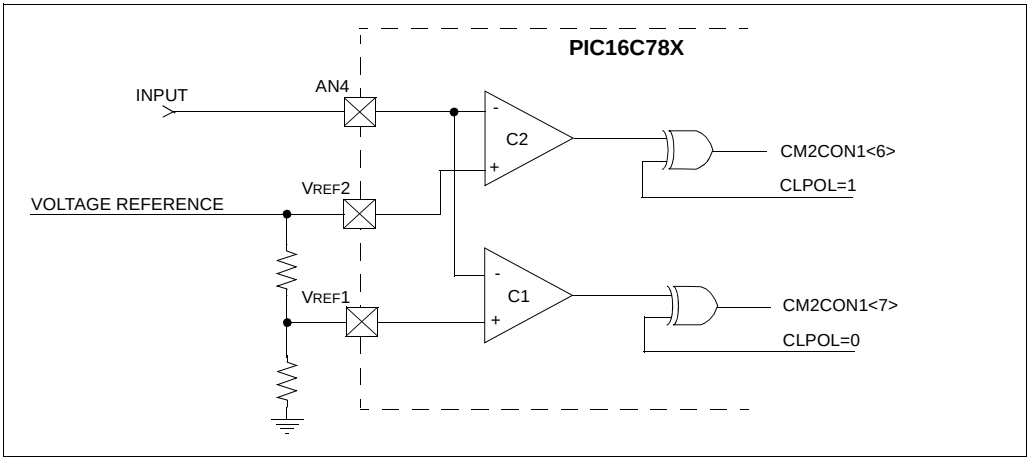
To form a low power window comparator, Comparators C1 & C2 are configured as follows:

- Common input RB0/INT/AN4/V_{REF}
- Separate external reference voltages
- Programmed for slow speed operation

In addition, the output of comparator C2 must be inverted for common polarity with C1.

A block diagram of the window comparator with external connections is shown in Figure 12-4.

FIGURE 12-5: WINDOW COMPARATOR WITH INTERRUPT



EXAMPLE 12-3: WINDOW COMPARATOR

```
;*  Example of Low Power Window Comparator C1
;*  This code block will configure Comparator
;*   C1 and C2 for slow speed, C1 non invert,
;*  C2 invert, input on AN4, and external
;*  References
;*
;*  Interrupt service routine included
;*
    BANKSEL     TRISA       ; Select Bank 1
    BSF         TRISA,2     ; RA2 input
    BSF         TRISA,3     ; RA3 input
    BSF         TRISB,0     ; Set RB0

    BSF         ANSEL,AN2   ; RA2 analog
    BSF         ANSEL,AN3   ; RA3 analog
    BSF         ANSEL,AN4   ; RB4 analog

    BANKSEL     CM1CON0     ; Select Bank 2
    MOVLW       B'10000000'; C1: no output
    MOVWF       CM1CON0     ; VREF1, AN4
    MOVLW       B'10010000'; C2: no output
    MOVWF       CM2CON0     ; invert,VREF1,AN4

    BANKSEL     PIE1        ; Select Bank 1
    BCF         INTCON,GIE  ; Disable Int
    BSF         PIE1,C1IE   ; Enabl C1&C2 Ints
    BSF         PIE1,C2IE
    BSF         INTCON,PEIE
    BSF         INTCON,GIE ; Enabl Global Ints
;*********************************************
;*  WINDOW COMPARATOR ISR with context save

WC_INT_SRV_R
    MOVWF       W_SAVE      ; Save W & STATUS
    SWAPF       STATUS,W
    MOVWF       STATUS_SAV

    BANKSEL     PIR1        ; Select Bank 0
    MOVLW       B'00110000'; Save Int
    ANDWF       PIR1,W
    MOVWF       WIN_INT

;*** CLEAR C1 INTERRUPT

    BTFSS       WIN_INT,C1IF; C1 Int ?
    GOTO        TST_C2_INT
    BANKSEL     CM1CON0     ; Select Bank 2
    MOVF        CM1CON0,F   ; Clear C2 mismatch
    BANKSEL     PIR1        ; Select Bank 0
    BCF         PIR1,C1IF   ; Clear C2 Int

;*** CLEAR C2 INTERRUPT

TXT_C2_INT
    BTFSS       WIN_INT,C2IF; C2 int?
    GOTO        USER_ISR
    BANKSEL     CM2CON0     ; Select Bank 2
    MOVF        CM2CON0,F   ; Clear C2 mismatch
    BANKSEL     PIR1        ; Select Bank 0
    BCF         PIR1,C1IF   ; Clear C2 int

USER_ISR
;*** USER INTERRUPT ROUTING
;*

    SWAPF       STATUS_SAVE,W; Restore W &
                            ; STATUS
    MOVWF       STATUS
    SWAPF       W_SAVE,F
    SWAPF       W_SAVE,W
    RETFIE                  ; Return
```

12.3 Effects of RESET

A RESET forces all registers to their RESET state. This disables both comparators.

TABLE 12-2: REGISTERS ASSOCIATED WITH THE COMPARATOR MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	0000 0000
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	—	C2SYNC	00-- ---0	00-- ---0
85h	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000	uuuu 0000
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx 0000	uuuu 0000
9Dh	ANSEL	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	1111 1111	1111 1111
0Ch	PIR1	LVDIF	ADIF	C2IF	C1IF	—	—	—	TMR1ON	0000 ---0	0000 ---0
8Ch	PIE1	LVDIE	ADIE	C2IE	C1IE	—	—	—	TMR1IE	0000 ---0	0000 ---0

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for comparator.

13.0 PROGRAMMABLE SWITCH MODE CONTROLLER (PSMC)

The Programmable Switch Mode Controller module provides all the necessary features to implement a pulsed feedback control system. The PSMC generates a pulse output based on its analog feedback.

Feedback from the comparator is programmable, allowing:

- Single or dual channel feedback
- Programmable reference voltage selection
- Programmable polarity

The pulse output of the PSMC is also programmable, featuring either Pulse Width (PWM) or Pulse Skip (PSM) Modulation. In PSM, a fixed duty cycle is generated or skipped, based on feedback. In PWM a feedback controlled pulse width is generated. In addition, the output configuration of the PSMC is programmable, enabling the following features:

- A single output
- A single output plus a slope compensation output
- Dual alternating outputs

All pulse start and duty cycle limit timing features of the PSMC are derived from the internal CPU clock.

Block diagrams for the PSMC are shown in Figure 13-1 through Figure 13-3.

13.1 Pulse Width Modulation (PWM)

In the PWM mode, the PSMC (shown in Figure 13-1 and Figure 13-2) is a timer-driven set/RESET pulse generator. Pulses are initiated by the internal counter chain. Following the completion of the programmable minimum duty cycle, the output pulse is terminated by either a high to low transition on the comparator output, or by the programmable maximum duty cycle (see Table 13-1 and Table 13-2). The resulting output is a variable duty cycle pulse with:

- Programmable frequency
- Feedback specified duty cycle
- Programmable minimum duty cycle including 0%
- Programmable maximum duty cycle

FIGURE 13-1: PSMC MODULE IN SINGLE OUTPUT PWM MODE (SIMPLIFIED BLOCK DIAGRAM)

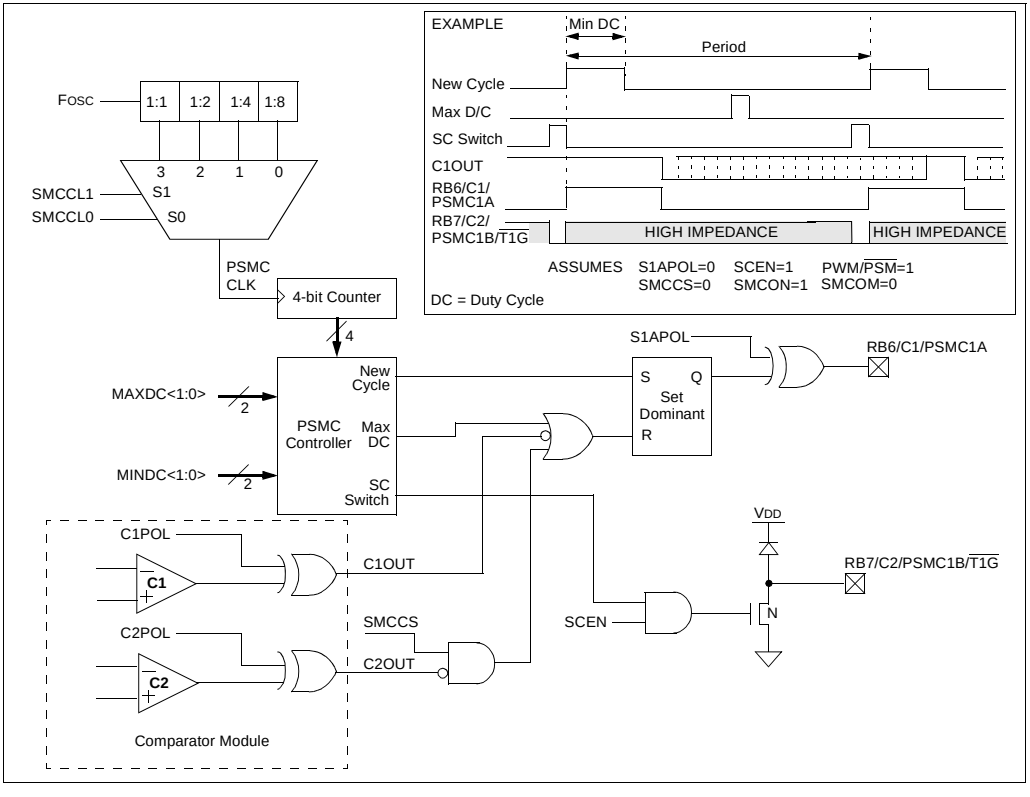


FIGURE 13-2: PSMC MODULE IN DUAL ALTERNATING OUTPUT PWM MODE (SIMPLIFIED BLOCK DIAGRAM)

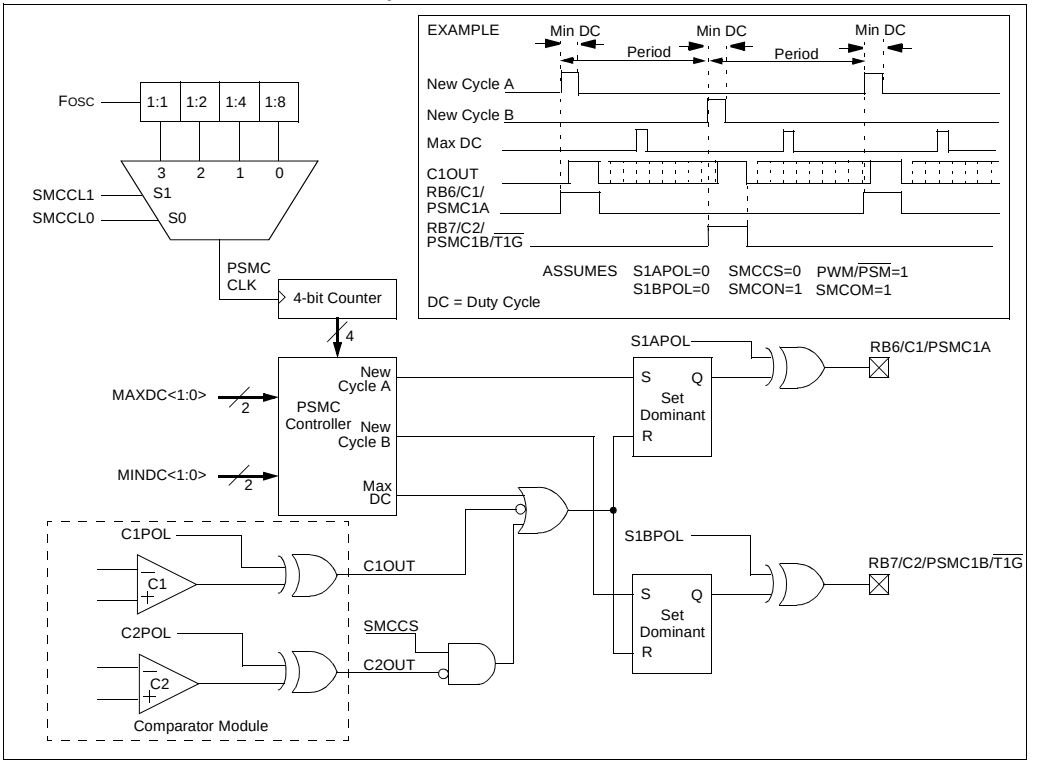


TABLE 13-1: PSMC1A OUTPUT SEQUENCE IN PWM MODE USING C1 COMPARATOR ONLY

Time	MINDC<1:0>	C1OUT	PSMC1A Output Signal
Beginning of PWM cycle	00	H	0 → 1
		L	0
	non-zero	x	0 → 1
During Min Duty Cycle	non-zero	x	1
After Min Duty Cycle, Before Max Duty Cycle	x	H → L	q→ 0
		L → H	0
Max Duty Cycle	x	x	q→ 0

Legend: x = Don't Care q = Prior State 0 = Inactive 1 = Active H = High L = Low

TABLE 13-2: PSMC1A OUTPUT SEQUENCE IN PWM MODE USING C1 AND C2 COMPARATORS

Time	MINDC<1:0>	C1OUT	C2OUT	PSMC1A Output Signal
Beginning of PWM cycle	00	H	H	0 → 1
		L	x	0
		x	L	0
	non-zero	x	x	0 → 1
During Min Duty Cycle	non-zero	x	x	1
After Min Duty Cycle, Before Max Duty Cycle	x	H → L	H	q → 0
		L → H	x	0
		H	H → L	q → 0
		x	L → H	0
Max Duty Cycle	x	x	x	q → 0

Legend: x = Don't Care q = Prior State 0 = Inactive 1 = Active H = High L = Low

13.1.1 PULSE SKIP MODULATION (PSM)

In PSM (Pulse Skip Modulation), the PSMC operates as a fixed duty cycle pulse generator, with its output gated by the analog feedback (see Figure 13-3). Immediately prior to the initiation of a pulse, the analog feedback is sampled. If the comparator output = H, a pulse is initiated and held active for the programmed duty cycle. If the comparator output = L, no pulse is initiated and the PSMC waits for the start of the next pulse (see Table 13-3 and Table 13-4). In this mode, both the frequency and duty cycle of the output pulse are programmable. The analog feedback gates the presence or absence of the pulse on a pulse-by-pulse basis.

FIGURE 13-3: PSMC MODULE IN SINGLE OUTPUT PSM MODE (SIMPLIFIED BLOCK DIAGRAM)

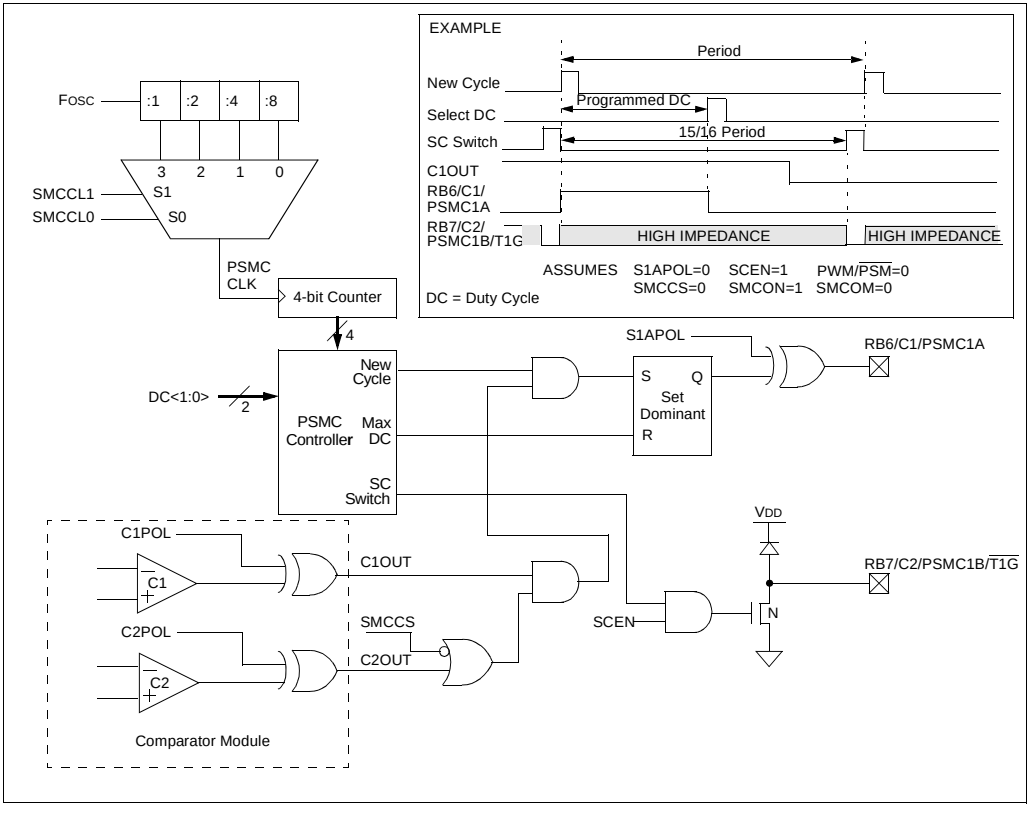


TABLE 13-3: PSMC1A OPERATION IN PSM MODE USING C1 COMPARATOR ONLY

Time	C1OUT	PSMC1A Output Signal
Beginning of PSM cycle	H	0 → 1
	L	0
During Pulse	x	No Change
		1
End of Pulse	x	1 → 0

Legend: x = Don't Care 0 = Inactive 1 = Active H = High L = Low

TABLE 13-4: PSMC1A OUTPUT SEQUENCE IN PSM MODE USING C1 AND C2 COMPARATORS

Time	C1OUT	C2OUT	PSMC1A Output Signal
Beginning of PSM cycle	H	H	0 → 1
	L	x	0
	x	L	0
During Pulse Duty Cycle	x	x	No Change
	x	x	No Change
After Pulse Duty Cycle	x	x	1 → 0

Legend: x = Don't Care 0 = Inactive 1 = Active H = High L = Low

13.1.2 SINGLE OR DUAL OUTPUT

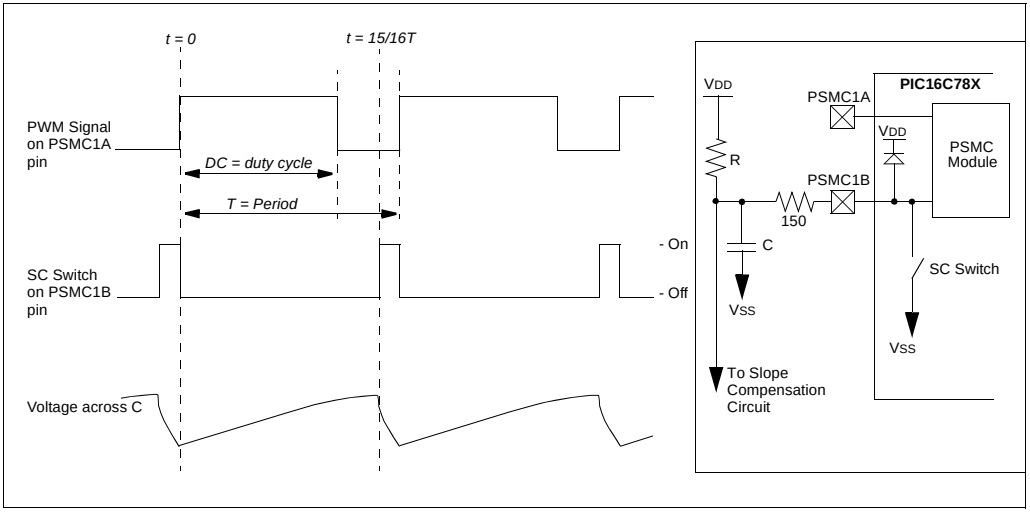
The PSMC has the capability to operate with either a single output, or dual alternating outputs. In the single output mode, the PSMC generates an output pulse on PSMC1A output only. The pulses are at the programmed frequency, and are variable between the programmed minimum and maximum duty cycle limits. In the dual output mode, the PSMC generates output pulses which alternate between PSMC1A and PSMC1B. The pulses generated at each output are generated at one half of the programmed frequency, and between 50% of the programmed minimum. and 50% maximum of the output duty cycle. The maximum duty cycle for either output is 50%.

13.1.3 SLOPE COMPENSATION

An optional feature of the PSMC single output mode is the ability to configure the PSMC1B output for use as a slope compensation ramp generator. In this mode, the PSMC1B output is pulled low for the last 1/16 of each pulse cycle. Connecting the PSMC1B output to an RC network, similar to Figure 13-4, results in a positive going pseudo ramp function. This pseudo ramp function is useful as an offset function for the loop error signal in unstable conditions at a duty cycle of greater than 50%.

Note:	When the Slope Compensation switch is enabled (SMCOM = 0, and SCEN = 1), the S1BPOL bit has no effect (see RC Network on next page for more detail).

FIGURE 13-4: SLOPE COMPENSATION (SC) SWITCH OPERATION



13.2 Control Registers

The PSMC is controlled by means of two special function registers: PSMCCON0 and PSMCCON1.

The PSMCCON0 register (Register 13-1) contains control bits for:

- Frequency of the output pulse
- Minimum and maximum duty cycle in PWM mode
- Fixed duty cycle in PSM mode

The PSMCCON1 register (Register 13-2) contains the control bits for:

- Enabling the PSMC module
- Setting the PSMC mode
- Configuring inputs and outputs

Note:	Following RESET, both the PSMC1A and PSMC1B outputs are held tri-state until the PSMC is configured. Driver circuitry for all power MOSFET transistors must have a resistor bias to turn off the transistor in the event of tri-state conditions, on either PSMC1A or PSMC1B, to prevent excessive stress on the MOSFET's and their associated circuitry.

13.2.1 PSMCCON0 REGISTER

The SMCCL<1:0> bits in the PSMCCON0 register, are used to set the pulse frequency of the PSMC.

Note:	Changing SMCCL<1:0> bits with the PSMC enabled (SMCON=1) can result in unpredictable output. Always disable PSMC before changing SMCCL<1:0>.

In the PWM mode, the MINDC <1:0> bits (PSMCCON0 <5:4>) specify the minimum duty cycle.

In the PWM mode, the MAXDC <1:0> bits (PSMCCON0 <3:2>) specify the maximum duty cycle limit.

In the PSM mode, the DC<1:0> bits (PSMCCON0<1:0>) specify the fixed duty cycle.

13.2.2 PSMCCON1 REGISTER

To enable the PSMC operation, the SMCON bit in the PSMCCON1 register must be set (see Register 13-2).

The PWM/$\overline{\text{PSM}}$ bit (PSMCCON1<1>) configures the output mode of the PSMC. When the PWM/$\overline{\text{PSM}}$ bit is set, the PSMC is configured for a PWM output. When the PWM/$\overline{\text{PSM}}$ bit is cleared, a fixed duty cycle pulse is output.

The SMCCS bit (PSMCCON1<0>) sets the input mode. When the SMCCS bit is set, the PSMC is configured for two inputs: C1 and C2. When cleared, only Comparator C1 is used.

SMCOM bit (PSMCCON1<1>) determines the number of outputs from the PSMC. When SMCOM is set, both PSMC1A and PSMC1B are active. When SMCOM is cleared, only the PSMC1A output is active and the PSMC1B output is available for another function.

S1APOL and S1BPOL control the polarity of the PSMC outputs. Setting the polarity bit configures the corresponding output for an active low state. Clearing the bit results in an active high output.

The SCEN bit (PSMCCON1<2>) enables the slope compensation output. When SCEN is set (and SMCOM is cleared) the PSMC1B output is configured to generate a slope compensation signal.

Note:	PSMC outputs must have their corresponding direction bits cleared in TRISB; TRISB<6>: for PSMC1A, and TRISB<7> for PSMC1B.

TABLE 13-5: PSMC OUTPUT MODES

FUNCTION	PSMC		PORTB	
	SMCOM	SCEN	TRISB<6>	TRISB<7>
Single Output	0	0	0	*
Single Output + Slope Compensation	0	1	0	0
Dual Output	1	x	0	0

Legend: x = Don't Care
*As needed for other functions (such as C2, RB7, $\overline{\text{T1G}}$).

REGISTER 13-1: PSMC CONTROL REGISTER0 (PSMCCON0: 111h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SMCCL1	SMCCL0	MINDC1	MINDC0	MAXDC1	MAXDC0	DC1	DC0
bit 7							bit 0

bit 7-6 **SMCCL<1:0>:** Clock Frequency Select bits
00 = Output frequency for single output mode is FOSC/128
01 = Output frequency for single output mode is FOSC/64
10 = Output frequency for single output mode is FOSC/32
11 = Output frequency for single output mode is FOSC/16

bit 5-4 **MINDC<1:0>:** Minimum Duty Cycle Select bits for PWM Mode
00 = Min duty cycle of 0
01 = Min duty cycle of 1/8
10 = Min duty cycle of 1/4
11 = Min duty cycle of 3/8

bit 3-2 **MAXDC<1:0>:** Maximum Duty Cycle Select bits for PWM Mode
00 = Max duty cycle of 1/2
01 = Max duty cycle of 5/8
10 = Max duty cycle of 3/4
11 = Max duty cycle of 15/16

bit 1-0 **DC<1:0>:** Duty Cycle Select bits for PSM Mode
00 = Duty cycle of 1/8
01 = Duty cycle of 3/8
10 = Duty cycle of 5/8
11 = Duty cycle of 15/16

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 13-2: PSMC CONTROL REGISTER1 (PSMCCON1: 112h)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SMCON	S1APOL	S1BPOL	—	SCEN	SMCOM	PWM/$\overline{\text{PSM}}$	SMCCS
bit 7							bit 0

bit 7 **SMCON:** PSMC Module Enable bit
1 = PSMC module on
0 = PSMC module off

bit 6 **S1APOL:** PSMC1A Output Polarity Control bit
1 = PSMC1A output signal is asserted low
0 = PSMC1A output signal is asserted high

bit 5 **S1BPOL:** PSMC1B Output Polarity Control bit
1 = PSMC1B output signal is asserted low
0 = PSMC1B output signal is asserted high

bit 4 **Unimplemented:** Read as '0

bit 3 **SCEN:** Slope Compensation Output Enable bit
If SMCOM = 1:
x = This bit is ignored
If SMCOM = 0:
1 = Slope Compensation Switch on PSMC1B pin is enabled
0 = Slope Compensation Switch on PSMC1B pin is not enabled. PSMC1B pin is available for other functions.

bit 2 **SMCOM:** PSMC Output Mode bit
1 = Dual alternating output mode. The module outputs are available on the PSMC1A and PSMC1B pins.
0 = Single output mode. The module output is available on the PSMC1A pin.

bit 1 **PWM/$\overline{\text{PSM}}$:** PSMC Modulation Mode Select bit
1 = PWM mode (Pulse Width Modulation)
0 = PSM mode (Pulse Skipping Modulation)

bit 0 **SMCCS:** PSMC Comparator Select bit
1 = PSMC module uses inputs from both C1OUT and C2OUT
0 = SMC module uses input from C1OUT only

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

13.3 Configuration

The programmable nature of the PSMC lends itself to a wide variety of applications involving current or voltage management. The following examples are intended to provide suggested applications for the PSMC. The examples are not complete designs, but rather block diagrams of some potential applications of the PSMC. For a broader list of applications, including supporting math and firmware examples, please refer to Microchip web page for applicable Application Notes.

13.3.1 EXAMPLE BOOST LC SWITCHING POWER SUPPLY

In this example, the PSMC controls the boost configuration switching power supply in Figure 13-5.

The PSMC is configured as a two feedback loop PWM, current mode, switching power supply controller. The inner current feedback loops consist of:

- PSMC
- MOSFET driver
- Power MOSFET Q1
- Inductor L1
- Current transformer
- Comparator C1

The outer voltage feedback loop consists of:

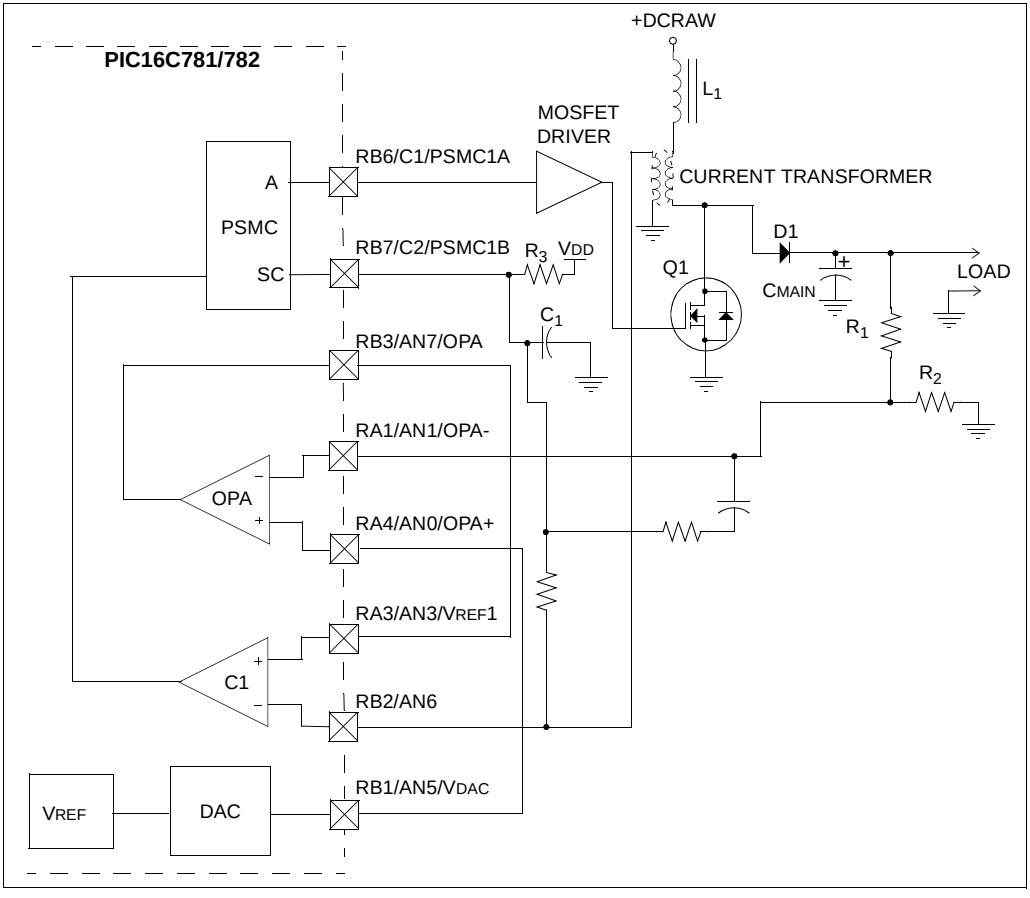
- Diode D1
- CMAIN
- OPAMP feedback filter
- DAC reference

The inner current loop is a pulsed current source driven by the PSMC. During the active phase of the output pulse, the inner loop builds up a current flow in inductor L1. The current in L1 is monitored by the current transformer. The output of the transformer is offset by the ramp from the slope compensation network R3/C1 and then fed into the comparator. When the voltage (proportional to the current flow in L1, offset by the slope compensation) exceeds the error voltage from the OPAMP, Q1 is turned off and L1 discharges through D1 into CMAIN for the remainder of the period.

The outer voltage loop monitors the output voltage across CMAIN using R1/R2. The reference voltage from the DAC is subtracted, generating the raw error voltage. The raw error voltage is filtered by the OPAMP and routed to Comparator C1 in the inner current loop.

The phase compensation output of the PSMC acts to improve loop stability by adding a pseudo-ramp waveform to the current sense transformer feedback in the inner loop. In conditions where the charge phase of the cycle is greater then 50%, the increased current feedback reduces the current charge in L1, slowing the charging of CMAIN. The result is a reduction in the overall loop gain for duty cycles of >50%, maintaining loop stability.

FIGURE 13-5: EXAMPLE BOOST CONFIGURATION LC SWITCHING POWER SUPPLY



Note:	The OPAMP, Comparator and DAC must be configured, prior to enabling the PSMC to prevent unpredictable operation which may stress the power MOSFET transistors.

EXAMPLE 13-1: PSMC CONFIGURATION EXAMPLE

```
;* This code block will configure the PSMC and
;*   all additional peripherals for a boost mode
;*   switching power supply.
;*
;*  Order of configuration
;*  1.  PORTA/B I/O and analog configured
;*  2.  DAC enabled, configured, and preset
;*  3.  Op Amp enabled and configured
;*  4.  Comparator C1 enabled and configured
;*  5.  PSMC configured
;*  6.  PSMC enabled


************************************************************
;*  This code block will configure all analog ports.

    BANKSEL     TRISA               ; Select Bank 1
    MOVLW       B'00001011'
    MOVWF       TRISA               ; Set RA0,1,& 3 as inputs
    MOVLW       B'11001110'
    MOVWF       TRISB               ; Set RB1,2,3,6 & 7 as inputs
    MOVLW       B'11101011'         ; Configure RA0, RA1, RA3,
    MOVWF       ANSEL               ; RB1, RB2, RB3 as analog

;*********************************************************************
;*  This code block will configure the DAC for VDD as
;*  DACREF, and RB1/AN5/VDAC as an output

    BANKSEL     DACON0              ; Select Bank 2

    CLRF        DAC                 ; Set DAC to safe value
    MOVLW       B'11000000'         ; Enable DAC, output
    MOVWF       DACON0              ;   and set DACREF = VDD

    MOVLW       OUTPUT_VALUE
    MOVWF       DAC                 ; Set DAC output level
;*********************************************************************
;*  This code block will configure the OPA module as an
;*  Op Amp, with a 2MHz GBWP

    MOVLW       B'10000001'         ; Set Op Amp mode and
    MOVWF       OPACON              ;  2MHz GBWP

;*********************************************************************************
;*  This code block will configure Comparator C1
;*  for normal speed and output polarity,
;*  input on AN6, and Reference from the VREF1

    MOVLW       B'10001010          ; Set C1, no ext out, norm
    MOVWF       CM1CON0             ;   speed & pol, VREF1, AN6

;*********************************************************************
;*  This code block will configure the PSMC module
;*  for PWM, FOSC/128, Single in, Single pulse out, slope comp out
;*  Non-inverting out, DC min = 0%, DC max = 75%

    MOVLW       B'00001000'
    MOVWF       PSMCCON0            ; Set DCmin 0, DCmax 75, FOSC/128
    MOVLW       B'00001010'         ; Set PWM Sngl in, Sngl out non-invert
    MOVWF       PSMCCON1            ; Slope comp
    BSF         PSMCCON1,SMCON      ; Enable PSMC
```

13.3.2 EXAMPLE BUCK LC SWITCHING POWER SUPPLY

In this example, the PSMC controls the buck configuration switching power supply in Figure 13-6.

The PSMC is configured as a typical PWM, current mode, switching power supply controller. The inner current feedback loops consist of:

- PSMC
- 2 MOSFET drivers
- Power MOSFETs Q1 and Q2
- Inductors L1 and L2
- Current transformer
- Comparator C1/C2

The outer voltage feedback loop consists of:

- Diodes D1, D2, D3, and D4
- CMAIN
- OPAMP feedback filter
- DAC reference

The circuit uses two feedback loops, an inner current control loop, and an outer voltage loop. The inner loop is further divided into two channels, Q1/L1, and Q2/L2. The PSMC operates a PWM output, alternately driving Q1 for a cycle, then driving Q2 the next. During the active phase of either output pulse, the inner loop builds up a current flow in the output's inductor, proportional to the error voltage received from the OPAMP. The current flow in the inductor begins the charging of CMAIN. When the voltage (proportional to the current flow in the inductor) exceeds the error voltage:

- The comparator resets the PSMC output
- The MOSFET is turned off
- The flyback diode forward biases
- The inductor discharges into CMAIN for the remainder of the period.

The outer voltage loop monitors the output voltage across CMAIN via R1/R2. The reference voltage from the DAC is subtracted from the feedback voltage to generate the raw error voltage. The raw error voltage is then filtered by the OPAMP and routed to Comparator C1 in the inner current loop.

In using two alternating outputs, the outputs are limited to less than 50% duty cycle. As a result, the circuit avoids the problems associated with instability at duty cycles of >50%.

For more information concerning the design of switching power supplies, refer to:

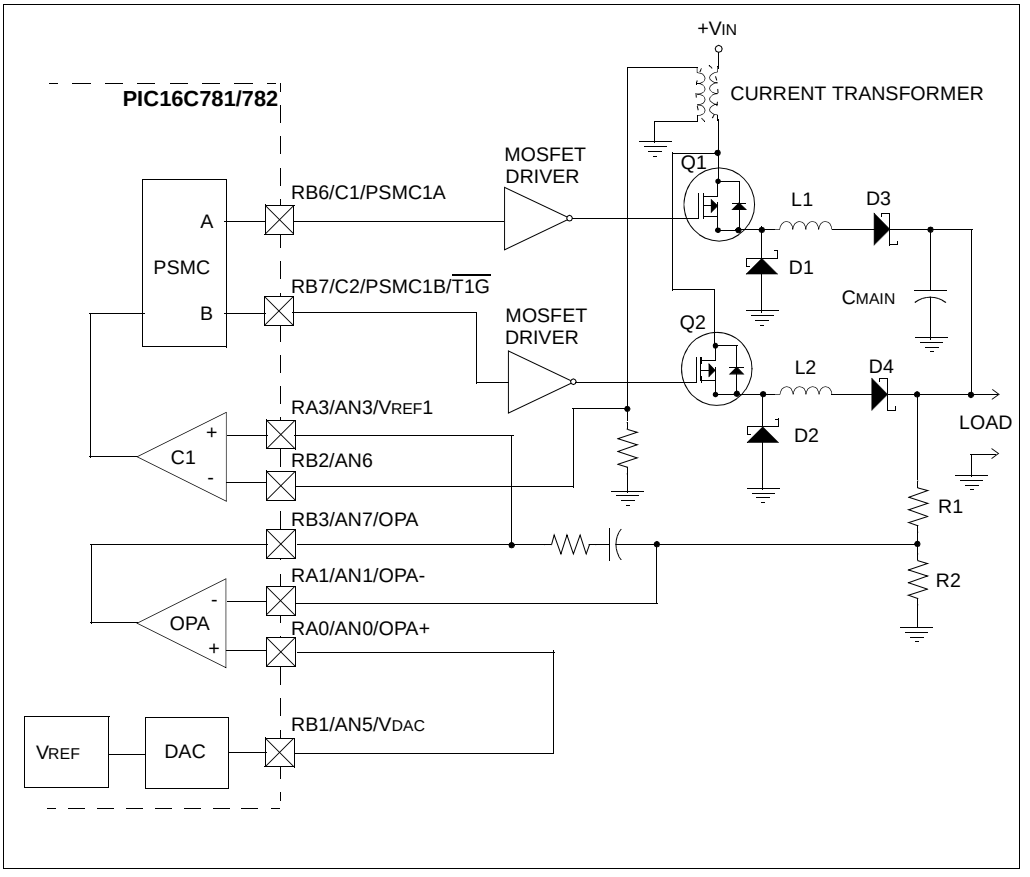
Switching Power Supply Design, by Abraham I. Pressman, published by McGraw Hill (ISBN 0-07-052236-7).

Note:	Following RESET, both the PSMC1A and PSMC1B outputs are held tri-state until the PSMC is configured. Driver circuitry for all power MOSFET transistors must have a resistor bias to turn off the transistor in the event of tri-state conditions on either output to prevent undo stress on the MOSFET's and their associated circuitry.

EXAMPLE 13-2: EXAMPLE PSMC CONFIGURATION FOR A BUCK MODE SWITCHING POWER SUPPLY

```
;*  PSMC Initialization
;*  This code block will configure the PSMC
;*  and all additional peripherals for a buck
;*  mode switching power supply.
;*
;*  Order of configuration
;*  1.  PORTA/B I/O and analog configured
;*  2.  DAC enabled, configured, and preset
;*  3.  Op Amp enabled and configured
;*  4.  Comparator C1 enabled and configured
;*  5.  PSMC configured
;*  6.  PSMC enabled
;*****************************************
;*  This code block will configure all analog ports.
;
    BANKSEL     TRISA               ; Select Bank 1
    MOVLW       B'00001011'
    MOVWF       TRISA               ; Set RA0,1,& 3 as inputs
    MOVLW       B'11001110
    MOVWF       TRISB               ; Set RB1,2,3,6 & 7 as inputs
    MOVLW       B'11101011'
    MOVWF       ANSEL               ; Set AN0,1,3,5,6 & 7 as analog

;*****************************************************
;*  This code block will configure the DAC for VDD as
;*  DACREF, and RB1/AN5/VDAC as an output.

    BANKSEL         DACON0              ; Select Bank 2

    CLRF            DAC                 ; Set DAC to safe value
    MOVLW           B'11000000'         ; Enable DAC, output
    MOVWF           DACON0              ;   and set DACREF = VDD

    MOVLW           OUTPUT_VALUE
    MOVWF           DAC                 ; Set dAC output level

;*****************************************************
;*  This code block will configure the OPA module
;*  as an Op Amp, with a 3 MHZ GBWP

    MOVLW           B'10000001'         ; Set Op Amp mode and
    MOVWF           OPACON              ;  2 MHz GBWP

;*****************************************************
;*  This code block will configure Comparator C1
;*  for normal speed and output polarity,
;*  input on AN6, and Reference from the VREF1

    MOVLW           B'10001010'         ; Set C1; no ext out, norm
    MOVWF           CM1CON0             ;  speed & pol, VREF1, AN6

;*****************************************************
;*  This code block will configure the PSMC module
;*  for PWM, Fosc/128, Single input, Single output
;*  Non-inverting out, DC min = 0%, DC max = 50%

    MOVLW           B'0000000'
    MOVWF           PSMCCON0            ; Set DCmin 0, DCmax 50, Fosc/128
    MOVLW           B'00000110'
    MOVWF           PSMCCON1            ; Set PWM, 1 in, 2 out, noninvert
    BSF             PSMCCON1,SMCON      ; Enable PSMC
```

FIGURE 13-6: EXAMPLE BUCK CONFIGURATION LC POWER SUPPLY



13.3.3 EXAMPLE MOTOR SPEED CONTROL

In Figure 13-7, the PSMC acts as a speed control for a brushless DC motor. The direction of the current in the motor winding is set by feedback from a Hall effect position sensor on the motor. The sensor switches the phase in the motor in response to the rotation of the rotor so that the magnetic field rotates just ahead of the rotor, pulling it in the desired direction. The speed at which the rotor spins is a function of the mechanical load on the rotor and the current in the field winding.

Speed control is accomplished by monitoring the speed via the Hall effect sensor and regulating the current in the winding appropriately. The winding current is regulated by the PSMC to be proportional to the value supplied by the DAC module. The feedback loop is closed by software making periodic measurement of the rotor speed using the Hall Effect sensor/Timer1 and adjusting the output value of the DAC appropriately.

The algorithm (used to determine the values output by the DAC module) depends on:

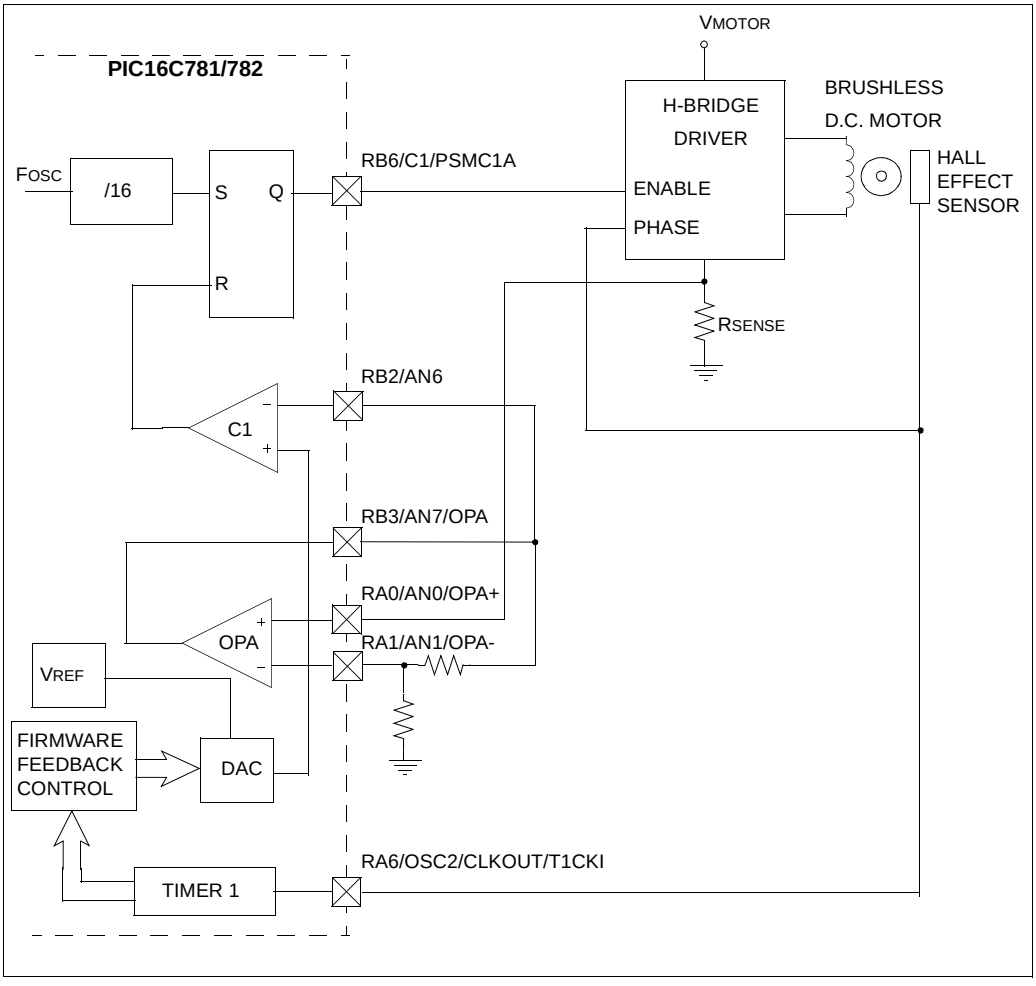
- mechanical system connected to the motor
- motor characteristics
- characteristics of the high current drive

An analysis of the mechanics of the system and the design of an appropriate control algorithm is beyond the scope of this Data Sheet. Therefore, the designer should consult a text dealing with the design of motor speed controls and feedback control system, in general, for the necessary design guidance.

EXAMPLE 13-3: PERIPHERAL CONFIGURATION EXAMPLE

```
;***********************************************
;*  This code block will configure the PSMC and
;*  all additional peripherals for a motor speed
;*  control.
;*
;*  Order of configuration
;*  1.  PORTA/B I/O and analog configured
;*  2.  DAC enabled, configured, and preset
;*  3.  Op Amp enabled and configured
;*  4.  Comparator C1 enabled and configured
;*  5.  PSMC configured
;*  6.  PSMC enabled
;*
;***********************************************
;*  This code block will configure all analog ports.

    BANKSEL     TRISA               ; Select Bank 1
    MOVLW       B'01000011'
    MOVWF       TRISA               ; Set RA0,1 & 6 as inputs
    MOVLW       B'00001100'
    MOVWF       TRISB               ; Set RB2 & 3 as inputs
    MOVLW       B'11000011'
    MOVWF       ANSEL               ; Set AN0,1,6,& 7 as analog

;***********************************************
;*  This code block will configure the DAC for VR as
;*  DACREF, and no output.

    BANKSEL     REFCON
    BSF         REFCON, VREN        ; Enable VR
    BANKSEL     DACON0              ; Select Bank 2

    CLRF        DAC                 ; Set DAC to safe value
    MOVLW       B'10000010'         ; Enable DAC, no output
    MOVWF       DACON0              ;  and set DACREF = VR

    MOVLW       OUTPUT_VALUE
    MOVWF       DAC                 ; Set DAC output level

;***********************************************
;*  This code block will configure the OPA module
;*  as an Op Amp, with a 2 MHz GBWP

    MOVLW       B'10000001'         ; Set Op Amp mode and
    MOVWF       OPACON              ;  2 MHz GBWP

;***********************************************
*   This code block will configure Comparator C1
*   for normal speed and output polarity,
*   input on AN6, and Reference from the VDAC

    MOVLW       B'10001110'         ; Set C1; no ext out, norm
    MOVWF       CM1CON0             ;  speed & pol, VDAC, AN6

;***********************************************
;*  This code block will configure the PSMC module
;*  for PWM, Fosc/16, Single input, Single output
;*  Non-inverting out, DC min = 0%, DC max = 94%

    MOVLW       B'11001100'
    MOVWF       PSMCCON0            ; Set DCmin 0, DCmax 94, Fosc/16
    MOVLW       B'00000010'
    MOVWF       PSMCCON1            ; Set PWM, Sngl in/out, noninvert
    BSF         PSMCCON1,SMCON      ; Enable PSMC
```

FIGURE 13-7: EXAMPLE BRUSHLESS D.C. MOTOR CONTROL



13.4 Effects of SLEEP and RESET

A device RESET forces all registers to their RESET state. This disables the PSMC and resets its outputs to digital inputs. It is good design practice to include a fail-safe resistor bias in all power transistor drive circuitry. The fail-safe circuit should disable the power device when the PSMC output drive transistor is held tri-state. This protects the power device and its associated circuitry from the stress of prolonged operation without feedback.

Placing the PIC16C781/782 into SLEEP mode will stop the main oscillator for the microcontroller. The PSMC derives its timing from the main oscillator. Therefore, operation of the PSMC will halt when the microcontroller enters SLEEP mode. To prevent damage, the outputs of the PSMC are gated so that they are driven to their inactive state whenever the device enters SLEEP mode. When the microcontroller wakes up, the PSMC resumes operation per its previously programmed configuration.

TABLE 13-6: REGISTERS ASSOCIATED WITH THE PSMC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
86h,186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	0000 0000
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
111h	PSMCCON0	SMCCL1	SMCCL0	MINDC1	MINDC0	MAXDC1	MAXDC0	DC1	DC0	0000 0000	0000 0000
112h	PSMCCON1	SMCON	S1APOL	S1BPOL	—	SCEN	SMCOM	PWM/$\overline{\text{PSM}}$	SMCCS	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for PSMC.

NOTES:

14.0 SPECIAL FEATURES OF THE CPU

These devices have a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features include:

- Oscillator selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Programmable Brown-out Reset (PBOR)
- Interrupts
- Watchdog Timer (WDT)
- Programmable Low Voltage Detection (PLVD)
- SLEEP
- Code protection
- ID locations
- In-Circuit Serial Programming™ (ICSP™)

Several oscillator options are available to allow the part to fit the application. The INTRC oscillator options save system cost while the LP crystal option saves power. A set of configuration bits is used to select various options.

The CPU also features a Watchdog Timer (WDT), which can be enabled either through a configuration bit during programming, or by the software. For added reliability, the WDT runs off its own internal RC oscillator instead of the main CPU clock.

In addition to the WDT, the CPU incorporates both an Oscillator Start-up Timer and a Power-up Timer. The Oscillator Start-up Timer (OST) is intended to hold the chip in RESET until the crystal oscillator has stabilized. The Power-up Timer (PWRT) holds the CPU in a fixed RESET delay of 72ms (nominal) on Power-up Resets (POR and PBOR), while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can awaken from SLEEP through:

- External RESET
- Watchdog Timer Wake-up
- Interrupt

Additional information on special features is available in the PIC Mid-Range Reference Manual, (DS33023).

14.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space, which can be accessed only during programming.

Some of the core features provided may not be necessary for each application in which a device may be used. The configuration word bits allow these features to be configured/enabled/disabled as necessary. These features include:

- Code Protection
- PBOR Trip Point
- Power-up Timer
- Watchdog Timer
- Device Oscillator Mode

As can be seen in Table 14-1, some additional configuration word bits have been provided for Brown-out Reset trip point selection.

REGISTER 14-1: CONFIGURATION WORD FOR PIC16C781/782 DEVICE (CONFIG:2007h)

$\overline{CP}$	$\overline{CP}$	BORV1	BORV0	$\overline{CP}$	$\overline{CP}$	—	BODEN	MCLRE	$\overline{PWRTE}$	WDTE	F0SC2	F0SC1	F0SC0
bit13													bit0

bit 13-12, 9-8 **CP:** Program Memory Code Protection bits
1 = Code Protection off
0 = All program memory is protected(1)

bit 11-10 **BORV<1:0>:** Brown-out Reset Voltage bits
00 = PBOR set to 4.5V
01 = PBOR set to 4.2V
10 = PBOR set to 2.7V
11 = PBOR set to 2.5V

bit 7 **Unimplemented:** Read as '1'

bit 6 **BODEN**: Brown-out Detect Reset Enable bit(1)
1 = Brown-out Detect Reset enabled
0 = Brown-out Detect Reset disabled

bit 5 **MCLRE:** RA5/$\overline{MCLR}$ Pin Function Select bit
1 = RA5/$\overline{MCLR}$ pin function is $\overline{MCLR}$
0 = RA5/$\overline{MCLR}$ pin function is digital input, $\overline{MCLR}$ internally tied to V_{DD}

bit 4 **$\overline{PWRTE}$**: Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0 **FOSC<2:0>**: Oscillator Selection bits

FOSC<2:0>	OSCILLATOR	RA6/OSC2/CLKOUT/T1CKI	RA7/OSC1/CLKIN
000	LP	Crystal/Resonator	Crystal/Resonator
001	XT	Crystal/Resonator	Crystal/Resonator
010	HS	Crystal/Resonator	Crystal/Resonator
011	EC	Digital I/O	CLKIN
100	INTRC	Digital I/O	Digital I/O
101	INTRC	CLKOUT	Digital I/O
110	RC	Digital I/O	RC
111	RC	CLKOUT	RC

Note 1: All of the CP bits must be given the same value to enable code protection.

14.2 Oscillator Configurations

14.2.1 OSCILLATOR TYPES

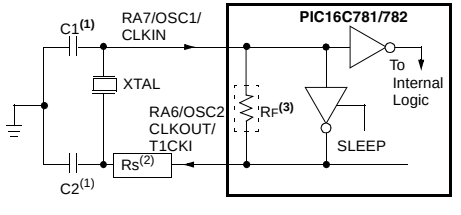
The PIC16C781/782 can be operated in eight different oscillator modes. The user can program three configuration bits FOSC<2:0> to select one of these eight modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC External Resistor and Capacitor (with and without CLKOUT)
- INTRC Internal 4 MHz/37 kHz (with and without CLKOUT)
- EC External Clock

14.2.2 LP, XT AND HS MODES

In LP, XT, or HS modes, a crystal or ceramic resonator is connected to the RA7/OSC1/CLKIN and RA6/OSC2/CLKOUT/T1CKI pins to establish oscillation (Figure 14-1). The PIC16C781/782 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may yield a frequency outside of the crystal manufacturers' specifications.

FIGURE 14-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Table 14-1 and Table 14-2 for recommended values of C1 and C2.

2: A series resistor (RS) may be required for AT strip cut crystals.

3: RF varies with the crystal chosen.

TABLE 14-1: CERAMIC RESONATORS

Ranges Tested:			
Mode	**Freq**	**C1**	**C2**
XT	455 kHz 2.0 MHz 4.0 MHz	68 - 100 pF 15 - 68 pF 15 - 68 pF	68 - 100 pF 15 - 68 pF 15 - 68 pF
HS	8.0 MHz 16.0 MHz	10 - 68 pF 10 - 22 pF	10 - 68 pF 10 - 22 pF
These values are for design guidance only. See Notes 1 and 2 in shaded box.			
In this test, all resonators used did not have built-in capacitors.			

TABLE 14-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF
These values are for design guidance only. See Notes 1 and 2 in shaded box.			

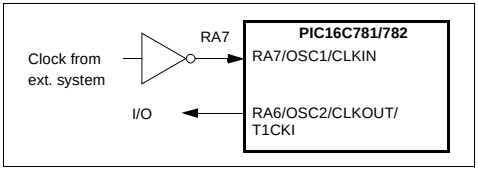
Note 1: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

2: Higher capacitance increases the stability of oscillator but also increases the start-up time.

14.2.3 EC MODE

In applications where the clock source is external, the PIC16C781/782 should be programmed to select the EC (External Clock) mode. In this mode, the RA6/OSC2/CLKOUT/T1CKI pin is available as an I/O pin. See Figure 14-2 for illustration. To minimize power supply current drawn, the EC oscillator input should be driven by a CMOS level square wave.

FIGURE 14-2: EC OSC CONFIGURATION



14.2.4 RC MODE

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of:

- supply voltage
- resistor (REXT) and capacitor (CEXT) values
- operating temperature

In addition, the oscillator frequency varies from unit to unit due to normal process variation. The difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low CEXT values. The user should allow for variations due to tolerance of external R and C components used. Figure 14-3 shows how the RC combination is connected to the PIC16C781/782. For REXT values below 2.2 kΩ, the oscillator operation may become unstable or stop completely. For very high REXT values (e.g., 1 MΩ or greater), the oscillator becomes sensitive to:

- noise
- humidity
- leakage

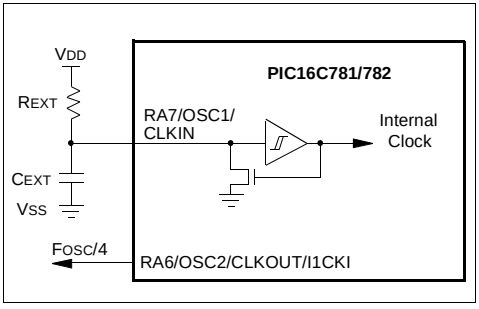
Microchip recommends keeping REXT between 3 kΩ and 100 kΩ.

Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as board trace capacitance or package lead frame capacitance.

See Section 18.0 for RC frequency variation from part to part due to normal process variation. The variation is greater for large values of R (since leakage current variations affect RC frequency more for large R) and for small values of C (since variations of input capacitance affect RC frequency more).

See Section 18.0 for variation of oscillator frequency due to VDD for given REXT and CEXT values (or for frequency variation due to operating temperature for given R, C, and VDD values).

FIGURE 14-3: RC OSCILLATOR MODE



14.2.5 INTRC MODE

The internal RC oscillator provides a fixed 4 MHz/37 kHz (nominal) system clock at VDD = 5V and 25°C. See Section 18.0 for information on variations over voltage and temperature ranges. The INTRC oscillator does not run during RESET.

14.2.6 DUAL SPEED OPERATION FOR INTRC MODE

A software programmable slow speed mode is available with the INTRC oscillator. This feature allows the firmware to dynamically toggle the oscillator speed between normal and slow frequencies. The nominal slow frequency is 37 kHz. Applications that require low current power savings, but cannot tolerate putting the part into SLEEP, may use this mode.

The OSCF bit (PCON<3>) is used to control dual speed mode. See the PCON Register, Register 2-6, for details.

When changing the INTRC internal oscillator speed, there is a brief period of time when the processor is inactive. When the speed changes from fast to slow, the processor inactive period is in the range of 100 μS to 300 μS. For a speed change from slow to fast, the processor is inactive between 1.25 μS and 3.25 μS, nominal.

14.2.7 CLKOUT

In the INTRC and RC modes, the PIC16C781/782 can be configured to provide a clock out signal by programming the configuration word. The oscillator frequency, divided by 4, can be used for test purposes or to synchronize other logic.

In the INTRC and RC modes, if the CLKOUT output is enabled, CLKOUT is held low during RESET.

14.3 RESET

The PIC16C781/782 devices have several different RESETS. These RESETS are grouped into two classifications: power-up and non power-up. The power-up type RESETS are the Power-on and Brown-out Resets, which assume the device VDD was below its normal operating range for the device's configuration. The non power-up type RESETS assume normal operating limits were maintained before/during and after the RESET.

- Power-on Reset (POR)
- Programmable Brown-out Reset (PBOR)
- Non Power-up ($\overline{MCLR}$) Reset during normal operation
- $\overline{MCLR}$ Reset during SLEEP
- WDT Reset (during normal operation)

Some registers are not affected in any RESET condition. Their status is unknown on a Power-up Reset and unchanged in any other RESET. Most other registers are placed into an initialized state upon RESET. However, they are not affected by a WDT Reset during SLEEP, because this is considered a WDT Wake-up, which is viewed as the resumption of normal operation.

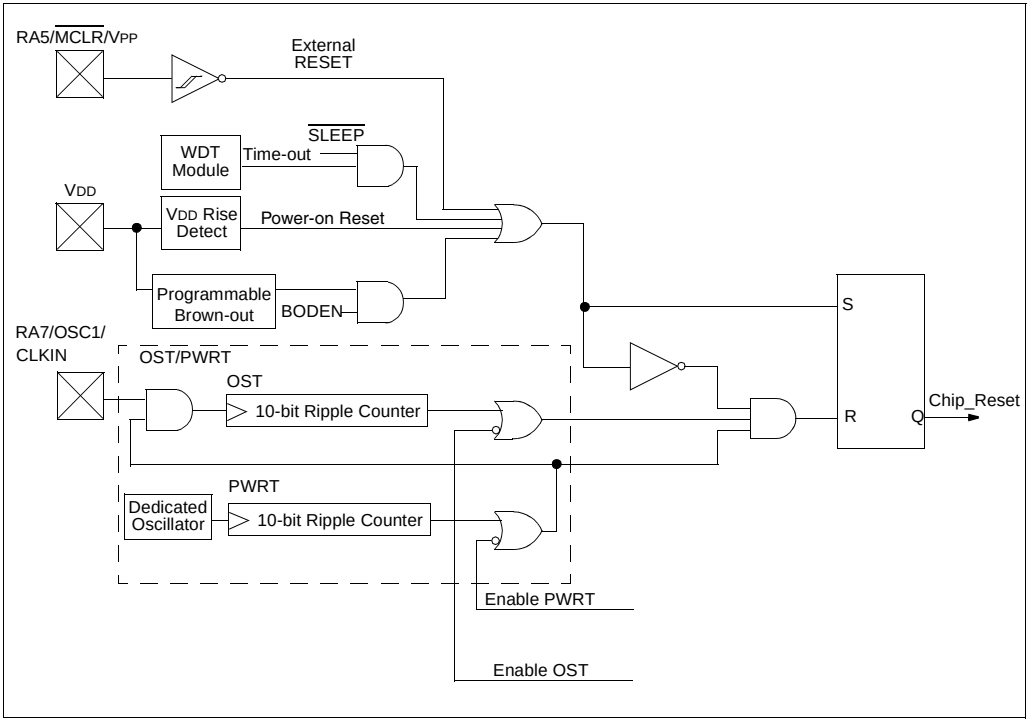
Several status bits have been provided to indicate which RESET occurred (see Table 14-4). See Table 14-5 for a full description of RESET states of special registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 14-4.

These devices have a $\overline{MCLR}$ noise filter in the $\overline{MCLR}$ Reset path. The filter detects and ignores small pulses.

It should be noted that a WDT Reset does not drive $\overline{MCLR}$ pin low.

FIGURE 14-4: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



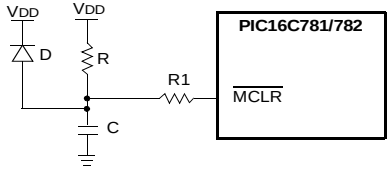
14.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when a VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, simply enable the internal MCLR feature. This eliminates external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Section 17.0 for details. For a slow rise time, see Figure 14-5.

Two delay timers (PWRT on OST) are provided, which hold the device in RESET after a POR (dependent upon device configuration), so that all operational parameters have been met prior to releasing the device to resume/begin normal operation.

When the device starts normal operation (exits the RESET condition), device operating parameters (i.e., voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met. Brown-out Reset may be used to meet the start-up conditions, or if necessary an external POR circuit may be implemented to delay end of RESET for as long as needed.

FIGURE 14-5: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD RAMP)



Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

14.5 Power-up Timer (PWRT)

The Power-up Timer provides a fixed TPWRT time-out on power-up type RESETS only. For a POR, the PWRT is invoked when the POR pulse is generated. For a BOR, the PWRT is invoked when the device exits the RESET condition (VDD rises above BOR trip point). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. The PWRT's time delay is designed to allow VDD to rise to an acceptable level. A configuration bit (PWRT) is provided to enable/disable the PWRT for the POR only. For a BOR the PWRT is always available regardless of the configuration bit setting.

The power-up time delay varies from chip-to-chip due to VDD, temperature and process variation. See DC parameters for details.

14.6 Programmable Brown-out Reset (PBOR)

The Programmable Brown-out Reset module is used to generate a RESET when the supply voltage falls below a specified trip voltage. The trip voltage is configurable to any one of four voltages provided by the BORV<1:0> configuration word bits.

Configuration bit BODEN can disable (if clear/programmed), or enable (if set), the Brown-out Reset circuitry. If VDD falls below the specified trip point for longer than TBOR (see Parameter 35, Section 17.0, Table 17-6), the brown-out situation resets the chip. A RESET may not occur if VDD falls below the trip point for less than TBOR. The chip remains in Brown-out Reset until VDD rises above VBOR. The Power-up Timer is invoked at that point and keeps the chip in RESET an additional TPWRT. If VDD drops below VBOR while the Power-up Timer is running, the chip goes back into a Brown-out Reset and the Power-up Timer is re-initialized. Once VDD rises above VBOR, the Power-up Timer again begins a TPWRT time delay.

14.7 Time-out Sequence

On power-up, the time-out sequence is as follows: First, PWRT time-out is invoked by the POR pulse. When the PWRT delay expires, the Oscillator Start-up Timer is activated. The total time-out varies depending on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there is no time-out at all. Figure 14-6, and Figure 14-9 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs expire. Then, bringing MCLR high begins execution immediately. This is useful for testing purposes or to synchronize more than one PIC microcontroller operating in parallel.

Table 14-5 shows the RESET conditions for some special function registers.

14.8 Power Control/Status Register (PCON)

The Power Control/Status Register, PCON, has two status bits that provide indication of which power-up type RESET occurred.

PCON<0> is Brown-out Reset Status bit, $\overline{BOR}$. Bit $\overline{BOR}$ is set on a Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if bit $\overline{BOR}$ cleared, indicating a BOR occurred. However, if the brown-out circuitry is disabled, the $\overline{BOR}$ bit is a "Don't Care" bit and is considered unknown upon a POR.

PCON<1> is $\overline{POR}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

When the CPU is running under the INTRC oscillator mode, the frequency of the INTRC oscillator can be switched to a power saving 37 kHz (nominal) mode. Clearing the OSCF (PCON<3>) enables oscillation at 37kHz, setting OSCF returns the oscillator to operation at 4MHz.

The Watchdog Timer is a free running, on-chip dedicated oscillator and timer, which does not require any external components to operate. The WDT provides a system RESET in the event that software does not execute a `CLRWDT` instruction within a specified interval. For reliability, the WDT will run even if the CPU clock has been stopped (for example, by the execution of a `SLEEP` instruction).

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to awaken and resume normal operation (Watchdog Timer Wake-up).

The WDT can be enabled either by setting the WDTE bit in the configuration register during programming, or by setting the WDTON bit (PCON<4>).

TABLE 14-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out	Wake-up from SLEEP
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1		
XT, HS, LP	TPWRT + 1024TOSC	1024TOSC	TPWRT + 1024TOSC	1024TOSC
EC, RC, INTRC	TPWRT	—	TPWRT	—

REGISTER 14-2: POWER CONTROL REGISTER (PCON: 8Eh)

U-0	U-0	U-0	R/W-q	R/W-1	U-0	R/W-q	R/W-x
—	—	—	WDTON	OSCF	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **WDTON:** WDT Software Enable bit

If WDTE bit (Configuration Word <3>) = 1:
This bit is not writable, always reads '1'

If WDTE bit (Configuration Word <3>) = 0:
1 = WDT is enabled
0 = WDT is disabled and cleared

bit 3 **OSCF:** Oscillator Speed bit (pending on new internal oscillator decision)

INTRC mode:
1 = 4 MHz typical
0 = 37 kHz typical

All other oscillator modes:
Ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit

1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit

1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
x = Bit is unknown	'q' = Value depends on condition	

TABLE 14-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Bit Significance
0	1	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	x	x	0	Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
1	1	1	0	$\overline{\text{MCLR}}$ Reset during SLEEP or interrupt wake-up from SLEEP

TABLE 14-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---0 1-01
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---0 1-uu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu	---0 1-uu
WDT Reset	000h	0000 1uuu	---0 1-uu
WDT Wake-up	PC + 1	uuu0 0uuu	---0 u-uu
Brown-out Reset	000h	0001 1uuu	---0 1-u0
Interrupt wake-up from SLEEP, GIE = 0	PC + 1	uuu1 0uuu	---u u-uu
Interrupt wake-up from SLEEP, GIE = 1	0004h	uuu1 0uuu	---u u-uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'.

FIGURE 14-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD)

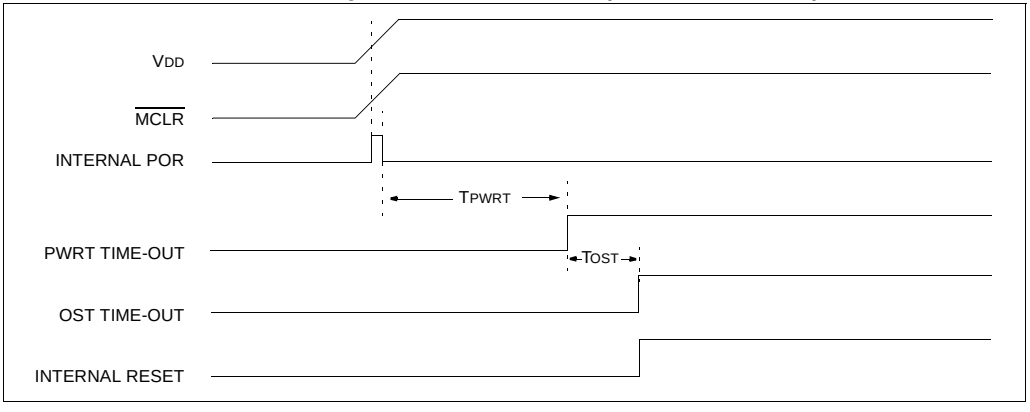


FIGURE 14-7: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD)

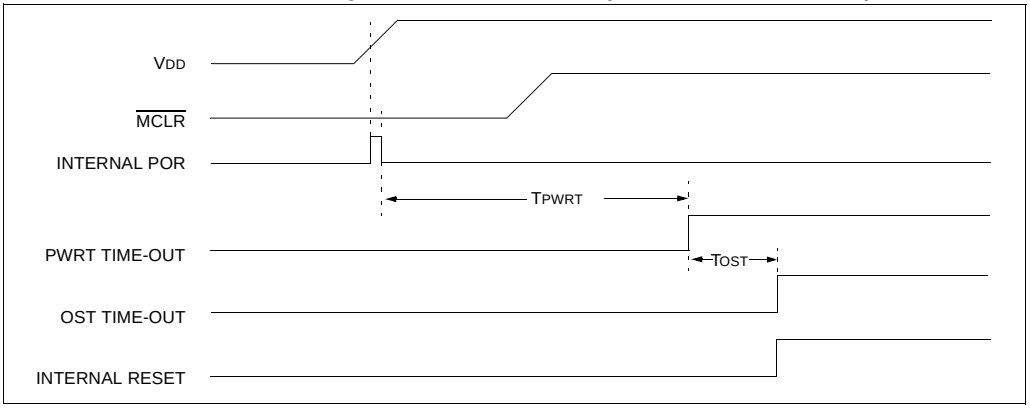


TABLE 14-6: INITIALIZATION CONDITION FOR ALL REGISTERS

Register	Power-On Reset or Brown-Out Reset	$\overline{\text{MCLR}}$ Reset or WDT Reset	Wake-up via WDT or Interrupt
W (not a mapped register)	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	0000 0000	uuuu uuuu	uuuu uuuu
TMR0	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	PC + 1(1)
STATUS	0001 1xxx	000q quuu(2)	uuuq quuu(2)
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	xxxx 0000	uuuu 0000	uuuu uuuu
PORTB	xxxx xx00	uuuu uu00	uuuu uu00
PCLATH	---0 0000	---0 0000	---u uuuu
INTCON	0000 000x	0000 000u	uuuu uuqq
PIR1	0000 ---0	0000 ---0	0000 ---u
CALCON	000- ----	000- ----	uuu- ----
TMR1L	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	-000 0000	-uuu uuuu	-uuu uuuu
PSMCCON0	0000 0000	0000 0000	uuuu uuuu
PSMCCON1	000- 0000	000- 0000	uuu- uuuu
CM1CON0	0000 0000	0000 0000	uuuu uuuu
CM2CON0	0000 0000	0000 0000	uuuu uuuu
CM2CON1	00-- ---0	00-- ---0	uu-- ---u
OPACON	00-- ---0	00-- ---0	uu-- ---u
ADRES	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	0000 0000	0000 0000	uuuu uuuu
OPTION_REG	1111 1111	1111 1111	uuuu uuuu
TRISA	1111 1111	1111 1111	uuuu uuuu
TRISB	1111 1111	1111 1111	uuuu uuuu
PIE1	0000 ---0	0000 ---0	uuuu ---u
PCON	---0 1-qq	---0 1-uu	---u u-uu
DAC	0000 0000	0000 0000	uuuu uuuu
DACON0	00-- --00	00-- --00	uu-- --uu
WPUB	1111 1111	1111 1111	uuuu uuuu
IOCB	1111 0000	1111 0000	uuuu uuuu
REFCON	---- 00--	---- 00--	---- uu--
LVDCON	--00 0101	--00 0101	--uu uuuu
ANSEL	1111 1111	1111 1111	uuuu uuuu
ADCON1	--00 ----	--00 ----	--uu ----
PMDATL	xxxx xxxx	uuuu uuuu	uuuu uuuu
PMADRL	xxxx xxxx	uuuu uuuu	uuuu uuuu
PMDATH	--xx xxxx	--uu uuuu	--uu uuuu
PMADRH	---- xxxx	---- uuuu	---- uuuu
PMCON1	1--- ---0	1--- ---0	1--- ---0

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

2: See Table 14-5 for RESET value for specific condition.

FIGURE 14-8: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD})

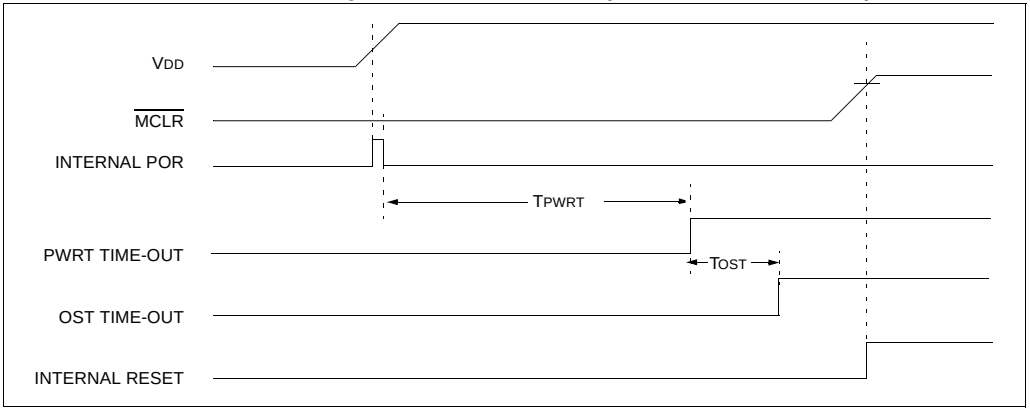
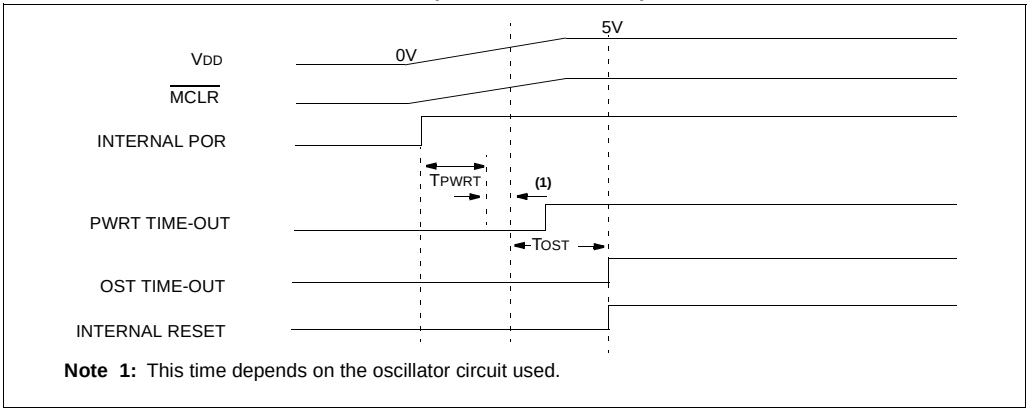


FIGURE 14-9: SLOW V_{DD} RISE TIME ($\overline{MCLR}$ TIED TO V_{DD})



Note 1: This time depends on the oscillator circuit used.

14.9 Interrupts

The devices have up to eight sources of interrupt. The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

A global interrupt enable bit, GIE (INTCON<7>), enables (if set) all unmasked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set, regardless of the status of the GIE bit. The GIE bit is cleared on RESET.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT/AN4/VR pin interrupt, the RB port Interrupt-on-Change (IOCB) and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the special function register PIR1. The corresponding interrupt enable bits are contained in special function register PIE1, and the peripheral interrupt enable bit is contained in special function register INTCON.

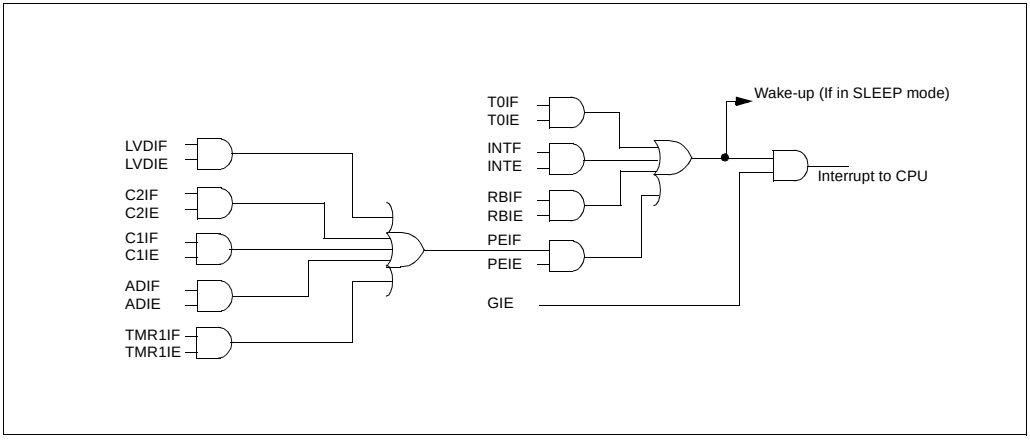
When an interrupt is serviced, the GIE bit is cleared to disable any further interrupt. The return address is pushed onto the stack and the PC is loaded with 0004h. Once in the Interrupt Service Routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency is three or four instruction cycles. The exact latency depends on when the interrupt event occurs. The latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

14.9.1 INT INTERRUPT

External interrupt on RB0/INT/AN4/VR pin is edge triggered: either rising, if bit INTEDG (OPTION_REG<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The INT interrupt can awaken the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following a wake-up sequence. See Section 14.12 for details on SLEEP mode.

FIGURE 14-10: INTERRUPT LOGIC



14.9.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register sets the flag bit, T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit, T0IE (INTCON<5>) (Section 2.5).

14.9.3 PORTB INTERRUPT-ON-CHANGE (IOCB)

An input change on PORTB<7:0> sets flag bit RBIF (INTCON<0>). The PORTB pin(s) which can individually generate interrupt are selectable in the IOCB register. The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>) (Section 2.5). PORTB must be configured as a digital input.

14.10 Context Saving During Interrupts

During an interrupt, only the PC is saved on the stack. At minimum, W and STATUS should be saved to preserve the context for the interrupted program. All registers that may be corrupted by the Interrupt Service Routine (ISR), such as PCLATH or FSR, should be saved.

Example 14-1 stores and restores the STATUS, W and PCLATH registers. The register, W_TEMP, is defined in Common RAM, the last 16 bytes of each bank that may be accessed from any bank. The STATUS_TEMP and PCLATH_TEMP are defined in bank 0.

The example:

a) Stores the W register.
b) Stores the STATUS register in bank 0.
c) Stores the PCLATH register in bank 0.
d) Executes the ISR code.
e) Restores the PCLATH register.
f) Restores the STATUS register.
g) Restores W.

Note:	The W_TEMP, STATUS_TEMP and PCLATH_TEMP are defined in the common RAM area (70h - 7Fh) to avoid register bank switching during context save and restore.

EXAMPLE 14-1: SAVING STATUS, W, AND PCLATH REGISTERS

```
#define    W_TEMP          0x70
#define    STATUS_TEMP     0x71
#define    PCLATH_TEMP     0x72
    org    0x04            ; Int Vector
    MOVWF   W_TEMP         ; Save W
    MOVF   STATUS,w
    MOVWF  STATUS_TEMP     ; save STATUS
    MOVF   PCLATH,w
    MOVWF  PCLATH_TEMP     ; save PCLATH
    :
    (Interrupt Service Routine)
    :
    MOVF   PCLATH_TEMP,w
    MOVWF  PCLATH
    MOVF   STATUS_TEMP,w
    MOVWF  STATUS
    SWAPF  W_TEMP,f        ; swapf loads W
    SWAPF  W_TEMP,w        ; w/o affect STATUS
    RETFIE
```

14.11 Watchdog Timer (WDT)

The Watchdog Timer uses a free running, on-chip RC oscillator, which does not require any external components. This oscillator is independent from the processor clock. The WDT runs even if the main clock of the device has been stopped (for example, by execution of a SLEEP instruction).

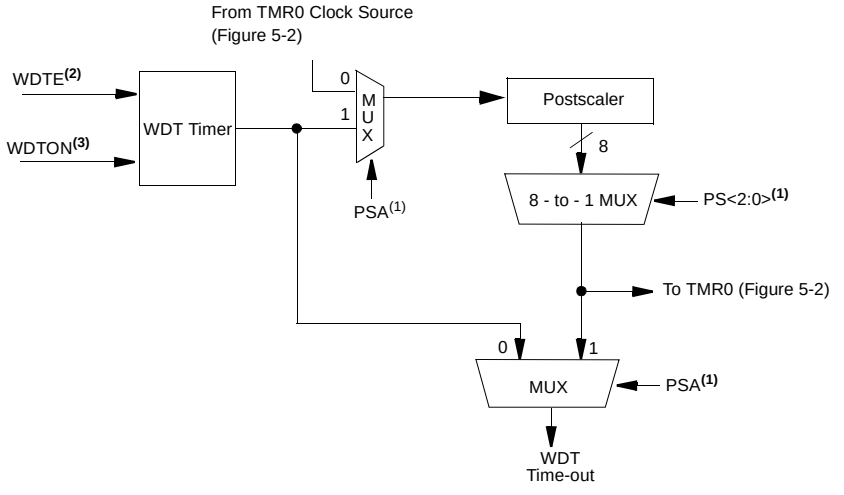
During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The $\overline{TO}$ bit in the STATUS register is cleared upon a Watchdog Timer time-out.

The WDT can be permanently enabled by programming the configuration bit WDTE, or by software via the WDTON bit in the Power Control register (PCON: 8EH). See Section 14.8 and Section 14.1.

WDT time-out period values may be found in the Electrical Specifications. Values for the WDT prescaler may be assigned using the OPTION_REG register.

Note 1:	The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT.
2:	When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count is cleared, but the prescaler assignment is not changed.

FIGURE 14-11: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: PSA and PS<2:0> are bits in the OPTION_REG register.
2: WDTE bit in the configuration word.
3: WDTON bit in the PCON register.

TABLE 14-7: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. Bits(1)	—	BODEN	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0
81h,181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
8Eh	PCON	—	—	—	WDTON	OCSF	—	$\overline{BOR}$	$\overline{POR}$

Legend: Shaded cells are not used by the Watchdog Timer.
Note 1: See Register 14-1 for the full description of the Configuration Word bits.

14.12 Power-down Mode (SLEEP)

Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer is cleared but keeps running, the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode:

- place all I/O pins at either V_{DD}, or V_{SS},
- ensure no external circuitry is drawing current from the I/O pin,
- power-down all peripherals,
- disable external clocks.

Pull all I/O pins that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at V_{DD} or V_{SS} for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

14.12.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. External RESET input on $\overline{MCLR}$ pin.
2. Watchdog Timer Wake-up (if WDT was enabled).
3. Interrupt from INT pin, PORTB IOCB, or any Peripheral Interrupts.

External $\overline{MCLR}$ Reset causes a device RESET. All other events are considered a continuation of program execution and cause a "wake-up". The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device RESET. The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. ADC conversion (when ADC clock source is RC).
3. Programmable low voltage detect.
4. Comparator C1 or C2 interrupt-on-change.
5. OPA in Comparator mode using IOCB.

Other peripherals cannot generate interrupts since during SLEEP, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

14.12.2 WAKE-UP USING INTERRUPTS

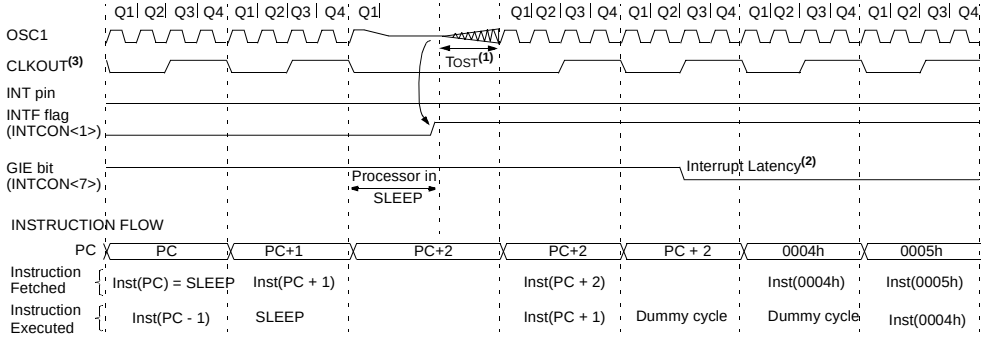
When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction completes as a NOP. Therefore, the WDT and WDT postscaler are not cleared, the $\overline{TO}$ bit is not set, and $\overline{PD}$ bits are not cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device immediately awakens from SLEEP. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler are cleared, the $\overline{TO}$ bit is set, and the $\overline{PD}$ bit is cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

FIGURE 14-12: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: TOST = 1024TOSC (drawing not to scale). This delay applies to LP, XT and HS modes only.
2: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
3: CLKOUT is not available in these osc modes, but shown here for timing reference.

15.0 INSTRUCTION SET SUMMARY

Each PIC16CXXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXXX instruction set summary in Table 15-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 15-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 15-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 15-2 lists the instructions recognized by the MPASM™ assembler.

Figure 15-1 shows the general formats that the instructions can have.

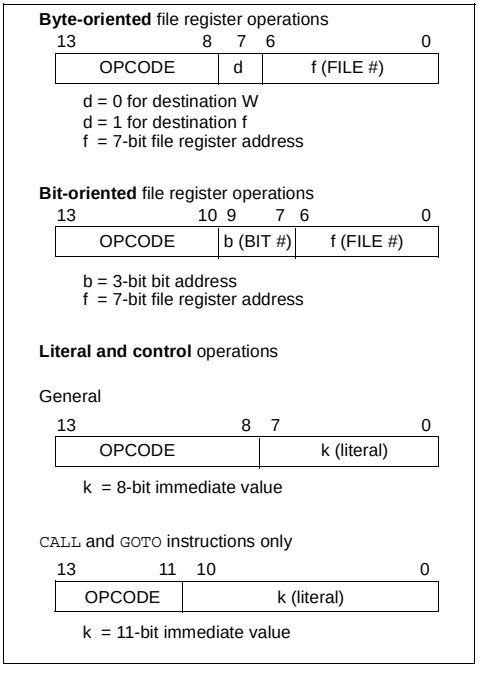
Note: To maintain upward compatibility with future PIC16CXXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 15-1: GENERAL FORMAT FOR INSTRUCTIONS



A description of each instruction is available in the PIC Mid-Range Reference Manual, (DS33023).

TABLE 15-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00 0101 dfff ffff	Z	1,2
CLRF	f	Clear f	1	00 0001 lfff ffff	Z	2
CLRW	-	Clear W	1	00 0001 0000 0011	Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff	Z	1,2
DECF	f, d	Decrement f	1	00 0011 dfff ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff		1,2,3
INCF	f, d	Increment f	1	00 1010 dfff ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00 1111 dfff ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00 0100 dfff ffff	Z	1,2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	1,2
MOVWF	f	Move W to f	1	00 0000 lfff ffff		
NOP	-	No Operation	1	00 0000 0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00 1101 dfff ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00 1100 dfff ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00 1110 dfff ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff		1,2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k	Add literal and W	1	11 111x kkkk kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11 1001 kkkk kkkk	Z	
CALL	k	Call subroutine	2	10 0kkk kkkk kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00 0000 0110 0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10 1kkk kkkk kkkk		
IORLW	k	Inclusive OR literal with W	1	11 1000 kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11 00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00 0000 0000 1001		
RETLW	k	Return with literal in W	2	11 01xx kkkk kkkk		
RETURN	-	Return from Subroutine	2	00 0000 0000 1000		
SLEEP	-	Go into standby mode	1	00 0000 0110 0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11 110x kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11 1010 kkkk kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

15.1 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[*label*] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

ANDLW	AND Literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	$0 \le f \le 127$ $0 \le b < 7$
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2TCY instruction.

BTFSC	Bit Test, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2TCY instruction.

CALL	Call Subroutine
Syntax:	[*label*] CALL k
Operands:	0 ≤ k ≤ 2047
Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>
Status Affected:	None
Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

CLRF	Clear f
Syntax:	[*label*] CLRF f
Operands:	0 ≤ f ≤ 127
Operation:	00h → (f) 1 → Z
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

CLRW	Clear W
Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W) 1 → Z
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

CLRWDT	Clear Watchdog Timer
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT 0 → WDT prescaler, 1 → $\overline{TO}$ 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

COMF	Complement f
Syntax:	[*label*] COMF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	($\bar{f}$) → (destination)
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

DECF	Decrement f
Syntax:	[*label*] DECF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) - 1 → (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 → (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, then a NOP is executed instead, making it a 2TCY instruction.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	$0 \le k \le 2047$
Operation:	k → PC<10:0> PCLATH<4:3> → PC<12:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 → (destination)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 → (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead, making it a 2TCY instruction.

IORLW	Inclusive OR Literal with W
Syntax:	[*label*] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .OR. (f) → (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) → (destination)
Status Affected:	Z
Description:	The contents of register f are moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register, since status flag Z is affected.

MOVLW	Move Literal to W
Syntax:	[*label*] MOVLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W)
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	0 ≤ f ≤ 127
Operation:	(W) → (f)
Status Affected:	None
Description:	Move data from W register to register 'f'.

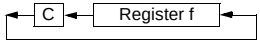
NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None

RETLW	Return with Literal in W
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RETURN	Return from Subroutine
Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

RLF	Rotate Left f through Carry
Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.



RRF **Rotate Right f through Carry**

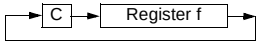
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped.

SUBLW **Subtract W from Literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.

XORLW **Exclusive OR Literal with W**

Syntax: [*label*]

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Description: The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

16.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELOQ® Demonstration Board

16.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or ‘C’)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

16.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

16.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI ‘C’ compilers for Microchip’s PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

16.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

16.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

16.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

16.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

16.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC MCUs and can be used to develop for this and other PIC microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

16.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable V_{DD} and V_{PP} supplies, which allow it to verify programmed memory at V_{DD} min and V_{DD} max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC devices. It can also set code protection in this mode.

16.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

16.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

16.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I^2C™ bus and separate headers for connection to an LCD module and a keypad.

16.13 PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

16.14 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

16.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters.

TABLE 16-1: DEVELOPMENT TOOLS FROM MICROCHIP

		PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16C9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	PIC18FXXX	24CXX/ 25CXX/ 93CXX	HCSXXX	MCRFXXX	MCP2510
Software Tools	MPLAB® Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	MPLAB® C17 C Compiler												✓	✓						
	MPLAB® C18 C Compiler														✓	✓				
	MPASM™ Assembler/ MPLINK™ Object Linker	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Emulators	MPLAB® ICE In-Circuit Emulator	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	ICEPIC™ In-Circuit Emulator	✓		✓	✓	✓		✓	✓	✓		✓								
Debugger	MPLAB® ICD In-Circuit Debugger				✓*			✓*			✓					✓				
Programmers	PICSTART® Plus Entry Level Development Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	PRO MATE® II Universal Device Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Demo Boards and Eval Kits	PICDEM™ 1 Demonstration Board			✓		✓		✓†		✓			✓							
	PICDEM™ 2 Demonstration Board				✓†			✓†							✓	✓				
	PICDEM™ 3 Demonstration Board											✓								
	PICDEM™ 14A Demonstration Board		✓																	
	PICDEM™ 17 Demonstration Board													✓						
	KEELOQ® Evaluation Kit																	✓		
	KEELOQ® Transponder Kit																	✓		
	microID™ Programmer's Kit																		✓	
	125 kHz microID™ Developer's Kit																		✓	
	125 kHz Anticollision microID™ Developer's Kit																		✓	
	13.56 MHz Anticollision microID™ Developer's Kit																		✓	
	MCP2510 CAN Developer's Kit																			✓

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

NOTES:

17.0 ELECTRICAL CHARACTERISTICS

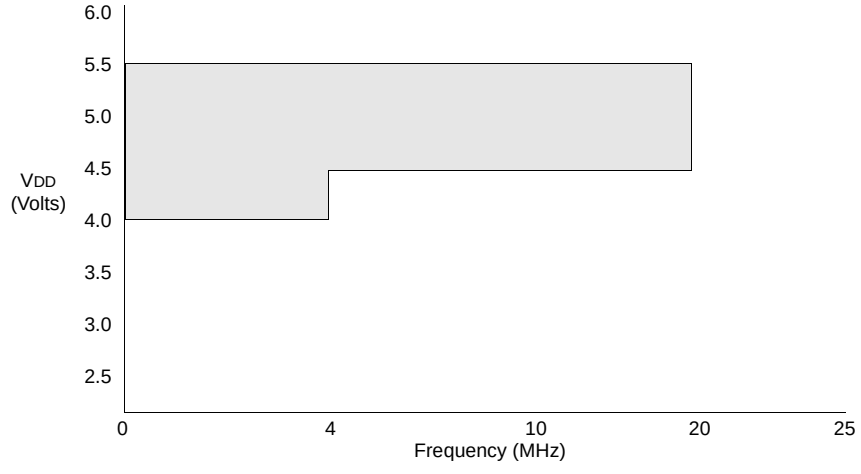
Absolute Maximum Ratings †

Ambient temperature under bias ..... -55°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD}, $\overline{MCLR}$ and RA4) ..... -0.3V to (V_{DD} + 0.3 V)
Voltage on V_{DD} with respect to V_{SS} ..... -0.3 to +7.5 V
Maximum voltage between AV_{DD} and V_{DD} pins ..... ± 0.3 V
Maximum voltage between AV_{SS} and V_{SS} pins ..... ± 0.3 V
Voltage on $\overline{MCLR}$ with respect to V_{SS} ..... -0.3 V to +8.5 V
Voltage on RA4 with respect to Vss ..... 0.3 V to +10.5 V
Total power dissipation(1) (PDIP, SOIC) ..... 1.0 W
Total power dissipation(1) (SSOP) ..... 0.65 W
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin ..... 250 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD} ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD} ..... ± 20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by PORTA and PORTB (combined) ..... 200 mA
Maximum current sourced by PORTA and PORTB (combined ..... 200 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$.

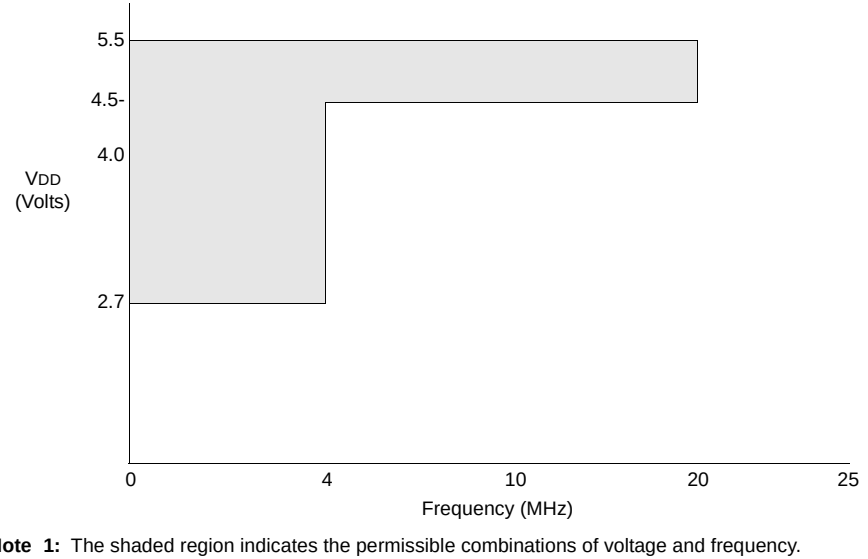
† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 17-1: PIC16C781/782 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 17-2: PIC16LC781/782 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

17.1 DC Characteristics: Power Supply

TABLE 17-1: DC CHARACTERISTICS: PIC16C781/782, DSTEMP (INDUSTRIAL)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature-40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	4.0 4.5	— —	5.5 5.5	V —	XT, EC, RC, INTRC Oscillator HS Oscillator
D001A	VDD	**Supply Voltage** (DSTEMP)	2.7 4.5	— —	5.5 5.5	V V	XT, EC, RC, INTRC Oscillator HS Oscillator
D002*	VDR	**RAM Data Retention Voltage(1)**	—	1.5	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	TBD	—	V	See section on Power-on Reset for details
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details. PWRT enabled
D010	IDD	**Supply Current(2)**	— — — —	TBD TBD TBD TBD	TBD TBD TBD TBD	mA mA mA mA	FOSC = 20 MHz, VDD = 5.5V* HS Oscillator FOSC = 20 MHz, VDD = 4.5V HS Oscillator FOSC = 4 MHz, VDD = 4.0V* XT, RC w/CLKOUT FOSC = 32 kHz, VDD = 4.0V LP Oscillator
D020 D020A	IPD	**Power-down Current(3)**	— —	TBD 1.5	TBD 19	µA µA	VDD = 5.5V VDD = 4.0V
	IOPA	**Operational Amplifier**	—	TBD TBD	TBD TBD	mA mA	VDD = 5.0V, GBWP = 0 VDD = 5.0V, GBWP = 1
	IVC*	**Voltage Comparators C1 and C2**	— —	TBD TBD	TBD TBD	mA mA	VDD = 5.0V, VID>100 mV C1SP = 0 VDD = 5.0 , VID>100 mV C1SP = 1
	IADC*	**Digital to Analog Converter (DAC)**	—	TBD	TBD	mA	VDD = 5.0V
D021	IWDT*	**Watchdog Timer**	—	TBD	TBD	mA	VDD = 4.0V
D026	IAD*	**Analog-to-Digital Converter (ADC)**	—	TBD	TBD	mA	VDD = 5.5V, ADC not converting
	IPLVD*	**Programmable Low Voltage Detect**		TBD	TBD	mA	VDD = 4.0V
	IPBOR*	**Programmable Brown-out Reset**		TBD	TBD	mA	VDD = 5.0V
1A	FOSC	**LP Oscillator, Operating Freq.** **INTRC Oscillator Operating Freq.** **XT Oscillator Operating Freq.** **HS Oscillator Operating Freq.**	9 — — 0 0	— 4 37 — —	200 — — 4 20	kHz MHz kHz MHz MHz	All temperatures All temperatures, OSCF = 1 All temperatures, OSCF = 0 All temperatures All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins configured as inputs, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins configured as iputs and tied to VDD or VSS.

17.2 DC Characteristics: Input/Output Pins

TABLE 17-2: DC CHARACTERISTICS: PIC16C781/782, DSTEMP (INDUSTRIAL)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and Operating voltage VDD range as described in DC spec Section 17-1				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Input Low Voltage					
	VIL	I/O ports:					
D030		with TTL buffer	VSS	—	0.15VDD	V	For entire VDD range
D030A			VSS	—	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	For entire VDD range
D032		$\overline{MCLR}$	VSS	—	0.2VDD	V	
D033		OSC1 (in XT, HS, LP and EC)	VSS	—	0.3 VD	V	
		Input High Voltage					
	VIH	I/O ports:		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			(0.25VDD + 0.8V)	—	VDD	V	For entire VDD range
D041		with Schmitt Trigger buffer	0.8VDD	—	VDD	V	For entire VDD range
D042		$\overline{MCLR}$	0.8VDD	—	VDD	V	
D042A		OSC1 (XT, HS, LP and EC)	0.7VDD	—	VDD	V	
D070	IPURB	**PORTB Weak Pull-up Current Per Pin**	50	250	400	µA	VDD = 5V, VPIN = VSS
		Input Leakage Current(1,2)					
D060	IIL	I/O ports (with digital functions)	—	—	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D060A	IIL	I/O ports (with analog functions)	—	—	±100	nA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		RA5/$\overline{MCLR}$/VPP	—	—	±5	µA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS, LP and EC osc configuration
		Output Low Voltage					
D080	VOL	I/O ports (Includes CLKOUT)	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
		Output High Voltage					
D090	VOH	I/O ports(2) (Includes CLKOUT)	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D150*	VOD	**Open Drain High Voltage**	—	—	10.5	V	RA4 pin
		Capacitive Loading Specs on Output Pins*					
D100	Cosc2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC mode)	—	—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

17.3 AC Characteristics: PIC16C781/782 (Industrial)

17.3.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

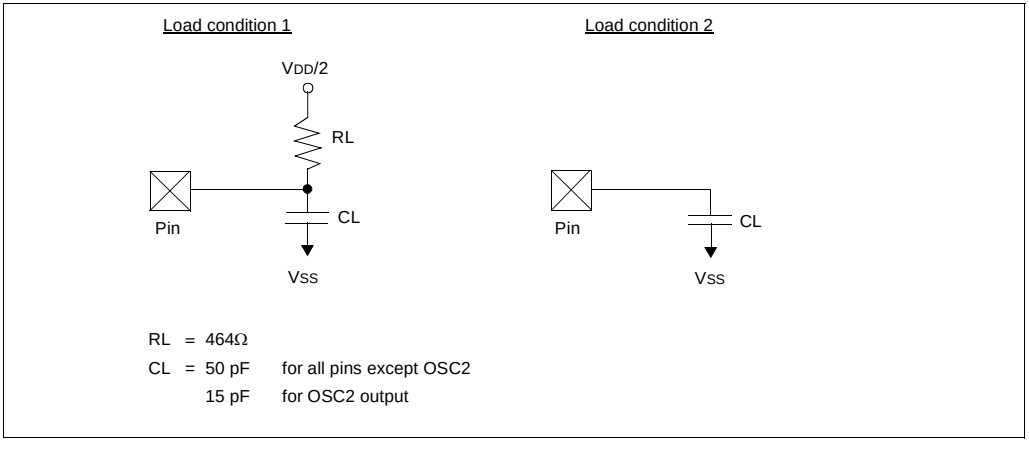
Lowercase letters (pp) and their meanings:

pp			
		osc	OSC1
ck	CLKOUT		
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{\text{MCLR}}$		

Uppercase letters and their meanings:

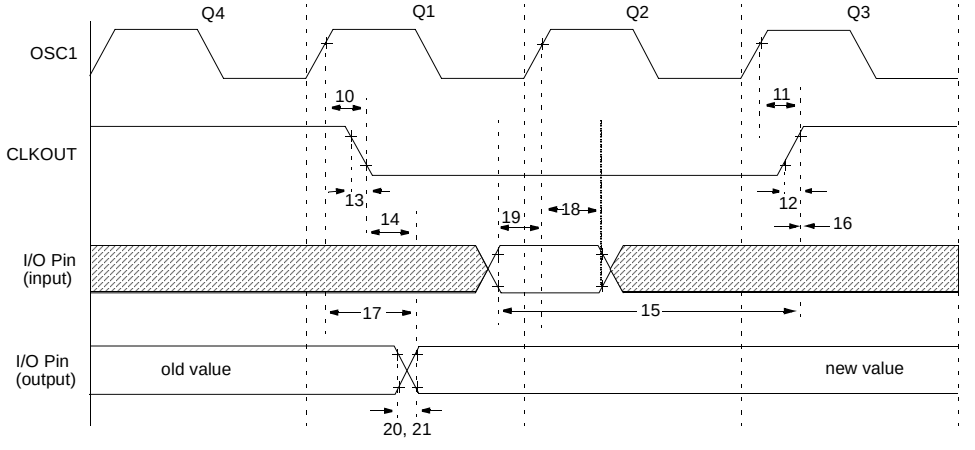
S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
		High	High
		Low	Low

FIGURE 17-3: LOAD CONDITIONS



17.3.2 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 17-4: CLKOUT AND I/O TIMING



Note 1: Refer to Figure 17-3 for load conditions.

TABLE 17-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	**(Note 1)**
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	**(Note 1)**
12*	TckR	CLKOUT rise time		—	35	100	ns	**(Note 1)**
13*	TckF	CLKOUT fall time		—	35	100	ns	**(Note 1)**
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	**(Note 1)**
15*	TioV2ckH	Port in valid before CLKOUT ↑		0.25TCY + 25	—	—	ns	**(Note 1)**
16*	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	**(Note 1)**
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16**C**781/782	100	—	—	ns	
			PIC16**LC**781/782	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16**C**781/782	—	10	25	ns	
			PIC16**LC**781/782	—	—	60	ns	
21*	TioF	Port output fall time	PIC16**C**781/782	—	10	25	ns	
			PIC16**LC**781/782	—	—	60	ns	
22††*	Tinp	INT pin high or low time		TCY	—	—	ns	
23††*	Trbp	RB7:RB0 change INT high or low time		TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

FIGURE 17-5: EXTERNAL CLOCK TIMING

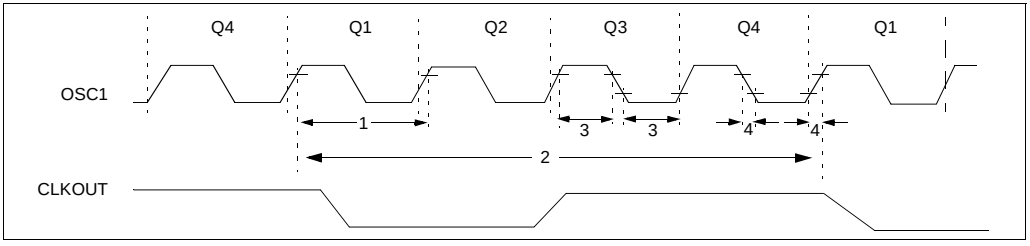


TABLE 17-4: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
1A	FOSC	External CLKIN Frequency(1)	DC	—	4	MHz	XT osc mode
			DC	—	20	MHz	EC osc mode
			DC	—	20	MHz	HS osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(1)	0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period(1)	250	—	—	ns	XT and RC osc mode
			50	—	—	ns	EC osc mode
			50	—	—	ns	HS osc mode
			5	—	—	µs	LP osc mode
		Oscillator Period(1)	250	—	10,000	ns	XT osc mode
			50	—	250	ns	HS osc mode
			5	—	—	µs	LP osc mode
2	TCY	Instruction Cycle Time(1)	200	TCY	DC	ns	TCY = 4/FOSC
3*	TOSL, TOSH	External Clock in (OSC1) High or Low Time	100	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
							EC oscillator
4*	TOSR, TOSF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator
							EC oscillator

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

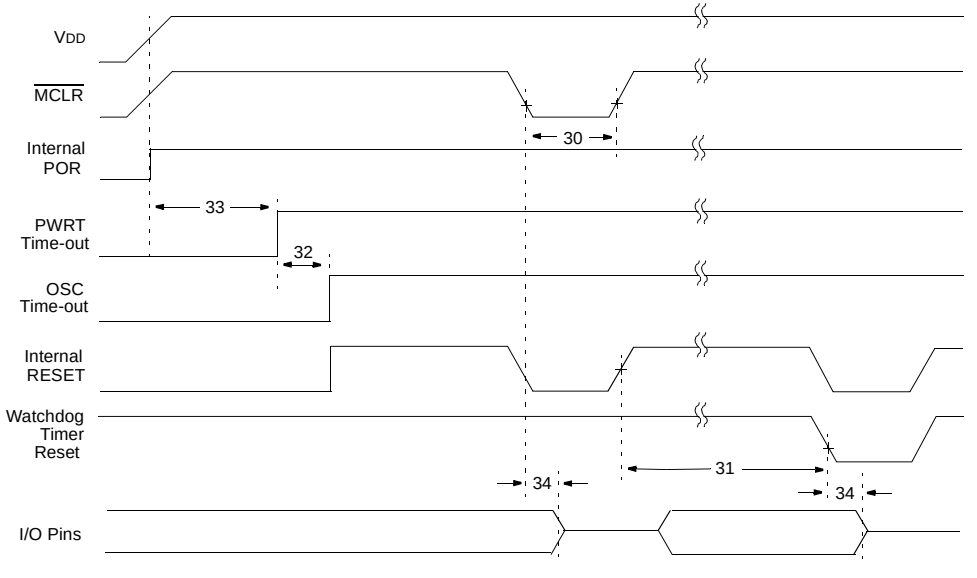
TABLE 17-5: INTERNAL RC OSCILLATOR CALIBRATED FREQUENCIES PIC16C781/782, DSTEMP

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40×C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 17-1.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
		Internal Calibrated RC Frequency	3.65	4.00	4.28	MHz	VDD = 5.0V
		Internal Calibrated RC Frequency	3.55*	4.00	4.31*	MHz	VDD = 2.5V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 17-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note 1: Refer to Figure 17-3 for load conditions.

FIGURE 17-7: BROWN-OUT RESET TIMING

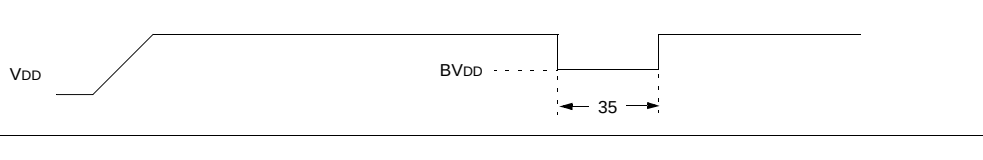


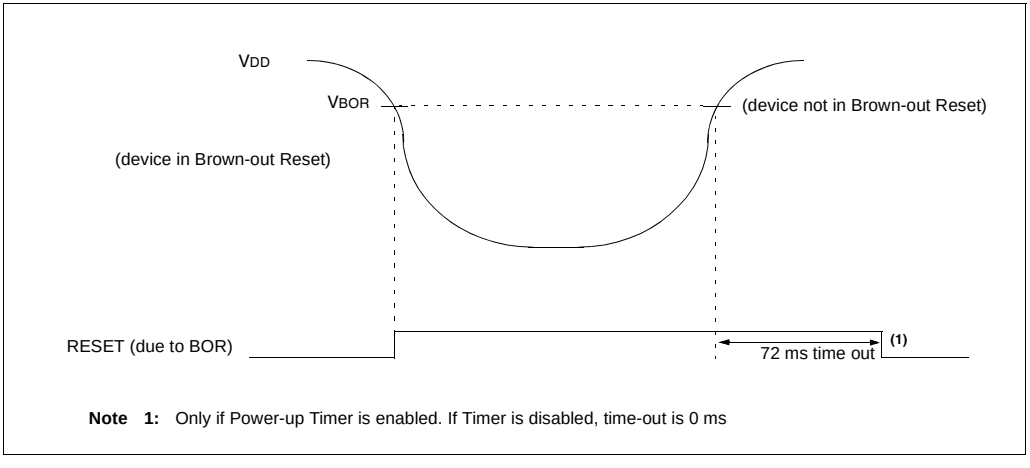
TABLE 17-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30*	TMCL	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	VDD = 5V, -40°C to +85°C
31*	TWDT	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
32*	TOST	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	TPWRT	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +85°C
34*	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.1	µs	
35*	TBOR	Brown-out Reset pulse width	100	—	—	µs	VDD ≤ VBOR (D005)

* These parameters are characterized but not tested.

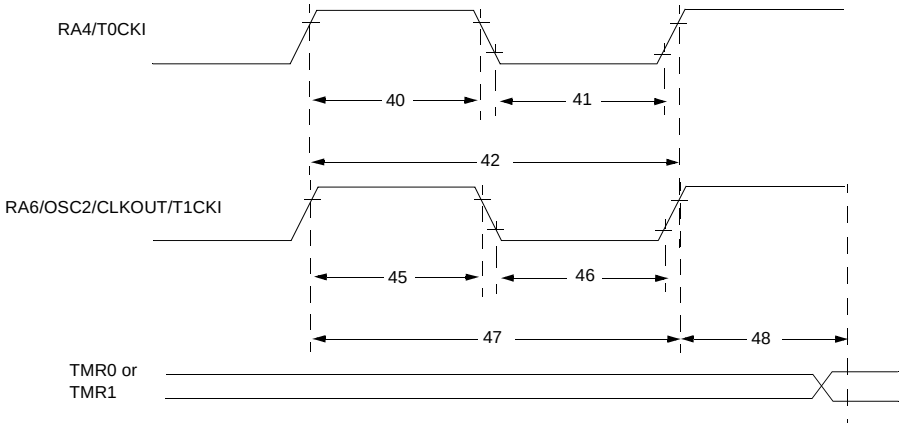
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 17-8: BROWN-OUT RESET CHARACTERISTICS



Note 1: Only if Power-up Timer is enabled. If Timer is disabled, time-out is 0 ms

FIGURE 17-9: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



Note: Refer to Figure 17-3 for load conditions.

TABLE 17-7: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	TTOH	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	Must also meet parameter 42
				With Prescaler	10	—	—	ns	
41*	TTOL	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	Must also meet parameter 42
				With Prescaler	10	—	—	ns	
42*	TTOP	T0CKI Period		No Prescaler	TCY + 40	—	—	ns	
				With Prescaler	Greater of: 20 or TCY + 40 / N	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	TT1H	T1CKI High Time	Synchronous, Prescaler = 1		0.5TCY + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16**C**781/782	15	—	—	ns	
			Asynchronous	PIC16**C**781/782	30	—	—	ns	
45*	TT1H	T1CKI High Time	Synchronous, Prescaler = 1		0.5Tcy + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16**LC**781/782	15	—	—	ns	
			Asynchronous	PIC16**LC**781/782	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, Prescaler = 1		0.5TCY + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16**C**781/782	15	—	—	ns	
			Asynchronous	PIC16**C**781/782	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, Prescaler = 1		0.5TCY + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16**LC**781/782	15	—	—	ns	
			Asynchronous	PIC16**LC**781/782	30	—	—	ns	
47*	TT1P	T1CKI input period	Synchronous	PIC16**C**781/782	Greater of: 30 OR TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	PIC16**C**781/782	60	—	—	ns	
47*	TT1P	T1CKI input period	Synchronous	PIC16**LC**781/782	Greater of: 30 OR TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	PIC16**C**781/782	60	—	—	ns	
	FT1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)			DC	—	50	kHz	
48*	Tcke2tmrl	Delay from external clock edge to timer increment			2TOSC	—	7TOSC	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

17.4 Operational Amplifier

TABLE 17-8: DC CHARACTERISTICS: OPERATIONAL AMPLIFIER (OPA)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2, and V_{OUT} ~ V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Input Offset Voltage						
	Input Offset Voltage	V_{OS}	TBD	±2	TBD	mV	Prior to Auto Calibration
	Input Offset Voltage						
	Input Offset Voltage	V_{OS}	TBD	±100	TBD	µV	Following Auto Calibration
	Input Current and Impedance						
	Input Bias Current	I_B	-50	—	+50	nA	Following Auto Calibration
	Input Offset Bias Current	I_{OS}	—	±1	—	pA	
	Common Mode						Following Auto Calibration
	Common Mode Input Range	V_{CM}	V_{SS}	—	V_{DD}-1.4	V	V_{DD} = 5 V
	Common Mode Rejection	CMR	TBD	80	—	dB	V_{CM} = V_{DD}/2, Frequency = DC
	Open Loop Gain						GBWP = 1 following Auto Calibration
	DC Open Loop Gain	A_{OL}	—	90	—	dB	R_L = 25 kΩ connected to V_{DD}/2, 50 mV < V_{OUT} < V_{DD} - 50 mV
	DC Open Loop Gain	A_{OL}	—	80	—	dB	R_L = 5 kΩ connected to V_{DD}/2, 100 mV < V_{OUT} < V_{DD} - 100 mV
	DC Open Loop Gain	A_{OL}	—	TBD	—	dB	GBWP = 0 following Auto Calibration RL = 50 kΩ connected to V_{DD}/2, 50 mV < V_{OUT} < V_{DD} - 50 mV
	DC Open Loop Gain	A_{OL}	—	TBD	—	dB	RL = 100 kΩ connected to V_{DD}/2, 50 mV < V_{OUT} < V_{DD} - 50 mV
	Output						GBWP = 1 Following Auto Calibration
	Output Voltage Swing	V_{OUT}	V_{SS}+0.1	—	V_{DD}-0.1	V	R_L = 5 kΩ connected to V_{DD}/2 V_{DD} = 5 V
	Output Short Circuit Current	I_{SC}	—	25	TBD	mA	
	Power Supply						
	Power Supply Rejection	PSR	—	80	—	dB	Following Auto Calibration
	Auto Calibration Reference	ACR	TBD	1.2	TBD	V	CALREF = 0

TABLE 17-9: AC CHARACTERISTICS: OPERATIONAL AMPLIFIER (OPA)

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, V_{SS} = GND, T_A = 25°C, VCM = V_{DD}/2, RL = 100kΩ to V_{DD}/2, and V_{OUT} = V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Gain Bandwidth Product	GBWP	—	75	—	kHz	V_{DD} = 5V, GBWP = 0
		GBWP	—	2	—	MHz	V_{DD} = 5V, GBWP = 1
	Input Offset Auto	T_Z	—	300	TBD	µs	V_{DD} = 5V, GBWP = 1
	Calibration Time	T_Z	—	TBD	TBD	µs	V_{DD} = 5V GBWP = 0
		T_{ON}	—	10	TBD	µs	V_{DD} = 5V, GWBP = 1
	Turn On Time	T_{ON}	—	TBD	TBD	µs	V_{DD} = 5V, GBWP = 0
	Phase Margin	ΘM	—	TBD	—	degrees	V_{DD} = 5V, GBWP = 0
		ΘM	—	TBD	—	degrees	V_{DD} = 5V, GBWP = 1
	Slew Rate	SR	—	TBD	—	V/µs	V_{DD} = 5V, GBWP = 0
		SR	—	TBD	—	V/µs	V_{DD} = 5V, GBWP = 1

Note: Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

17.5 Comparators

TABLE 17-10: DC CHARACTERISTICS: VOLTAGE COMPARATORS C1 AND C2

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, T_A = 25°C, V_{CM} = V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Input Offset Voltage	V_{OS}	TBD TBD	±1 ± 2.5	TBD TBD	mV mV	C1SP = 1, C2SP = 1 C1SP = 0, C2SP = 0
	Input Current and Impedance Input Bias Current Input Offset Bias Current	 I_B I_{OS}	 TBD —	 — TBD	 — TBD	 nA nA	
	Common Mode Common Mode Input Range Common Mode Rejection	 V_{CM} CMR	 V_{SS} —	 — 70	 V_{DD}-1.4V	 V dB	 V_{DD} = 5V V_{CM} = V_{DD}/2, Frequency = DC
	Open Loop Gain DC Open Loop Gain	 A_{OL}	 —	 90	 —	 dB	
	Power Supply Rejection	PSR	—	TBD	—	dB	V_{DD} = 5V

TABLE 17-11: AC CHARACTERISTICS: COMPARATORS C1 AND C2

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, T_A = 25°C, V_{CM} = V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Response Time Response Time	 t_r	 —	 75	 —	 ns	 V_{DD} = 5V, C1SP = 1, C2SP = 1, Comparator output signal is for internal use only, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
		t_r	—	0.5	—	µs	V_{DD} = 5V, C1SP = 0, C2SP = 0, Comparator output signal is for internal use only, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
		t_r	—	100	TBD	ns	V_{DD} = 5 , C_L = 100 pF, C1SP = 1, C2SP = 1, Comparator output is available on I/O pin, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
		t_r	—	0.5	TBD	µs	V_{DD} = 5 , C_L = 100 pF, C1SP = 0, C2SP = 0, Comparator output is available on I/O pin, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
	Turn On Time	T_{ON}	— —	10 TBD	TBD TBD	µs µs	C1SP = 0, C2SP = 0, V_{DD} = 5V C1SP = 1, C2SP = 1, V_{DD} = 5V

17.6 Digital-to-Analog Converter (DAC)

TABLE 17-12: DC CHARACTERISTICS: DIGITAL-TO-ANALOG CONVERTER (DAC)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, T_A = 25°C V_{DD} = 5V, DACREF = 5V Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Resolution	RES			8	bits	
	Transfer Function Accuracy Integral Non-Linearity Error Differential Non-Linearity Error Offset Error Gain Error	 $INL^{(1)}$ $DNL^{(1)}$ 	 TBD TBD TBD TBD	 .25 .10 ±2.5 .25	 TBD TBD TBD TBD	 LSb LSb mV LSb	V_{DD} = 5V, DACREF = 5V
	DACREF Input Characteristics DACREF Input Impedance DACREF Input Max Voltage	 R_{REF} V_{MAX}	 TBD TBD	 100 —	 — V_{DD}	 kΩ V	
	Output Characteristics Output Voltage Range Output Short Circuit Current Output Series Resistance	 V_{OUT} I_{SC}* R_O*	 V_{SS}+.05 V_{SS}+0.1 — — —	 — — 2 TBD	 V_{DD}-0.05 V_{DD}-0.1 TBD TBD	 V V mA Ω	 V_{DD} = 5V R_L = 100 kΩ to V_{DD}/2 V_{DD} = 5V R_L = 25 kΩ to V_{DD}/2 V_{DD} = 5V $V_{DD} \geq 3V$ $V_{DAC} = V_{DD}/2$
	Power Supply Power Supply Current	 I_{DAC}	 —	 250	 TBD	 μA	 V_{DD} = 5V

* Characterized, but not tested.

Note 1: Calculated using end point method.

TABLE 17-13: AC CHARACTERISTICS: DIGITAL-TO-ANALOG CONVERTER (DAC)

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7 V to 5.5 V, TA = 25°C Operating Temperature-40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Output Characteristics Slew Rate	 SR	 —	 1	 —	 V/μs	 V_{DD} = 5 V, C_L = 50 pF
	Settling Time	T_S	—	5	10	μs	V_{DD} = 5 V, C_L = 50 pF Settling time to 1/2 LSb for 10%FS to 90%FS step
	Turn On Time	T_{ON}	—	10	TBD	μs	V_{DD} = 5 V

Note 1: Data in 'Typ' column is at 5V, 25° C unless otherwise stated. These parameters are for design guidance only and are not tested.

17.7 Analog Peripherals Characteristics

17.7.1 BANDGAP VOLTAGE

Bandgap voltage is used as the reference voltage in the PBOR, PLVD, Auto Calibration, and VR modules

FIGURE 17-10: BANDGAP START-UP TIME

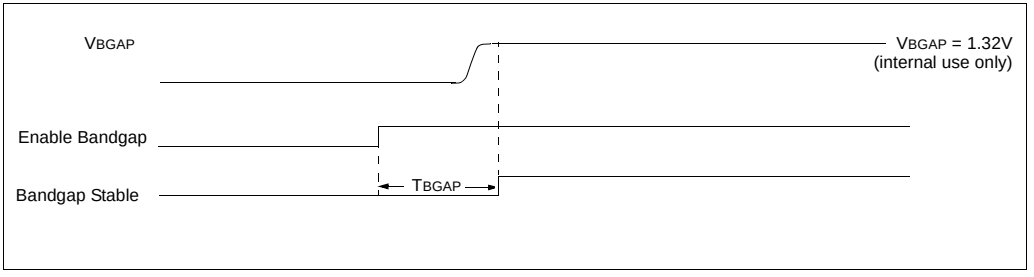


TABLE 17-14: BANDGAP START-UP TIME

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
36*	TBGAP	Bandgap start-up time	—	30	—	µs	Defined as the time between the instant that the bandgap is enabled and the moment that the bandgap reference voltage is stable.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

17.7.2 VR MODULE

TABLE 17-15: DC CHARACTERISTICS: VR

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): Operating temperature -40°C ≤ TA ≤ +85°C for industrial Operating voltage VDD as described in Section 17.1				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D400	VR	Output Voltage	—	3.072	—	V	VDD ≥ 3.5V
D402*	TCVOUT	Output Voltage Temperature Coefficient	—	TBD	TBD	ppm/°C	
D404*	IVREFSO	External Load Source	—	—	5	mA	
D405*	IVREFSI	External Load Sink	—	—	-5	mA	
	CL*	External Capacitor Load	—	—	200	pF	
D406*	DVOUT/ DIOUT	Load Regulation	—	1	TBD	mV/mA	ISOURCE = 0 mA to 5 mA
			—	1	TBD		ISINK = 0 mA to 5 mA
D407*	DVOUT/ DVDD	Supply Regulation	—	—	1	mV/V	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

17.7.3 PROGRAMMABLE LOW VOLTAGE DETECT MODULE (PLVD)

TABLE 17-16: LOW VOLTAGE DETECT CHARACTERISTICS

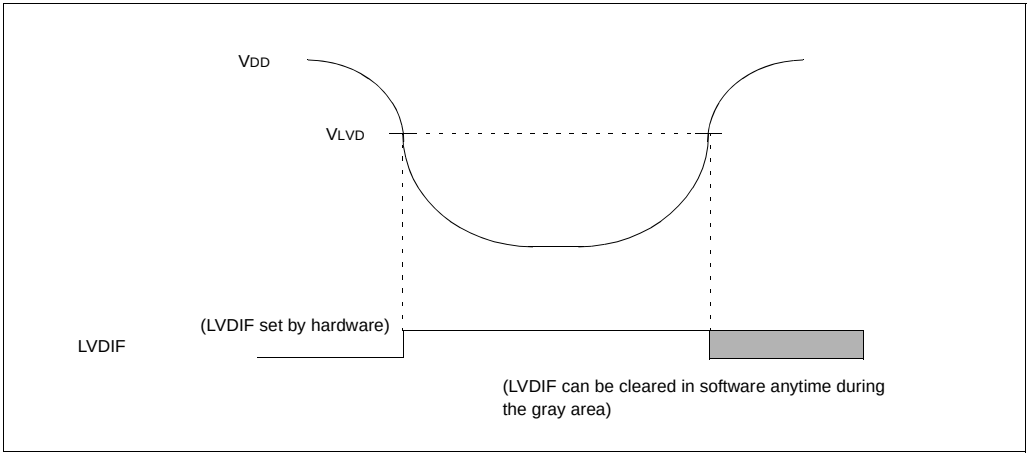


TABLE 17-17: ELECTRICAL CHARACTERISTICS: PLVD

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial Operating voltage VDD range as described in DC spec Section 17-1.					
Param No.	**Characteristic**		**Symbol**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D420*	PLVD Voltage	LV = 0100	VPLVD	2.35	—	2.80	V	—
		LV = 0101		2.55	—	3.02	V	—
		LV = 0110		2.64	—	3.14	V	—
		LV = 0111		2.83	—	3.37	V	—
		LV = 1000		3.11	—	3.71	V	—
		LV = 1001		3.29	—	3.93	V	—
		LV = 1010		3.39	—	4.04	V	—
		LV = 1011		3.58	—	4.26	V	—
		LV = 1100		3.77	—	4.49	V	—
		LV = 1101		3.95	—	4.71	V	—
		LV = 1110		4.23	—	5.05	V	—

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

17.7.4 PROGRAMMABLE BROWN-OUT RESET MODULE DC CHARACTERISTICS: PBOR

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): Operating temperature-40°C ≤ TA ≤ +85°C for Industrial Operating voltage VDD range as described in DC spec Section 17-1.					
Param No.	**Characteristic**		**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D005*	BOR Voltage	BORV<1:0> = 11	VBOR	2.35	—	2.80	V	—
		BORV<1:0> = 10		2.55	—	3.02		—
		BORV<1:0> = 01		3.95	—	4.71		—
		BORV<1:0> = 00		4.23	—	5.05		—

TABLE 17-18: ADC CONVERTER CHARACTERISTICS PIC16C781/782

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	8	bits	ADCREF = AVDD = 5.12V, VSS ≤ VAIN ≤ ADCREF
A02	EABS	Absolute Error	—	—	< ±1	LSb	ADCREF = AVDD = 5.12V, VSS ≤ VAIN ≤ ADCREF
			—	—	< ±2	LSb	ADCREF = AVDD = 3.0V(3)
A03	INL	Integral Now Linearity Error	—	—	< ±1	LSb	ADCREF = AVDD = 5.12V, VSS ≤ VAIN ≤ ADCREF
			—	—	< ±2	LSb	ADCREF = AVDD = 3.0V(3)
A04	DNL	Differential Now Linearity Error	—	—	< ±1	LSb	ADCREF = AVDD = 5.12V, VSS ≤ VAIN ≤ ADCREF
			—	—	< ±2	LSb	ADCREF = AVDD = 3.0V(3)
A05	GN	Gain Error	—	—	< ±1	LSb	ADCREF = AVDD = 5.12V, VSS≤ VAIN ≤ ADCREF
			—	—	< ±2	LSb	ADCREF = AVDD = 3.0V(3)
A06	EOFF	Offset Error	—	—	< ±1	LSb	ADCREF = AVDD = 5.12V, VSS ≤ VAIN ≤ ADCREF
			—	—	< ±2	LSb	ADCREF = AVDD = 3.0V(3)
A10	—	Monotonicity	—	guaranteed(4)	—	—	VSS ≤ VAIN ≤ ADCREF
A20	ADCREF	Reference Voltage	3.0V	—	VDD + 0.3	V	—
A25	VAIN	Analog Input Voltage	VSS - 0.3	—	ADCREF	V	—
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10.0	kΩ	—
A40	IADC	ADC Conversion Current (VDD)	—	180	—	μA	Average current consumption when ADC is on.(1)
A50	IREF	ADCREF Input Current(2)	10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD, see Section 9.3.
			—	—	40	μA	During ADC Conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

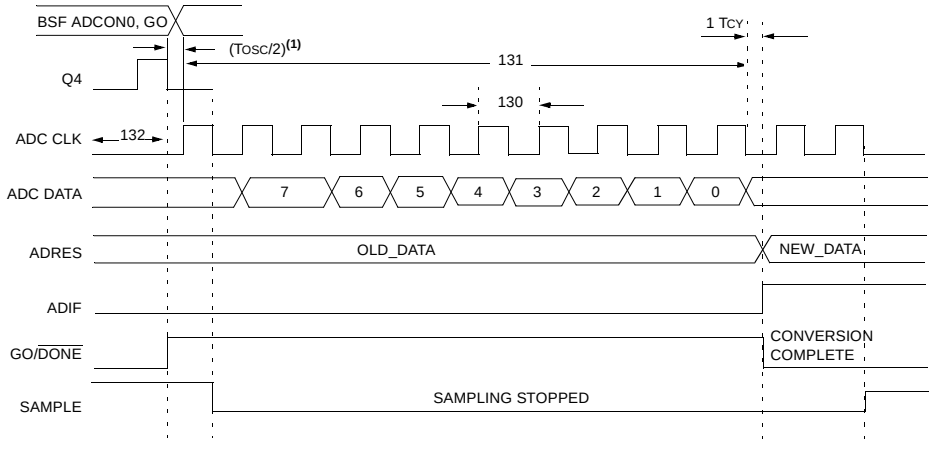
Note 1: When ADC is off, it will not consume any current other than minor leakage current. The power-down current specification (D020A) includes any such leakage from the ADC module.

2: ADCREF current is from RA3/AN3/VREF1 pin or AVDD pin, whichever is selected as reference input.

3: These specifications apply if ADCREF = 3.0 V and if AVDD ≥ 3.0 V. VAIN must be between VSS and ADCREF.

4: The A/D conversion result never decreases with an increase in the Input Voltage and has no missing codes.

FIGURE 17-11: ADC CONVERSION TIMING



Note 1: If the ADC clock source is selected as RC, a time of TCY is added before the ADC clock starts. This allows the SLEEP instruction to be executed.

TABLE 17-19: ADC CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	ADC clock period ADC Internal RC Oscillator Period	PIC16C781/782 PIC16LC781/782	2.0 TBD	4.0 TBD	6.0 TBD	µs µs	ADC RC mode
131	TCNV	Conversion time (not including S/H time)(1)		—	9.5	—	TAD	
132	TACQ	Acquisition time(2)		 5*	20 —	— —	µs µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 19.5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to ADC clock start		—	TOSC/2§	—	—	If the ADC clock source is selected as RC, a time of TCY is added before the ADC clock starts. This allows the SLEEP instruction to be executed.
135	TSWC	Switching from convert → sample time		1.5§	—	—	TAD	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ These specifications ensured by design.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 13.1 for min. conditions.

NOTES:

18.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for design guidance and are not tested nor guaranteed. In some graphs or tables the data presented is outside specified operating range (e.g., outside specified V_{DD} range.). This is for information only and devices are ensured to operate properly only within the specified range. The data presented in this section is a statistical summary of data collected on units from different lots over a period of time.

Standard deviation is denoted by sigma (σ).

Typ or Typical represents the mean of the distribution at 25°C.

Max or Maximum represents the mean +3σ over the temperature range of -40°C to 85°C.

Min or Minimum represents the mean -3σ over the temperature range of -40°C to 85°C.

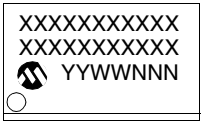
Graphs and Tables are not available at this time.

NOTES:

19.0 PACKAGING INFORMATION

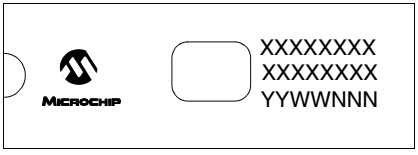
19.1 Package Marking Information

20-Lead SSOP

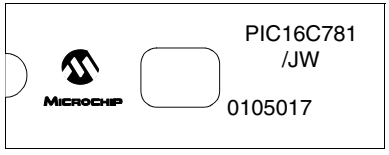


Example

20-Lead CERDIP Windowed

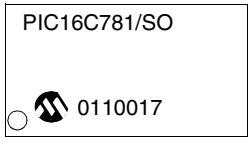


Example

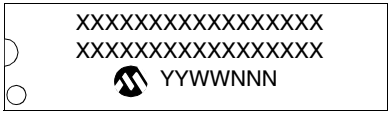


20-Lead SOIC

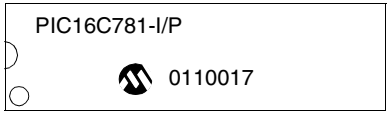
Example



20-Lead PDIP



Example

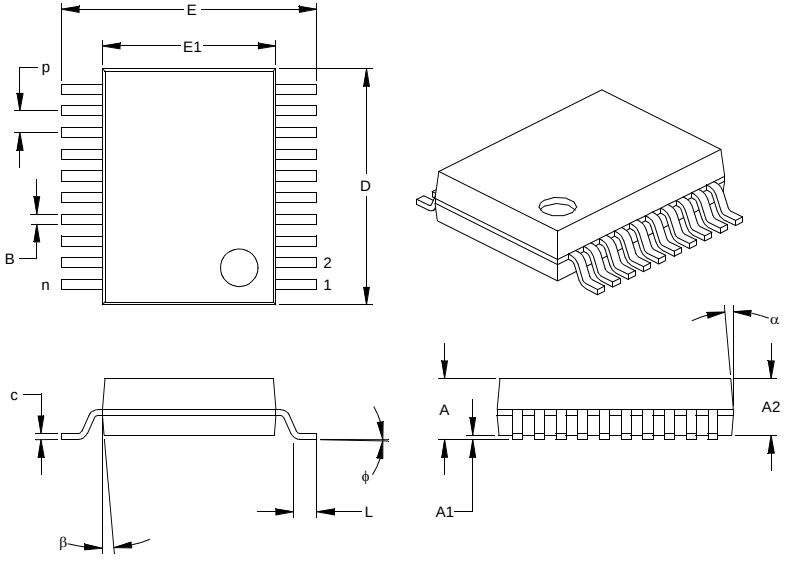


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	c	.004	.007	.010	0.10	0.18	0.25
Foot Angle	ϕ	0	4	8	0.00	101.60	203.20
Lead Width	B	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

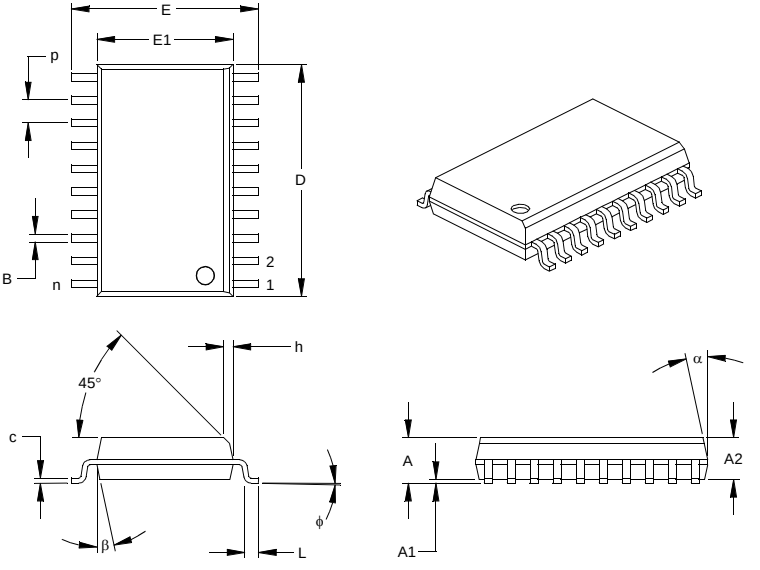
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MO-150
Drawing No. C04-072

20-Lead CERDIP Windowed

Diagram not available at this time.

20-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



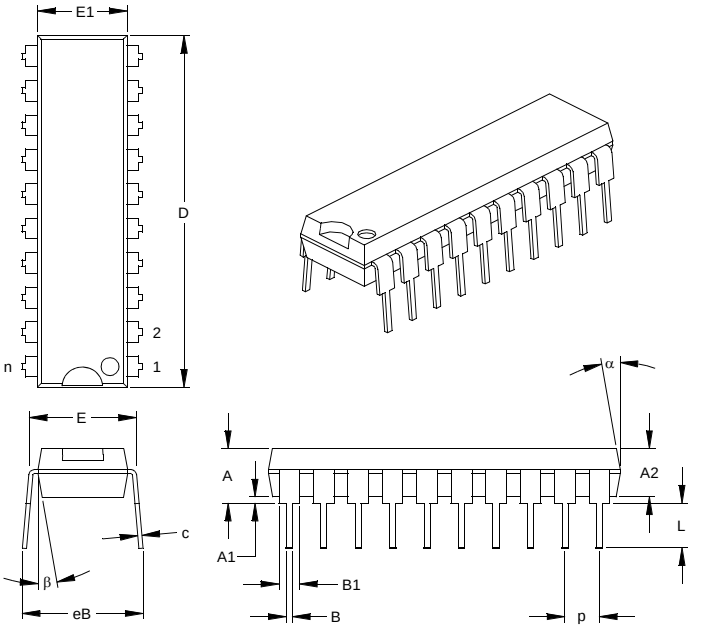
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.496	.504	.512	12.60	12.80	13.00
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-094

20-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.295	.310	.325	7.49	7.87	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	1.025	1.033	1.040	26.04	26.24	26.42
Tip to Seating Plane	L	.120	.130	.140	3.05	3.30	3.56
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.055	.060	.065	1.40	1.52	1.65
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-019

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PIC16C781/782 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC16C781: VDD range 4.0V-5.5V PIC16C781T: VDD range 4.0V-5.5V (Tape and Reel) PIC16LC781: VDD range 2.7V-5.5V PIC16LC781T: VDD range 2.7V-5.5V (Tape and Reel)
Temperature Range	I = -40°C to +85°C
Package	SO = SOIC SS = SSOP P = PDIP JW = Windowed CERDIP
Pattern	QTP, SQTP, ROM Code (factory specified) or Special Requirements . Blank for OTP and Windowed devices.

Examples:

a) PIC16C781-I/P Industrial Temp., Plastic DIP package, normal VDD limits

b) PIC16LC781-I/SS Industrial Temp., SSOP package, extended VDD limits

c) PIC16C781-I/SOT Industrial Temp., SOIC package, Tape and Reel, normal VDD limits

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type.

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