

+5V To $\pm 10V$ Voltage Converter

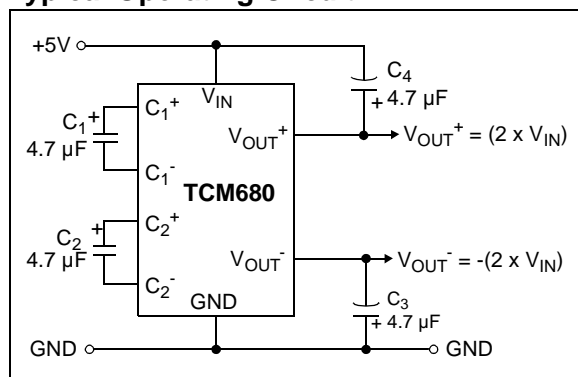
Features

- 99% Voltage Conversion Efficiency
- 85% Power Conversion Efficiency
- Input Voltage Range:
 - +2.0V to +5.5V
- Only 4 External Capacitors Required
- 8-Pin SOIC Package

Applications

- $\pm 10V$ From +5V Logic Supply
- $\pm 6V$ From a 3V Lithium Cell
- Handheld Instruments
- Portable Cellular Phones
- LCD Display Bias Generator
- Panel Meters
- Operational Amplifier Power Supplies

Typical Operating Circuit



General Description

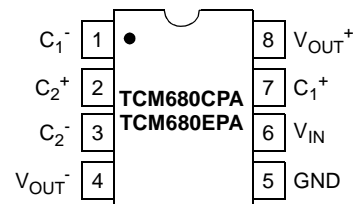
The TCM680 is a dual charge pump, voltage converter that produces output voltages of $+2V_{IN}$ and $-2V_{IN}$ from a single input voltage of +2.0V to +5.5V. Common applications include $\pm 10V$ from a single +5V logic supply and $\pm 6V$ from a +3V lithium battery.

The TCM680 is packaged in 8-pin SOIC and PDIP packages and requires only four inexpensive, external capacitors. The charge pumps are clocked by an on-board 8 kHz oscillator. Low output source impedances (typically 140 Ω) provide maximum output currents of 10 mA for each output. Typical power conversion efficiency is 85%.

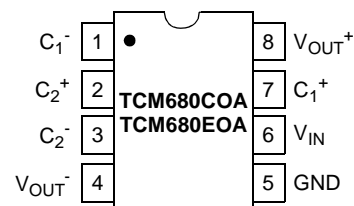
High efficiency, small size and low cost make the TCM680 suitable for a wide variety of applications that need both positive and negative power supplies derived from a single input voltage.

Package Type

PDIP



SOIC



TCM680

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{IN}	+5.8V
V_{OUT}^{+}	+11.6V
V_{OUT}^{-}	-11.6V
V_{OUT}^{+} Short-Circuit Duration.....	Continuous
V_{OUT}^{+} Current	75 mA
V_{IN} dV/dT	1 V/ μ sec
Power Dissipation ($T_A \leq 70^{\circ}\text{C}$)	
8-Pin PDIP	730 mW
8-Pin SOIC	470 mW
Operating Temperature Range.....	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	+150°C

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = +5\text{V}$, $T_A = +25^{\circ}\text{C}$, refer to Figure 1-1.						
Parameters	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage Range	V_{IN}	2.0	—	5.5	V	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, $R_L = 2\text{ k}\Omega$
Supply Current	I_{IN}	—	0.5	1.0	mA	$V_{IN} = 3\text{V}$, $R_L = \infty$
		—	1.0	2.0		$V_{IN} = 5\text{V}$, $R_L = \infty$
		—	—	2.5		$V_{IN} = 5\text{V}$, $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$, $R_L = \infty$
		—	—	3.0		$V_{IN} = 5\text{V}$, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, $R_L = \infty$
Negative Charge Pump Output Source Resistance	R_{OUT}^{-}	—	140	180	Ω	$I_L^{-} = 10\text{ mA}$, $I_L^{+} = 0\text{ mA}$, $V_{IN} = 5\text{V}$
		—	180	250		$I_L^{-} = 5\text{ mA}$, $I_L^{+} = 0\text{ mA}$, $V_{IN} = 2.8\text{V}$
		—	—	220		$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$
		—	—	250		$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
		—	—	—		$I_L^{-} = 10\text{ mA}$, $I_L^{+} = 0\text{ mA}$, $V_{IN} = 5\text{V}$
Positive Charge Pump Output Source Resistance	R_{OUT}^{+}	—	140	180	Ω	$I_L^{+} = 10\text{ mA}$, $I_L^{-} = 0\text{ mA}$, $V_{IN} = 5\text{V}$
		—	180	250		$I_L^{+} = 5\text{ mA}$, $I_L^{-} = 0\text{ mA}$, $V_{IN} = 2.8\text{V}$
		—	—	220		$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$
		—	—	250		$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
		—	—	—		$I_L^{+} = 10\text{ mA}$, $I_L^{-} = 0\text{ mA}$, $V_{IN} = 5\text{V}$
Oscillator Frequency	F_{OSC}	—	21	—	kHz	
Power Efficiency	P_{EFF}	—	85	—	%	$R_L = 2\text{ k}\Omega$
Voltage Conversion Efficiency	V_{OUTEFF}	97	99	—	%	V_{OUT}^{+} , $R_L = \infty$
		97	99	—		V_{OUT}^{-} , $R_L = \infty$

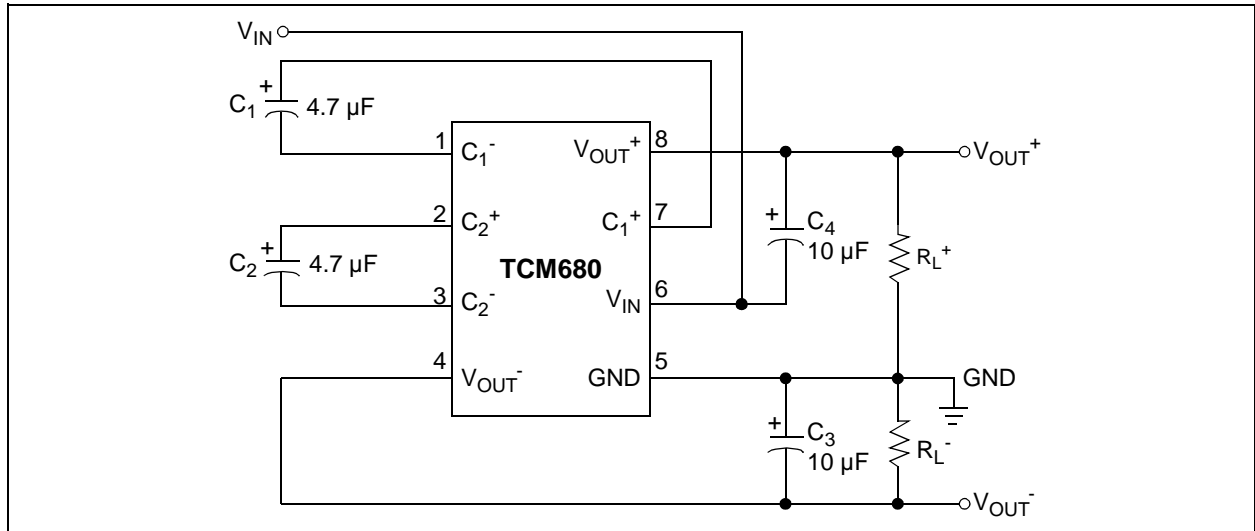


FIGURE 1-1: Test Circuit Used For DC Characteristics Table.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{IN} = +5V$, $T_A = +25^\circ C$.

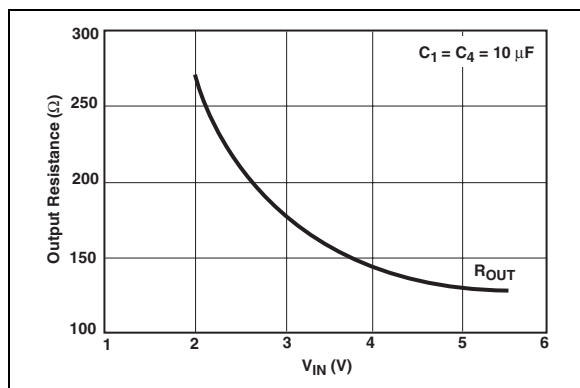


FIGURE 2-1: Output Resistance vs. V_{IN} .

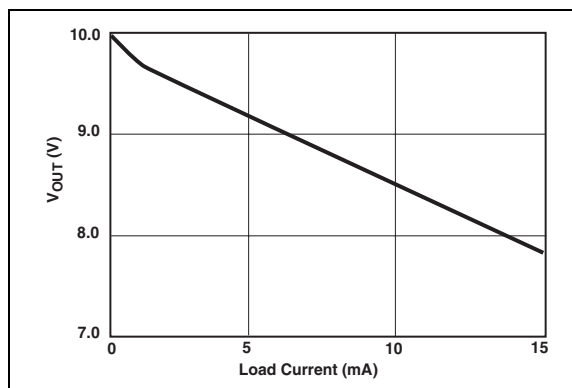


FIGURE 2-4: V_{OUT}^+ or V_{OUT}^- vs. Load Current.

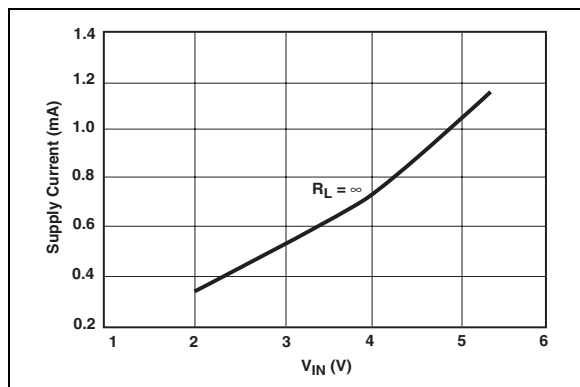


FIGURE 2-2: Supply Current vs. V_{IN} .

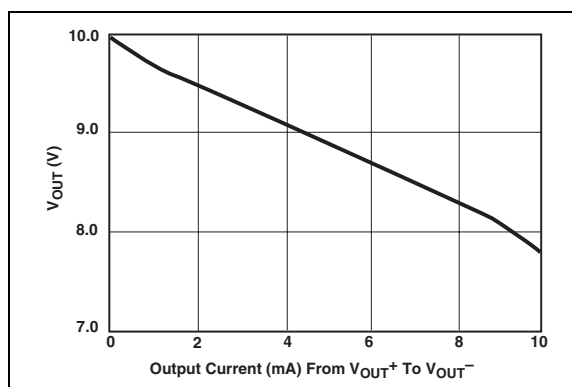


FIGURE 2-5: Output Voltage vs. Output Current.

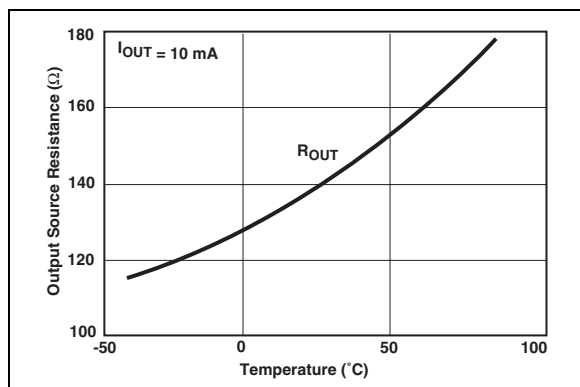


FIGURE 2-3: Output Source Resistance vs. Temperature.

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, SOIC)	Symbol	Description
1	C_1^-	Input. First charge pump capacitor. Negative connection
2	C_2^+	Input. Second charge pump capacitor. Positive connection.
3	C_2^-	Input. Second charge pump capacitor. Negative connection.
4	V_{OUT}^-	Output. Negative Output voltage
5	GND	Input. Ground connection.
6	V_{IN}	Input. Power supply.
7	C_1^+	Input. First charge pump capacitor. Positive connection.
8	V_{OUT}^+	Output. Positive Output Voltage.

3.1 First Charge Pump Capacitor (C_1^-)

Negative connection for the charge pump capacitor (flying capacitor) used to transfer charge from the input source to a second charge pump capacitor. This charge pump capacitor is used to double the input voltage and store the charge in the second charge pump capacitor.

It is recommended that a low ESR (equivalent series resistance) capacitor be used. Additionally, larger values will lower the output resistance.

3.2 Second Charge Pump Capacitor (C_2^+)

Positive connection for the second charge pump capacitor (flying capacitor) used to transfer charge from the first charge pump capacitor to the output.

It is recommended that a low ESR (equivalent series resistance) capacitor be used. Additionally, larger values will lower the output resistance.

3.3 Second Charge Pump Capacitor (C_2^-)

Negative connection for the second charge pump capacitor (flying capacitor) used to transfer charge from the first charge pump capacitor to the output. Proper orientation is imperative when using a polarized capacitor.

3.4 Negative Output Voltage (V_{OUT}^-)

Negative connection for the negative charge pump output capacitor. The negative charge pump output capacitor supplies the output load during the first, third and fourth phases of the switching cycle. During the second phase of the switching cycle, charge is restored to the negative charge pump output capacitor. The negative output voltage magnitude is approximately twice the input voltage.

It is recommended that a low ESR (equivalent series resistance) capacitor be used. Additionally, larger values will lower the output ripple.

3.5 Ground (GND)

Input zero volt reference.

3.6 Power Supply Input (V_{IN})

Positive power supply input voltage connection. It is recommended that a low ESR (equivalent series resistance) capacitor be used to bypass the power supply input to ground (GND).

3.7 First Charge Pump Capacitor (C_1^+)

Positive connection for the charge pump capacitor (flying capacitor) used to transfer charge from the input source to a second charge pump capacitor. Proper orientation is imperative when using a polarized capacitor.

3.8 Positive Output Voltage (V_{OUT}^+)

Positive connection for the positive charge pump output capacitor. The positive charge pump output capacitor supplies the output load during the first, second and third phases of the switching cycle. During the fourth phase of the switching cycle, charge is restored to the positive charge pump output capacitor. The positive output voltage magnitude is approximately twice the input voltage.

It is recommended that a low ESR (equivalent series resistance) capacitor be used. Additionally, larger values will lower the output ripple.

4.0 DETAILED DESCRIPTION

4.1 V_{OUT}^- Charge Storage - Phase 1

The positive side of capacitors C_1 and C_2 are connected to +5V at the start of this phase. C_1^+ is then switched to ground and the charge in C_1^- is transferred to C_2^- . Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

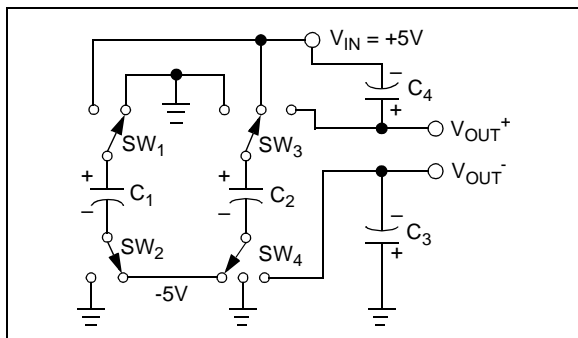


FIGURE 4-1: Charge Pump - Phase 1.

4.2 V_{OUT}^- Transfer - Phase 2

Phase two of the clock connects the negative terminal of C_2 to the V_{OUT}^- storage capacitor C_3 and the positive terminal of C_2 to ground, transferring the generated -10V to C_3 . Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

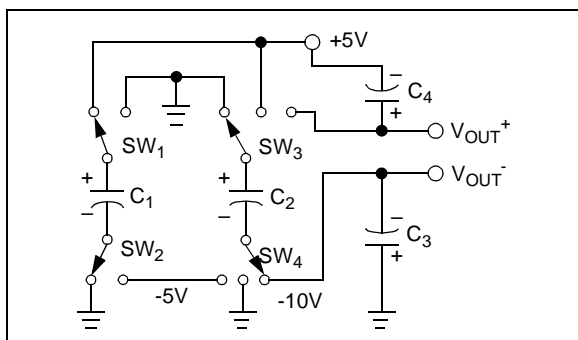


FIGURE 4-2: Charge Pump - Phase 2.

4.3 V_{OUT}^+ Charge Storage - Phase 3

The third phase of the clock is identical to the first phase – the charge stored in C_1 produces -5V in the negative terminal of C_1 , which is applied to the negative side of capacitor C_2 . Since C_2^+ is at +5V, the voltage potential across C_2 is 10V.

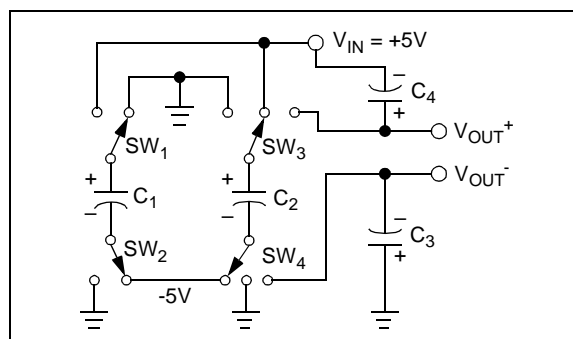


FIGURE 4-3: Charge Pump - Phase 3.

4.4 V_{OUT}^+ Transfer - Phase 4

The fourth phase of the clock connects the negative terminal of C_2 to ground and transfers the generated 10V across C_2 to C_4 , the V_{OUT}^+ storage capacitor. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

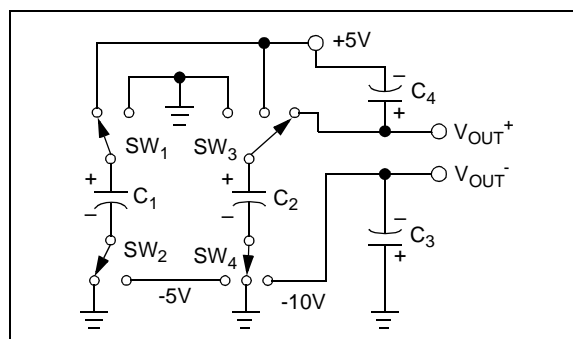


FIGURE 4-4: Charge Pump - Phase 4.

4.5 Maximum Operating Limits

The maximum input voltage rating must be observed. The TCM680 will clamp the input voltage to 5.8V. Exceeding this maximum threshold will cause excessive current to flow through the TCM680, potentially causing permanent damage to the device.

4.6 Switched Capacitor Converter Power Losses

The overall power loss of a switched capacitor converter is affected by four factors:

1. Losses from power consumed by the internal oscillator, switch drive, etc. These losses will vary with input voltage, temperature and oscillator frequency.
2. Conduction losses in the non-ideal switches.
3. Losses due to the non-ideal nature of the external capacitors.
4. Losses that occur during charge transfer from the pump to reservoir capacitors when a voltage difference between the capacitors exists.

The power loss for the TCM680 is calculated using the following equation:

EQUATION

$$P_{LOSS} = (I_{OUT+})^2 \times R_{OUT-} + (I_{OUT-})^2 \times R_{OUT+} + I_{IN} \times V_{IN}$$

5.0 APPLICATIONS INFORMATION

5.1 Voltage Multiplication and Inversion

The TCM680 performs voltage multiplication and inversion simultaneously, providing positive and negative outputs (Figure 5-1). The magnitude of both outputs is, approximately, twice the input voltage. Unlike other switched capacitor converters, the TCM680 requires only four external capacitors to provide both functions simultaneously.

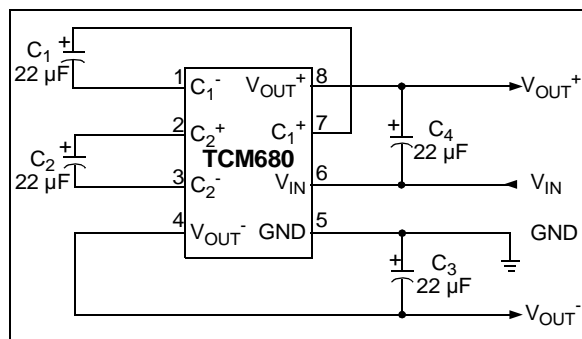


FIGURE 5-1: Positive and Negative Converter.

5.2 Capacitor Selection

The TCM680 requires only 4 external capacitors for operation, which can be inexpensive, polarized aluminum electrolytic types. For the circuit in Figure 5-1, the output characteristics are largely determined by the external capacitors. An expression for R_{OUT} can be derived as shown below:

EQUATION

$$R_{OUT}^{+} = 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) + 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2) + ESR_{C4}$$

$$R_{OUT}^{-} = 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) + 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2) + ESR_{C3}$$

Assuming all switch resistances are approximately equal:

EQUATION

$$R_{OUT}^{+} = 32R_{SW} + 8ESR_{C1} + 8ESR_{C2} + ESR_{C4} + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2)$$

$$R_{OUT}^{-} = 32R_{SW} + 8ESR_{C1} + 8ESR_{C2} + ESR_{C3} + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2)$$

R_{OUT} is typically 140Ω at $+25^{\circ}\text{C}$ with $V_{IN} = +5\text{V}$ and C_1 and C_2 as $4.7\mu\text{F}$ low ESR capacitors. The fixed term ($32R_{SW}$) is about 130Ω . It can easily be seen that increasing or decreasing values of C_1 and C_2 will affect efficiency by changing R_{OUT} . However, be careful about ESR. This term can quickly become dominant with large electrolytic capacitors. Table 5-1 shows R_{OUT} for various values of C_1 and C_2 (assume 0.5Ω ESR). C_1 and C_4 must be rated at 6 VDC or greater while C_2 and C_3 must be rated at 12 VDC or greater.

Output voltage ripple is affected by C_3 and C_4 . Typically, the larger the value of C_3 and C_4 , the less the ripple for a given load current. The formula for $V_{RIPPLE(p-p)}$ is given below:

EQUATION

$$V_{RIPPLE(p-p)}^{+} = \{1/[2(f_{PUMP}/3) \times C4] + 2(ESR_{C4})\} (I_{OUT}^{+})$$

$$V_{RIPPLE(p-p)}^{-} = \{1/[2(f_{PUMP}/3) \times C3] + 2(ESR_{C3})\} (I_{OUT}^{-})$$

For a $10\mu\text{F}$ (0.5Ω ESR) capacitor for C_3 , C_4 , $f_{PUMP} = 21\text{ kHz}$ and $I_{OUT} = 10\text{ mA}$, the peak-to-peak ripple voltage at the output will be less than 100 mV . In most applications ($I_{OUT} \leq 10\text{ mA}$), $10\text{-}20\mu\text{F}$ output capacitors and $1\text{-}5\mu\text{F}$ pump capacitors will suffice. Table 5-2 shows V_{RIPPLE} for different values of C_3 and C_4 (assume 1Ω ESR).

TABLE 5-1: OUTPUT RESISTANCE VS. C_1 , C_2

$C_1, C_2 (\mu\text{F})$	$R_{OUT}^{+}, R_{OUT}^{-} (\Omega)$
0.1	1089
0.47	339
1	232
3.3	165
4.7	157
10	146
22	141
100	137

TABLE 5-2: V_{RIPPLE} PEAK-TO-PEAK VS. C_3 , C_4 ($I_{OUT} 10\text{ mA}$)

$C_3, C_4 (\mu\text{F})$	$V_{RIPPLE(p-p)}^{+}, V_{RIPPLE(p-p)}^{-} (\text{mV})$
0.47	1540
1	734
3.3	236
4.7	172
10	91
22	52
100	27

5.3 Paralleling Devices

To reduce the value of R_{OUT}^- and R_{OUT}^+ , multiple TCM680 voltage converters can be connected in parallel (Figure 5-2). The output resistance of both outputs will be reduced, approximately, by a factor of n , where n is the number of devices connected in parallel.

EQUATION

$$R_{OUT}^- = \frac{R_{OUT}^- \text{ (of TCM680)}}{n \text{ (number of devices)}}$$

EQUATION

$$R_{OUT}^+ = \frac{R_{OUT}^+ \text{ (of TCM680)}}{n \text{ (number of devices)}}$$

Each device requires its own pump capacitors, but all devices may share the same reservoir capacitors. To preserve ripple performance, the value of the reservoir capacitors should be scaled according to the number of devices connected in parallel.

5.4 Output Voltage Regulation

The outputs of the TCM680 can be regulated to provide +5V from a 3V input source (Figure 5-3). The TCM680 performs voltage multiplication and inversion producing output voltages of, approximately, +6V. The TCM680 outputs are regulated to +5V with the linear regulators TC55 and TC59. The TC54 is a voltage detector providing an indication that the input source is low and that the outputs may fall out of regulation. The input source to the TCM680 can vary from 2.8V to 5.5V without adversely affecting the output regulation making this application well suited for use with single cell Li-Ion batteries or three alkaline or nickel based batteries connected in series.

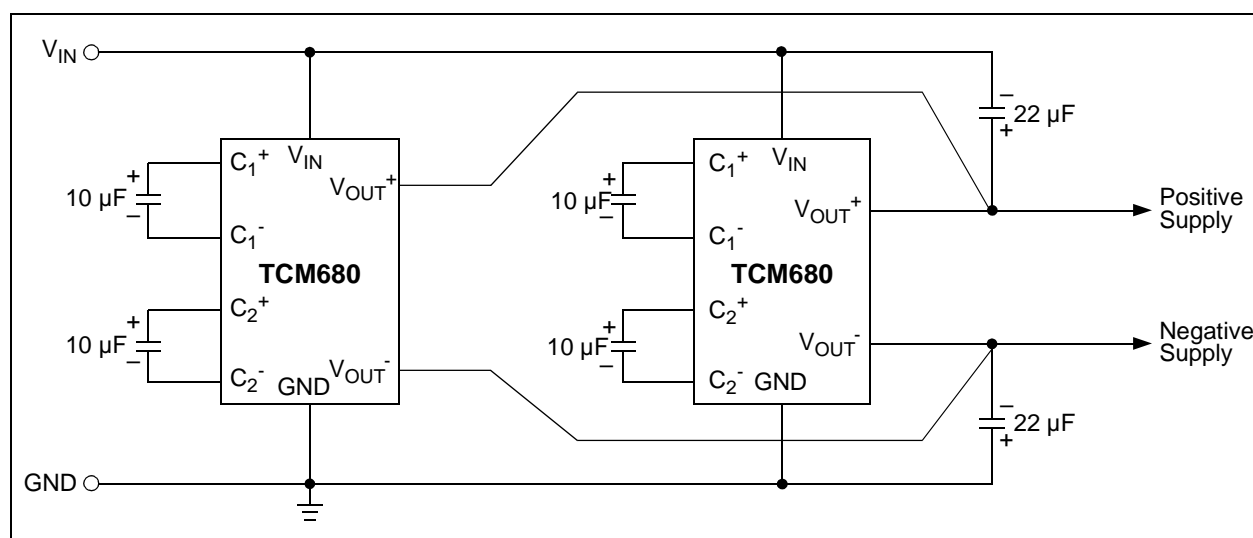


FIGURE 5-2: Paralleling TCM680 for Lower Output Source Resistance.

TCM680

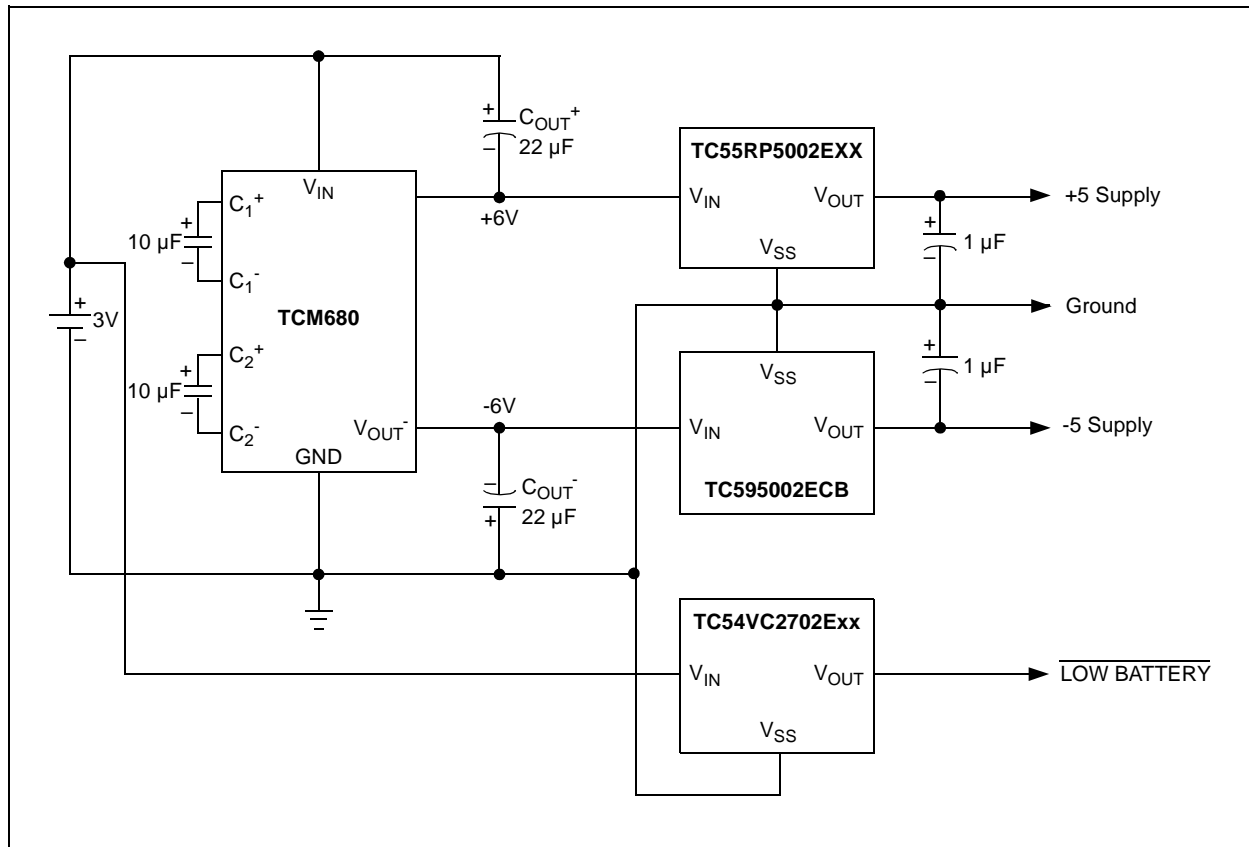
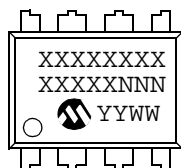


FIGURE 5-3: Split Supply Derived from 3V Battery.

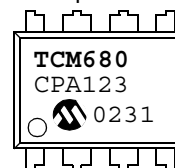
6.0 PACKAGING INFORMATION

6.1 Packaging Marking Information

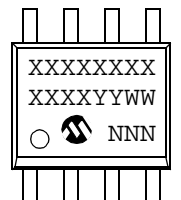
8-Lead PDIP (300 mil)



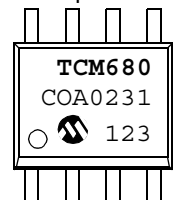
Example:



8-Lead SOIC (150 mil)



Example:



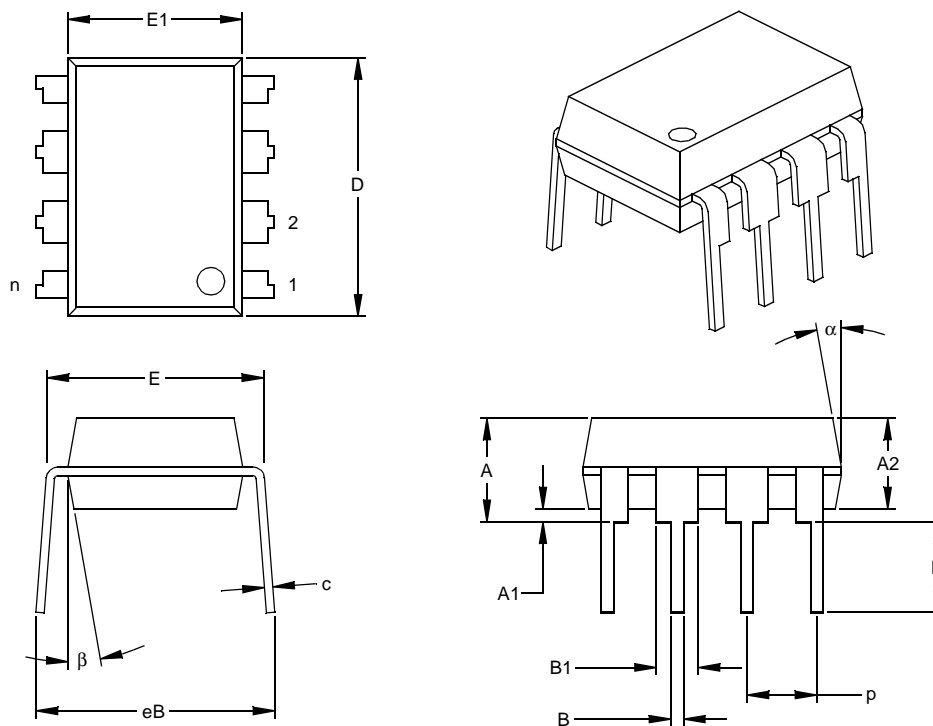
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

TCM680

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

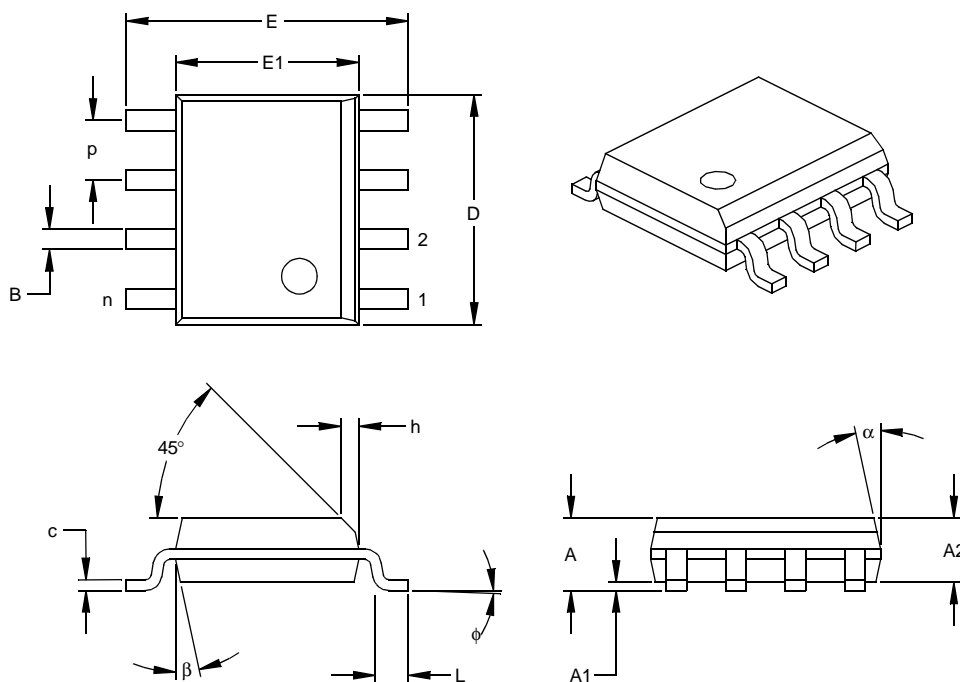
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

TCM680

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>		<u>X</u>	<u>/XX</u>
Device		Temperature Range	Package
Device:		TCM680: Charge Pump Converter	
Temperature Range:		C = 0°C to +70°C E = -40°C to +85°C	
Package:		PA = Plastic DIP (300 mil Body), 8-lead OA = Plastic SOIC, (150 mil Body), 8-lead OATR = Plastic SOIC, (150 mil Body), 8-lead (Tape and Reel)	
		Examples:	
		a) TCM680COA: Charge Pump Converter, SOIC pkg, 0°C to +70°C.	
		b) TCM680COATR: Charge Pump Converter, SOIC pkg, 0°C to +70°C, Tape and Reel.	
		c) TCM680CPA: Charge Pump Converter, PDIP pkg, 0°C to +70°C.	
		d) TCM680EOA: Charge Pump Converter, SOIC pkg, -40°C to +85°C.	
		e) TCM680EOATR: Charge Pump Converter, SOIC pkg, -40°C to +85°C, Tape and Reel.	
		f) TCM680EPA: Charge Pump Converter, PDIP pkg, -40°C to +85°C.	

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



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