



Not recommended for new designs –
Please use 93LC46C, 93LC56C or 93LC66C.

93LC46/56/66

1K/2K/4K 2.5V Microwire Serial EEPROM

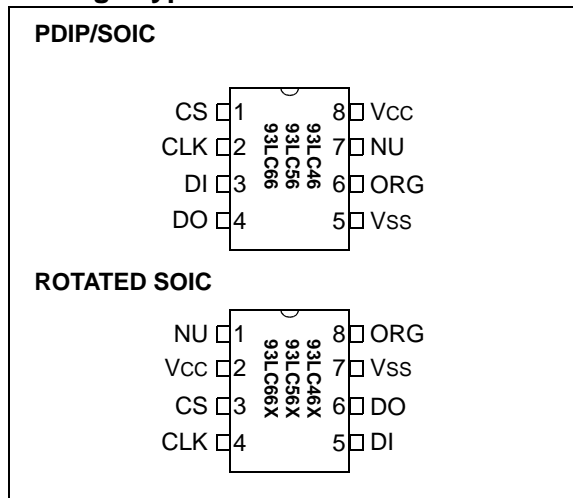
Features:

- Single supply with programming operation down to 2.5V
- Low-power CMOS technology
- 100 μ A typical active read current at 2.5V
- 3 μ A typical standby current at 2.5V
- ORG pin selectable memory configuration
- 128 x 8- or 64 x 16-bit organization (93LC46)
- 256 x 8- or 128 x 16-bit organization (93LC56)
- 512 x 8 or 256 x 16 bit organization (93LC66)
- Self-timed erase and write cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during erase/write cycles
- Sequential read function
- 1,000,000 E/W cycles ensured
- Data retention > 200 years
- 8-pin PDIP/SOIC (SOIC in JEDEC standards)
- Temperature ranges supported:
 - Industrial (I): -40°C to +85°C

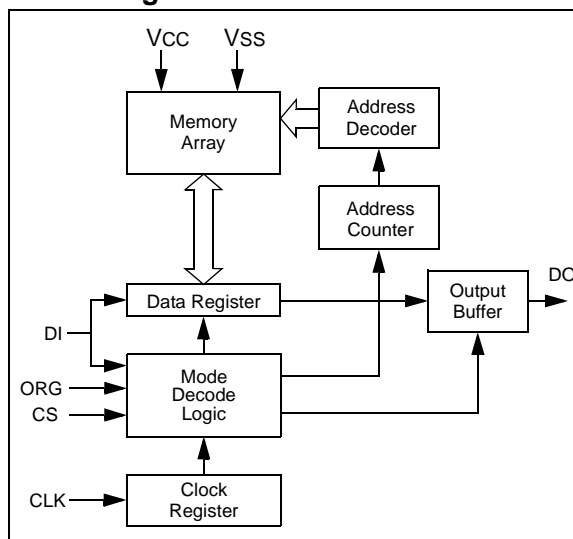
Description:

The Microchip Technology Inc. 93LC46/56/66 are 1K, 2K and 4K low voltage serial Electrically Erasable PROMs (EEPROM). The device memory is configured as x8 or x16 bits depending on the external logic of levels of the ORG pin. Advanced CMOS technology makes these devices ideal for low power nonvolatile memory applications. The 93LC Series is available in standard 8-pin PDIP and surface mount SOIC packages. The rotated pin-out 93LC46X/56X/66X are offered in the “SN” package only.

Package Types



Block Diagram



93LC46/56/66

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

V _{CC}	6.5V
All inputs and outputs w.r.t. V _{SS}	-0.6V to V _{CC} + 1.0V
Storage temperature	-65°C to +150°C
Ambient temperature with power applied.....	-40°C to +125°C
ESD protection on all pins	≥ 4 kV

† **NOTICE:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

DC CHARACTERISTICS			V _{CC} = +2.5V to +5.5V Industrial (I): T _A = -40°C to +85°C				
Param. No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
D1	V _{IH1}	High-level input voltage	2.0	—	V _{CC} +1	V	V _{CC} ≥ 2.7V
	V _{IH2}		0.7 V _{CC}	—	V _{CC} +1	V	V _{CC} ≥ 2.7V
D2	V _{IL1}	Low-level input voltage	-0.3	—	0.8	V	V _{CC} ≥ 2.7V
	V _{IL2}		-0.3	—	0.2 V _{CC}	V	V _{CC} ≥ 2.7V
D3	V _{OL1}	Low-level output voltage	—	—	0.4	V	I _{OL} = 2.1 mA, V _{CC} = 4.5V
	V _{OL2}		—	—	0.3	V	I _{OL} = 100 μA, V _{CC} = 2.5V
D4	V _{OH1}	High-level output voltage	2.4	—	—	V	I _{OL} = 400 μA, V _{CC} = 4.5V
	V _{OH2}		V _{CC} -0.2	—	—	V	I _{OL} = 100 μA, V _{CC} = 2.5V
D5	I _{LI}	Input leakage current	—	—	±10	μA	V _{IN} = 0.1V to V _{CC}
D6	I _{LO}	Output leakage current	—	—	±10	μA	V _{OUT} = 0.1V to V _{CC}
D7	C _{IN} , C _{OUT}	Pin capacitance (all inputs/outputs)	—	—	7	pF	V _{IN} /V _{OUT} = 0V (Note 1 & 2) T _A = 25°C, F _{CLK} = 1 MHz
D8	I _{CC} write	Operating current	—	—	3	mA	F _{CLK} = 2 MHz, V _{CC} = 5.5V (Note 2)
D9	I _{CC} read		—	—	1	mA	F _{CLK} = 2 MHz, V _{CC} = 5.5V
			—	—	500	μA	F _{CLK} = 1 MHz, V _{CC} = 3.0V
D10	I _{CCS}	—	100	—	μA	F _{CLK} = 1 MHz, V _{CC} = 2.5V	
		—	—	30	μA	CLK = CS = 0V; V _{CC} = 5.5V	
		—	3	—	μA	CLK = CS = 0V; V _{CC} = 3.0V CLK = CS = 0V; V _{CC} = 2.5V ORG, DI = V _{SS} or V _{CC}	

- Note 1:** This parameter is tested at T_A = 25°C and F_{CLK} = 1 MHz.
Note 2: This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS

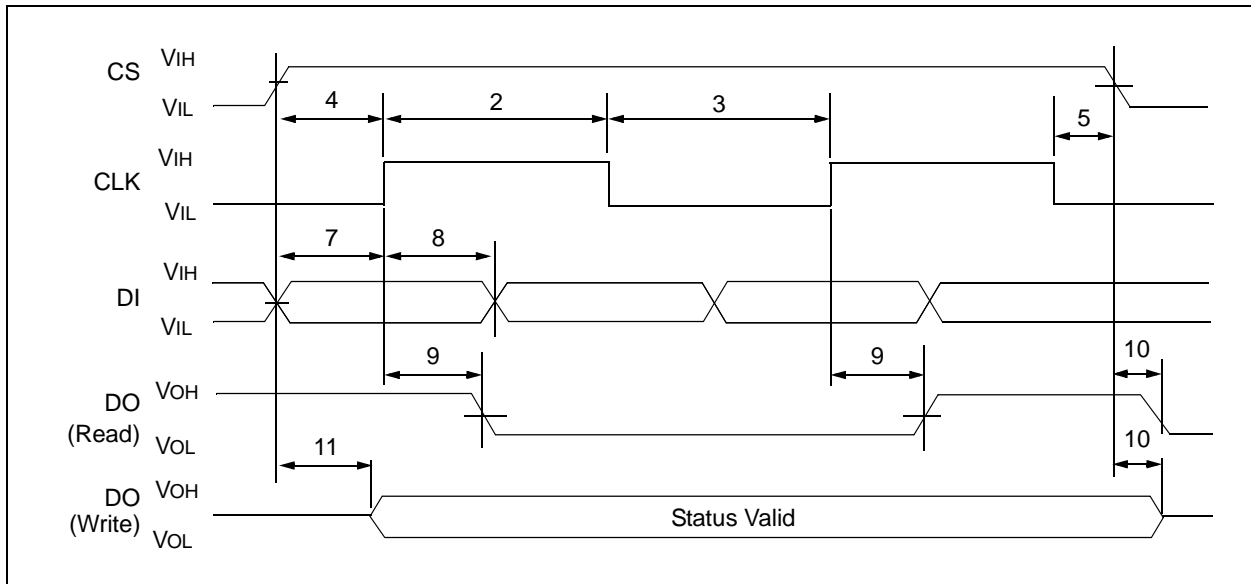
AC CHARACTERISTICS			VCC = +2.5V to +5.5V Industrial (I): TA = -40°C to +85°C				
Param. No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
1	FCLK	Clock frequency	—	—	2	MHz	VCC ≥ 4.5V
			—	—	1	MHz	VCC < 4.5V
2	TCKH	Clock high time	250	—	—	ns	
3	TCKL	Clock low time	250	—	—	ns	
4	TCSS	Chip select setup time	50	—	—	ns	Relative to CLK
5	TCSH	Chip select hold time	0	—	—	ns	Relative to CLK
6	TCSL	Chip select low time	250	—	—	ns	
7	TDIS	Data input setup time	100	—	—	ns	Relative to CLK
8	TDIH	Data input hold time	100	—	—	ns	Relative to CLK
9	TPD	Data output delay time	—	—	400	ns	CL = 100 pF
10	TCZ	Data output disable time	—	—	100	ns	CL = 100 pF (Note 2)
11	TSV	Status valid time	—	—	500	ns	CL = 100 pF
12	TWC	Program cycle time	—	4	10	ms	Erase/Write mode
13	TEC		—	8	15	ms	ERAL mode (VCC=5V ±10%)
14	TWL		—	16	30	ms	WRAL mode (VCC=5V ±10%)
15	—	Endurance	1M	—	1M	cycles	25°C, VCC = 5.0V, Block mode (Note 3)

Note 1: This parameter is tested at TA = 25°C and FCLK = 1 MHz.

2: This parameter is periodically sampled and not 100% tested.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at: www.microchip.com.

FIGURE 1-1: SYNCHRONOUS DATA TIMING



93LC46/56/66

TABLE 1-1: INSTRUCTION SET FOR 93LC46: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 XXXX	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	9
ERAL	1	00	1 0 XXXX	—	(RDY/BSY)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	25
WRAL	1	00	0 1 XXXX	D15 - D0	(RDY/BSY)	25
EWDS	1	00	0 0 XXXX	—	High-Z	9

TABLE 1-2: INSTRUCTION SET FOR 93LC46: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	18
EWEN	1	00	1 1 X X X X X	—	High-Z	10
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	10
ERAL	1	00	1 0 X X X X X	—	(RDY/BSY)	10
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/BSY)	18
EWDS	1	00	0 0 X X X X X	—	High-Z	10

TABLE 1-3: INSTRUCTION SET FOR 93LC56: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/BSY)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

TABLE 1-4: INSTRUCTION SET FOR 93LC56: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/BSY)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/BSY)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

TABLE 1-5: INSTRUCTION SET FOR 93LC66: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/BSY)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

TABLE 1-6: INSTRUCTION SET FOR 93LC66: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X	—	High-Z	12
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	12
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	12
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	20
WRAL	1	00	0 1 X X X X X X	D7 - D0	(RDY/BSY)	20
EWDS	1	00	0 0 X X X X X X	—	High-Z	12

2.0 FUNCTIONAL DESCRIPTION

When the ORG pin is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an erase/write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

2.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL and WRAL). As soon as CS is high, the device is no longer in the Standby mode.

An instruction following a Start condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become “don't care” bits until a new Start condition is detected.

2.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a “bus conflict” to occur during the “dummy zero” that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Data Protection

During power-up, all programming modes of operation are inhibited until VCC has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when VCC has fallen below 1.4V at nominal conditions.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

2.4 Read

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16-bit (x16 organization) or 8-bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

2.5 Erase/Write Enable and Disable (EWEN, EWDS)

The 93LC46/56/66 power up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all erase/write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

2.6 Erase

The ERASE instruction forces all data bits of the specified address to the logical “1” state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical “0” indicates that programming is still in progress. DO at logical “1” indicates that the register at the specified address has been erased and the device is ready for another instruction.

The erase cycle takes 4 ms per word typical.

2.7 Write

The `WRITE` instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The write cycle takes 4 ms per word typical.

2.8 Erase All (ERAL)

The `ERAL` instruction will erase the entire memory array to the logical "1" state. The `ERAL` cycle is identical to the `ERASE` cycle except for the different opcode. The `ERAL` cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The `ERAL` instruction is ensured at 5V ±10%.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete.

The `ERAL` cycle takes (8 ms typical).

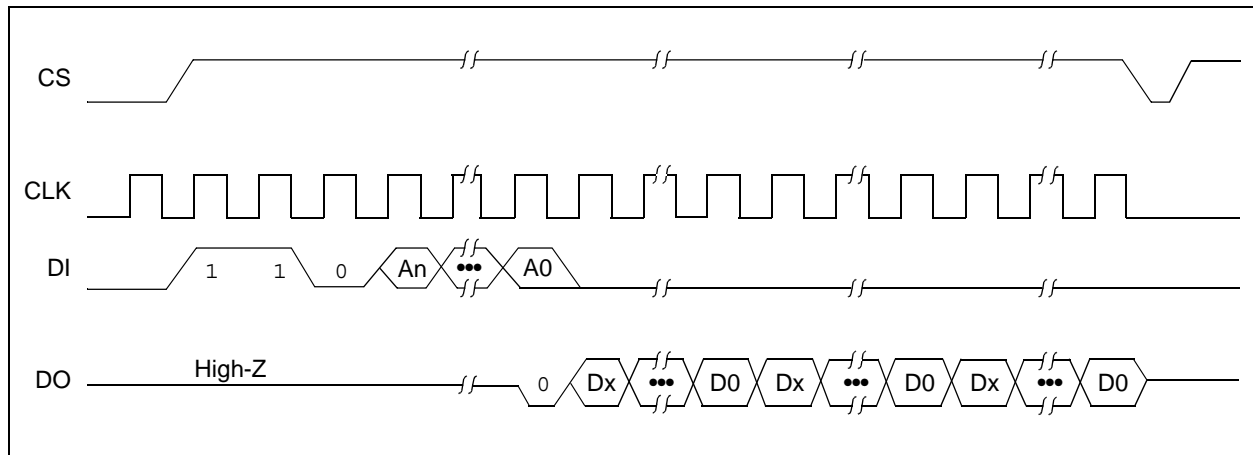
2.9 Write All (WRAL)

The `WRAL` instruction will write the entire memory array with the data specified in the command. The `WRAL` cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The `WRAL` command does include an automatic `ERAL` cycle for the device. Therefore, the `WRAL` instruction does not require an `ERAL` instruction but the chip must be in the `EWEN` status. The `WRAL` instruction is ensured at 5V ±10%.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The `WRAL` cycle takes 16 ms typical.

FIGURE 2-1: READ TIMING



93LC46/56/66

FIGURE 2-2: EWEN TIMING

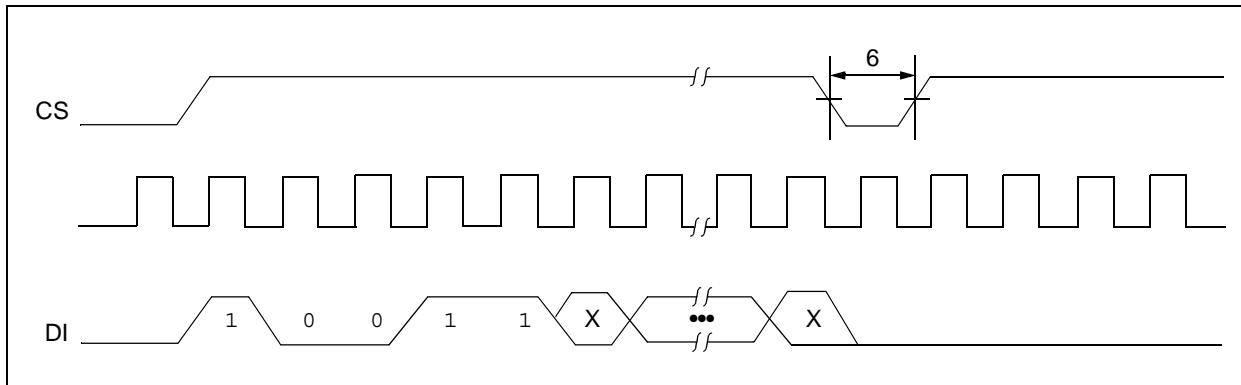


FIGURE 2-3: EWDS TIMING

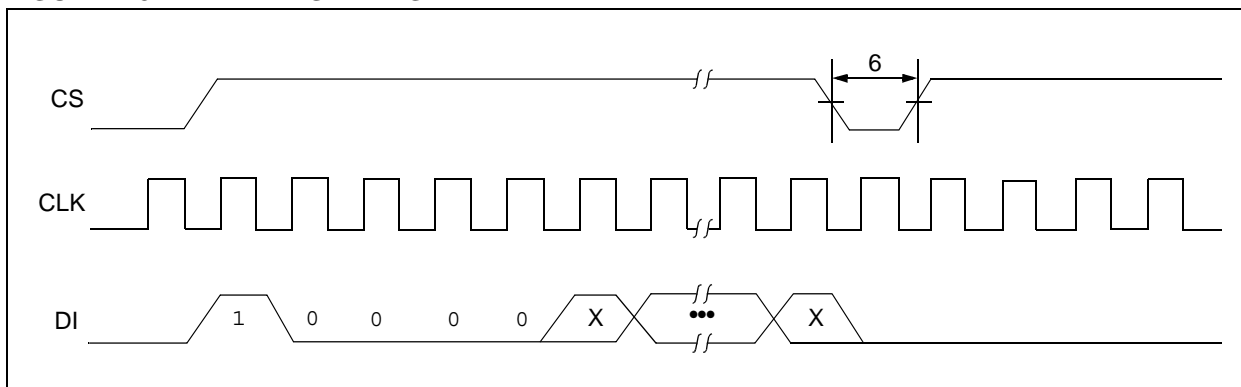


FIGURE 2-4: WRITE TIMING

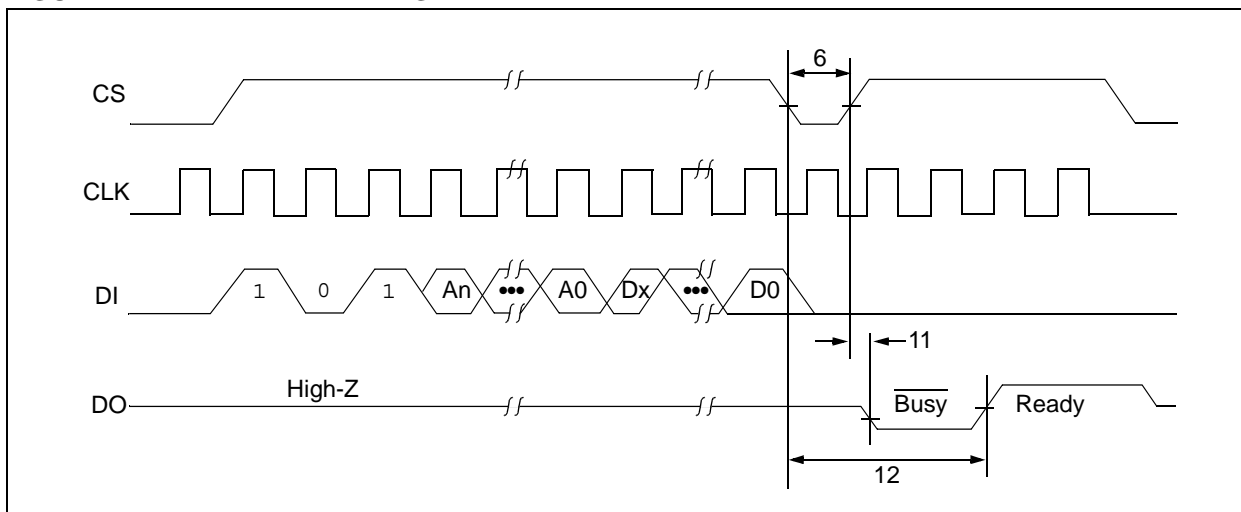


FIGURE 2-5: WRAL TIMING

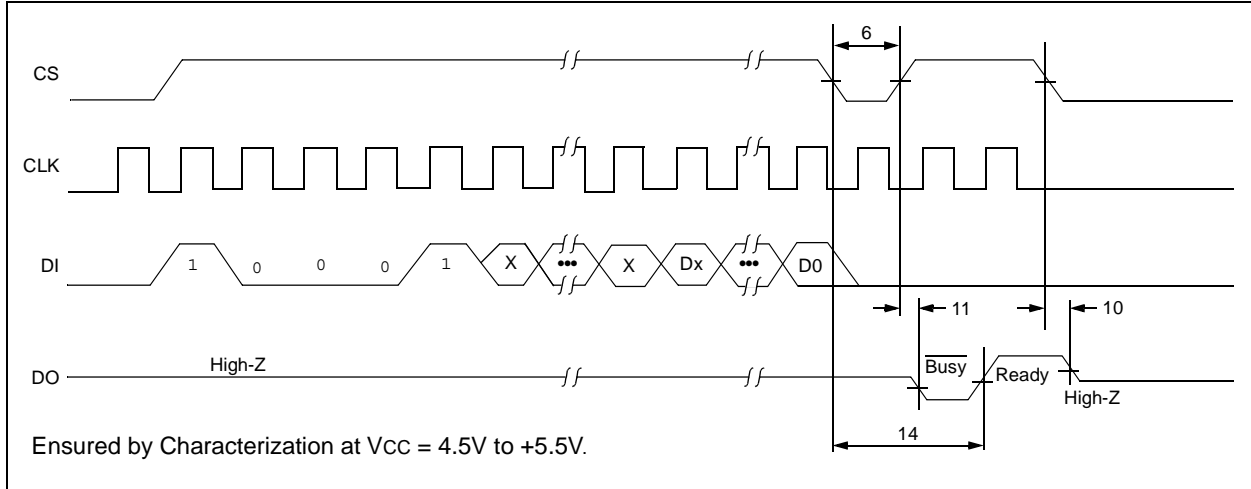


FIGURE 2-6: ERASE TIMING

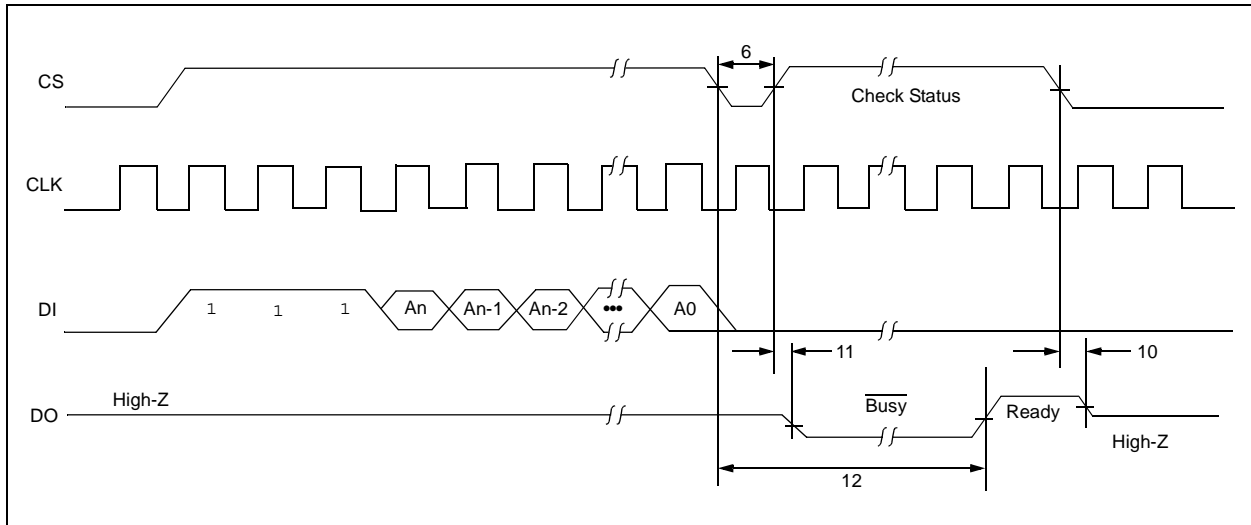
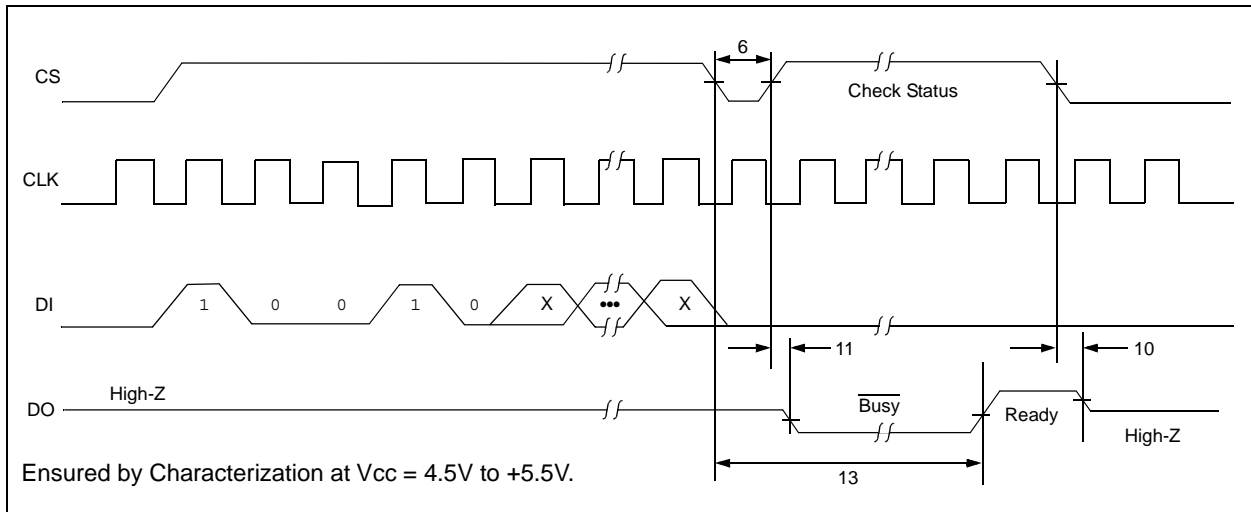


FIGURE 2-7: ERAL TIMING



93LC46/56/66

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	PDIP	SOIC	ROTATED TSSOP	Description
CS	1	1	3	Chip Select
CLK	2	2	4	Serial Data Clock
DI	3	3	5	Serial Data Input
DO	4	4	6	Serial Data Output
Vss	5	5	7	Ground
ORG	6	6	8	Memory Configuration
NU	7	7	1	Not Utilized
Vcc	8	8	2	+1.8V to 5.5V Power Supply

3.1 Chip Select (CS)

A high level selects the device. A low level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (T_{CSL}) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

3.2 Serial Clock (CLK)

The serial clock is used to synchronize the communication between a master device and the 93LC46/56/66. Opcode, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (T_{CKH}) and clock low time (T_{CKL}). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a “don't care” if CS is low (device deselected). If CS is high, but Start condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for Start condition).

CLK cycles are not required during the self-timed write (i.e., auto erase/write) cycle.

After detection of a Start condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become “don't care” inputs waiting for a new Start condition to be detected.

Note: CS must go low between consecutive instructions.

3.3 Data In (DI)

Data In is used to clock in a Start bit, opcode, address and data synchronously with the CLK input.

3.4 Data Out (DO)

Data Out is used in the Read mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK).

This pin also provides Ready/Busy status information during erase and write cycles. Ready/Busy status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (T_{CSL}) and an erase or write operation has been initiated.

The Status signal is not available on DO, if CS is held low or high during the entire write or erase cycle. In all other cases DO is in the High-Z mode. If status is checked after the write/erase cycle, a pull-up resistor on DO is required to read the Ready signal.

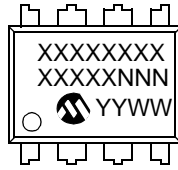
3.5 Organization (ORG)

When ORG is connected to V_{CC}, the (x16) memory organization is selected. When ORG is tied to V_{SS}, the (x8) memory organization is selected. ORG can only be floated for clock speeds of 1 MHz or less for the (x16) memory organization. For clock speeds greater than 1 MHz, ORG must be tied to V_{CC} or V_{SS}.

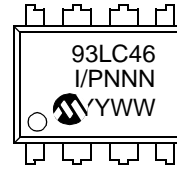
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

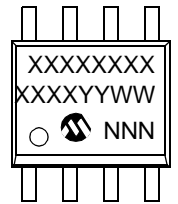
8-Lead PDIP (300 mil)



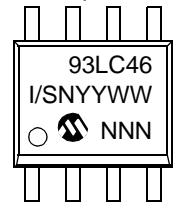
Example:



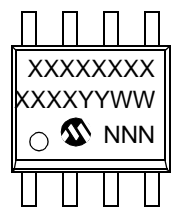
8-Lead SOIC (150 mil)



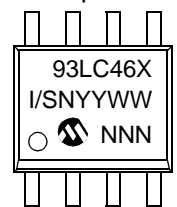
Example:



8-Lead Rotated SOIC (150 mil)



Example:



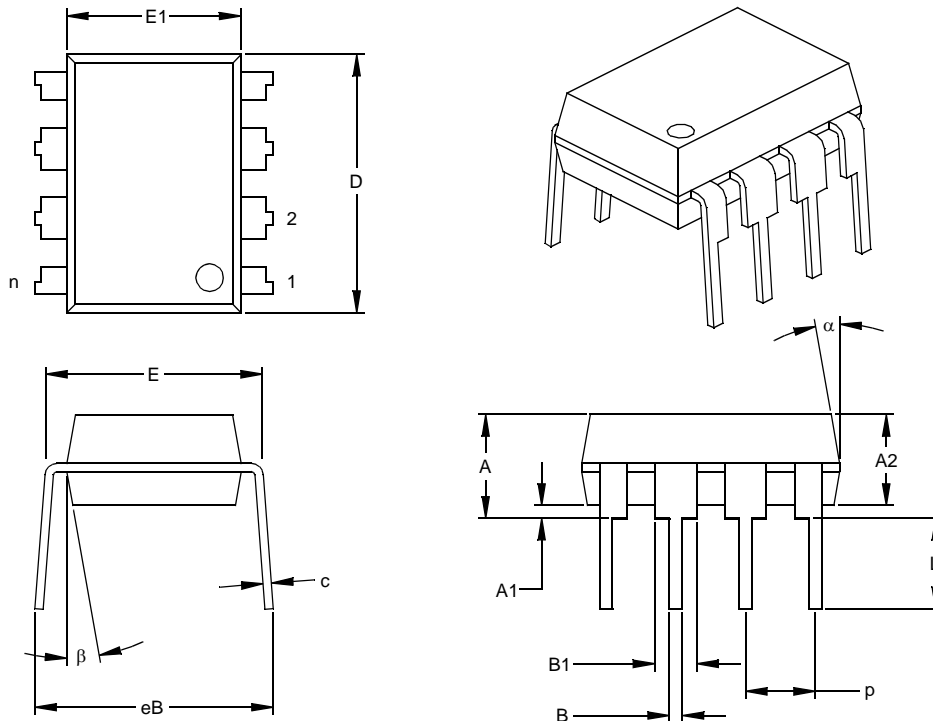
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

93LC46/56/66

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

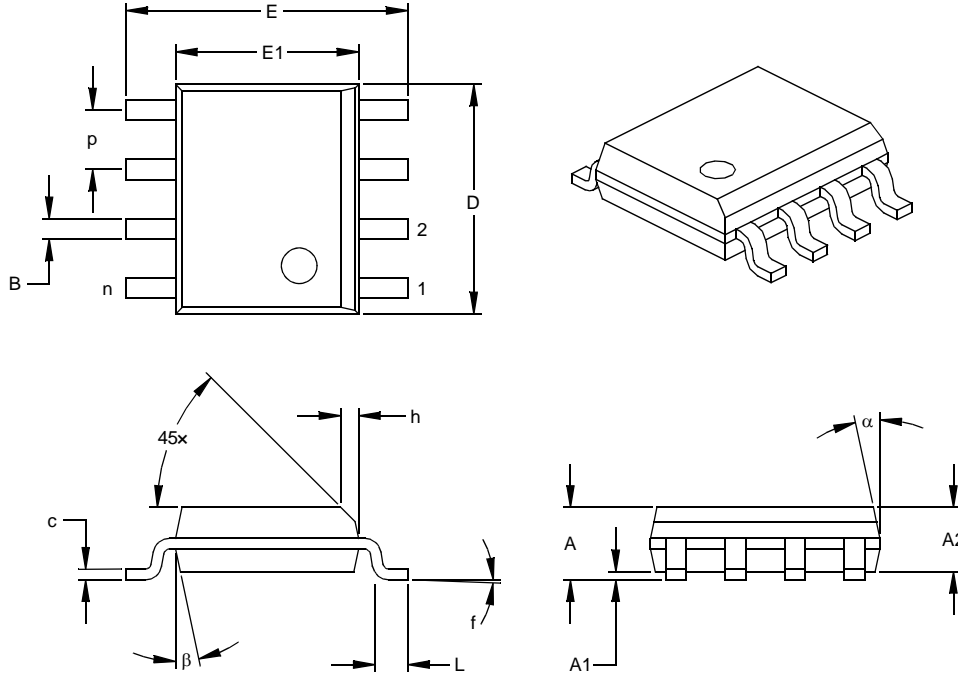
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
 § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
 JEDEC Equivalent: MS-012
 Drawing No. C04-057

APPENDIX A: REVISION HISTORY

Revision B

Added note to page 1 header (Not recommended for new designs).

Updated document format.

Revision C

Added a note to each package outline drawing.

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: <http://microchip.com/support>

93LC46/56/66

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

TO: Technical Publications Manager Total Pages Sent _____

RE: Reader Response

From: Name _____

Company _____

Address _____

City / State / ZIP / Country _____

Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? Y N

Device: 93LC46/56/66

Literature Number: DS21712C

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>	
Device	Temperature Range	Package	Pattern	
Device	93LC46:	1K 2.5V Microwire Serial EEPROM		
	93LC46X:	1K 2.5V Microwire Serial EEPROM in alternate pinouts (SN package only)		
	93LC46T:	1K 2.5V Microwire Serial EEPROM (Tape and Reel)		
	93LC46XT:	1K 2.5V Microwire Serial EEPROM (Tape and Reel)		
	93LC56:	2K 2.5V Microwire Serial EEPROM		
	93LC56X:	2K 2.5V Microwire Serial EEPROM in alternate pinouts (SN package only)		
	93LC56T:	2K 2.5V Microwire Serial EEPROM (Tape and Reel)		
	93LC56XT:	2K 2.5V Microwire Serial EEPROM (Tape and Reel)		
	93LC66:	4K 2.5V Microwire Serial EEPROM		
	93LC66X:	4K 2.5V Microwire Serial EEPROM in alternate pinouts (SN package only)		
	93LC66T:	4K 2.5V Microwire Serial EEPROM (Tape and Reel)		
	93LC66XT:	4K 2.5V Microwire Serial EEPROM (Tape and Reel)		
Temperature Range	I	= -40°C to +85°C		
Package	P	= Plastic DIP (300 mil body), 8-lead		
	SN	= Plastic SOIC (150 mil body), 8-lead		

Examples:

- a) 93LC46-I/P: 1K, 128x8 or 64x16 Serial EEPROM, PDIP package
- b) 93LC46-I/SN: 1K, 128x8 or 64x16 Serial EEPROM, SOIC package
- c) 93LC46T-I/SN: 1K, 128x8 or 64x16 Serial EEPROM, SOIC package, tape and reel
- d) 93LC46X-I/SN: 1K, 128x8 or 64x16 Serial EEPROM, Rotated SOIC package
- e) 93LC56-I/P: 2K, 256x8 or 128x16 Serial EEPROM, PDIP package
- f) 93LC56-I/SN: 2K, 256x8 or 128x16 Serial EEPROM, SOIC package
- g) 93LC56T-I/SN: 2K, 256x8 or 128x16 Serial EEPROM, SOIC package, tape and reel
- h) 93LC56X-I/SN: 2K, 256x8 or 128x16 Serial EEPROM, Rotated SOIC package
- i) 93LC66-I/P: 4K, 512x8 or 256x16 Serial EEPROM, PDIP package
- j) 93LC66-I/SN: 4K, 512x8 or 256x16 Serial EEPROM, SOIC package
- k) 93LC66T-I/SN: 4K, 512x8 or 256x16 Serial EEPROM, SOIC package, tape and reel
- l) 93LC66X-I/SN: 4K, 512x8 or 256x16 Serial EEPROM, Rotated SOIC package

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

93LC46/56/66

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniclient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. & KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2002-2012, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 9781620767337

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC[®] MCUs and dsPIC[®] DSCs, KEELOQ[®] code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Osaka
Tel: 81-66-152-7160
Fax: 81-66-152-9310

Japan - Yokohama
Tel: 81-45-471-6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

10/26/12