CL8801

Sequential Linear LED Driver

Features

- Minimal Component Count
  (Base Configuration: CL8801 + Four Resistors + Diode Bridge)
- No Magnetics, No Capacitors
- Up to 7.5W Output (13W with Heat Sink)
- >110 Lm/W using Efficient LEDs
- 85% Typical Electrical Efficiency
- >0.95 Power Factor
- <30% THD Line Current
- Low Conducted EMI without Filters
- 85% LED Luminous Utilization
- Phase Dimmer Compatible with an RC Network

Applications

- Fluorescent Tube Retrofit
- Incandescent and CFL Bulb Replacement
- General LED Lighting

General Description

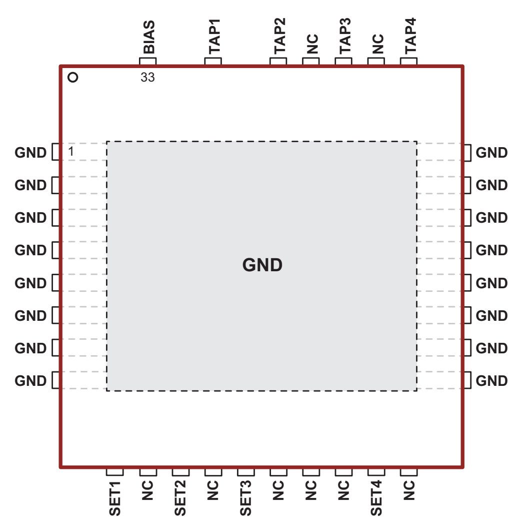
The CL8801 is designed to drive a long string of inexpensive, low-current LEDs directly from the AC mains. A basic driver circuit consists of CL8801, four resistors and a bridge rectifier. Two to four additional components are optional for various levels of transient protection. No capacitors, EMI filters or power factor correction circuits are needed.

A string of series/parallel LEDs is tapped at four locations. Four linear current regulators sink current at each tap and are sequentially turned on and off, thereby tracking the input sine wave voltage. Voltage across each regulator is minimized when conducting, providing high efficiency. Output current at each tap is individually resistor-adjustable. Cross-regulation, as the CL8801 switches from one regulator to another, provides smooth transitions. The current waveform can be tailored to optimize for input voltage range, line/load regulation, output power/current, efficiency, power factor, THD, dimmer compatibility and LED utilization.

With the addition of an RC network, the driver is compatible with phase dimming.

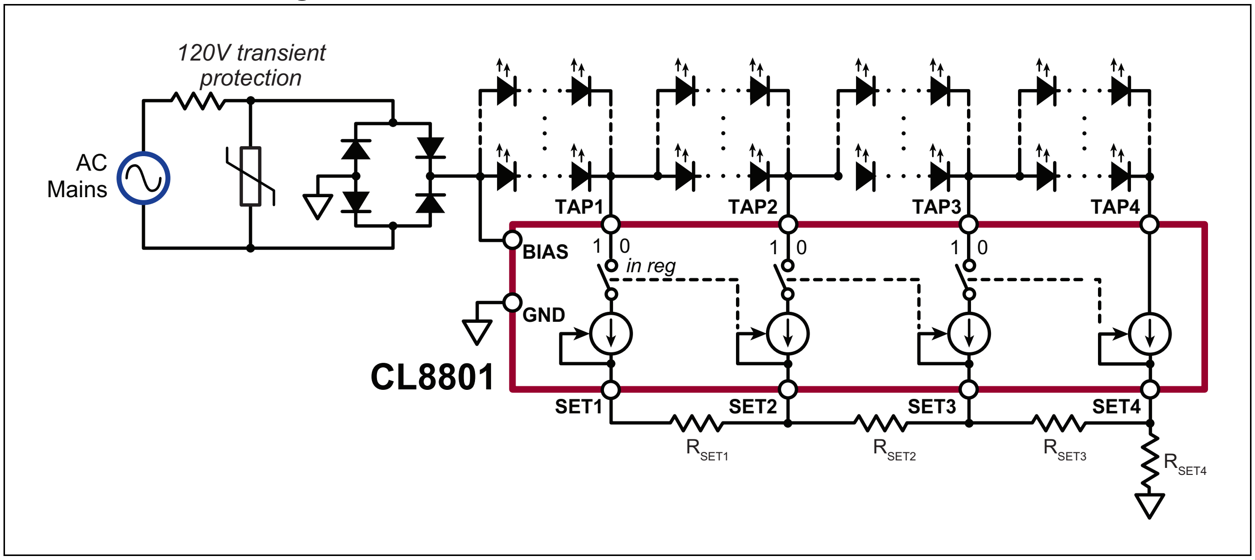
Package Type

33-lead QFN
(Top view)

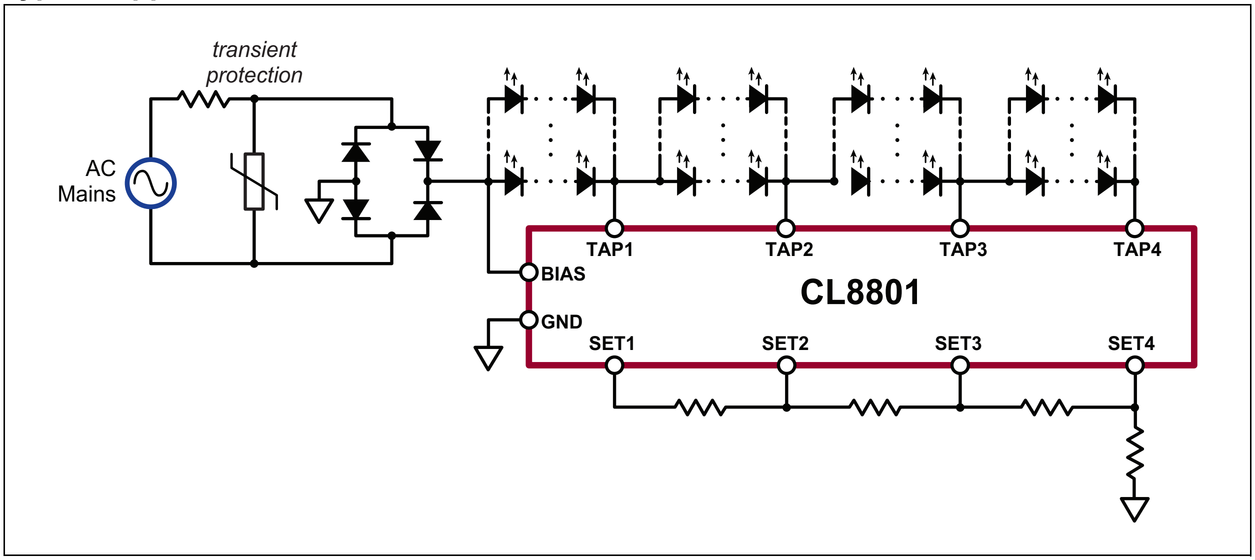


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{BIAS}, V_{TAP1} .... –0.5V to +550V
V_{TAP2-4} .... –0.5V to +320V
V_{SET1-4} 4V
Operating Junction Temperature, T_J .... –55°C to +125°C
Storage Temperature, T_S .... –65°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Electrical Specifications: All voltages with respect to GND pin

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
Output Current	TAP1	I_{OUT}	—	—	60	mA	
	TAP2		—	—	90		
	TAP3		—	—	200		
	TAP4		—	—	200		
Output Voltage	TAP1	V_{OUT}	—	—	400	V	Non-conducting
	TAP2–4		—	—	300		Non-conducting
	TAP1–4		—	—	Note 1		Conducting
Applied BIAS Voltage		V_{BIAS}	—	—	440	V	

Note 1: Voltage capability is determined by power dissipation (V x I).

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions at 25°C unless noted otherwise

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
BIAS Pin Input Current		I_{BIAS}	—	250	410	µA	V_{BIAS} = 170V
Output Current, On	TAP1	$I_{TAP(ON)}$	60	—	—	mA	V_{TAP1} = 30V, $V_{SET1–4}$ = GND
	TAP2		90	—	—		V_{TAP2} = 17V, $V_{SET1–4}$ = GND
	TAP3		200	—	—		V_{TAP3} = 17V, $V_{SET1–4}$ = GND
	TAP4		200	—	—		V_{TAP4} = 17V, $V_{SET1–4}$ = GND
Output Current, Off		$I_{TAP(OFF)}$	—	0	10	µA	Tap 1–3, V_{BIAS} = 170V
Regulation Voltage at SET Pins	SET1–3	V_{REG}	1.8	2	2.2	V	
	SET4		1.89	2.1	2.31	V	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	–55	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
33-Lead QFN	θ_{JA}	—	24	—	°C/W	**Note 1**
	θ_{JC}	—	2.5	—	°C/W	**Note 2**

Note 1: One oz Cu four-layer board, 3 x 4-inch PCB with thermal pad and thermal via array

2: Junction to exposed heat slug

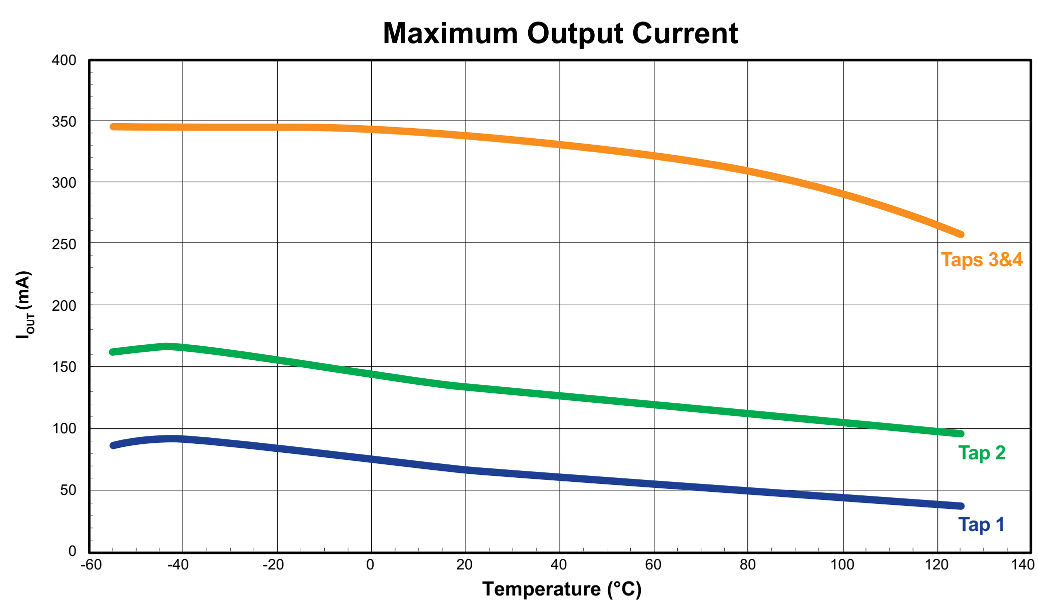


FIGURE 1-1: *Output Current Thermal Characteristics.*

2.0 PIN DESCRIPTION

The details on the pins of CL8801 are listed in Table 2-1. Refer to **Package Type** for the location of pins. The high-voltage pins are located on one side of the package and are arranged from lowest to highest voltage. Pin-to-pin voltage gradients are minimized.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1–8	GND	Circuit common. (Used for heat sink ground plane.)
9	SET1	Current sense for linear current regulators for each tap. Resistors on these pins set the tap currents.
10	NC	No internal connection
11	SET2	Current sense for linear current regulators for each tap. Resistors on these pins set the tap currents.
12	NC	No internal connection
13	SET3	Current sense for linear current regulators for each tap. Resistors on these pins set the tap currents.
14	NC	No internal connection
15	NC	No internal connection
16	NC	No internal connection
17	SET4	Current sense for linear current regulators for each tap. Resistors on these pins set the tap currents.
18	NC	No internal connection
19, 20	GND	Circuit common. (Used for heat sink ground plane.)
21	GND	Circuit common. (Used for heat sink ground plane.) Connect to bridge rectifier return.
22–26	GND	Circuit common. (Used for heat sink ground plane.)
27	TAP4	Current regulator outputs. Connect to taps along the LED string.
28	NC	No internal connection
29	TAP3	Current regulator outputs. Connect to taps along the LED string.
30	NC	No internal connection
31	TAP2	Current regulator outputs. Connect to taps along the LED string.
32	TAP1	Current regulator outputs. Connect to taps along the LED string.
33	BIAS	Provides bias for driver. Connect to rectified AC.
Underside Plate (GND)		For heat sinking purposes, it should be soldered to a 4 cm^2 exposed copper area. It should also be electrically connected to circuit common (GND).

3.0 APPLICATION INFORMATION

3.1 Overview

Designing a driver to meet particular requirements may be a difficult task considering the 16 design variables: tap current (4), number of series-connected LEDs per segment (4), and the number of parallel-connected LEDs per segment (4). Manually selecting values will provide light, but the chosen values may be far from optimal with regard to efficiency, LED utilization and line regulation.

In addition to configuring the driver, several circuits may be employed to increase reliability, performance and cost. The following sections briefly describe these circuits. For additional information and design assistance, contact your nearest Microchip field applications engineer.

3.2 Transient Protection

The driver circuits have no need for capacitors that could otherwise absorb transient energy nor is there a need for EMI filters that would block transients. Therefore, the full burden of transient protection is borne by the protection circuit. (See Figure 3-1.) The two-stage approach in the following schematics provides 2.5 kV protection, both pulse and ring per EN 61000-4-5 and EN 61000-4-12, six hits each. (See Figure 3-2.)

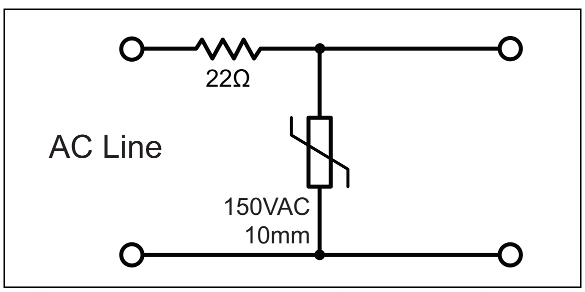


FIGURE 3-1: *100 VAC to 120 VAC Transient Protection.*

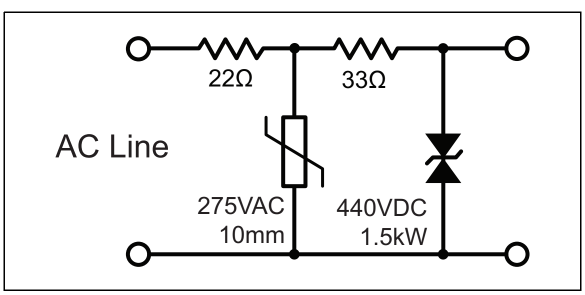


FIGURE 3-2: *230 VAC Transient Protection.*

3.3 Zener Diode Substitution

Zener diodes may be substituted for LEDs in the bottom stages of the design. The last one or two stages of LEDs contribute little to the light output—they are mainly present to offload the adjacent upstream regulator at high line voltages to minimize losses. The advantages of Zener substitution include minimizing unlit LEDs at low line for better light uniformity, better line regulation at high line, fewer LEDs for lower cost and less PCB area and fewer board-to-board connections. Disadvantages include slightly reduced efficiency at high line and additional heat load on the driver board.

3.4 Phase Dimming

As with any light load, the LED lamp might not draw enough current to ensure proper dimmer operation. This is especially true for 230 VAC dimmers. Triodes for Alternating Current (TRIAC) used in dimmers require a minimum latching current when triggered to place the TRIAC in the latched-on state. Once latched, a minimum holding current is required to maintain the TRIAC in the ON state. Latching current is many times greater than the holding current and is the main concern with dimmer compatibility.

Higher latching current can be provided by a simple series RC network across the AC line. A short time constant provides a current spike at the turn-on edge. (See Figure 3-3.)

Less common is inadequate holding current. The minimum dimmer holding current is typically 10 mA to 20 mA. Tap1 at 60 mA (maximum) exceeds the minimum.

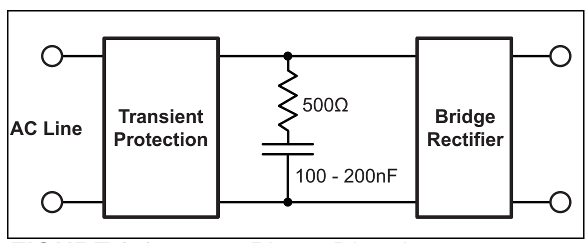


FIGURE 3-3: *Phase Dimming.*

3.5 Power Boost

Higher output power can be achieved by offloading a portion of the power dissipation from the CL8801 to external Field-Effect Transistors (FETs). The circuit in Figure 3-4 drops most of the tap voltage across the FETs, thereby shifting the bulk of the dissipation to the FETs.

3.6 Strobing

Twice per AC line cycle the line voltage crosses zero volts, during which time there is no light output.

The circuit in Figure 3-5 can provide 5% to10% valley fill. It has little effect on input current wave shape (THD, PF) and efficiency. This circuit is intended to prevent the output from reaching zero. It will not significantly reduce output ripple.

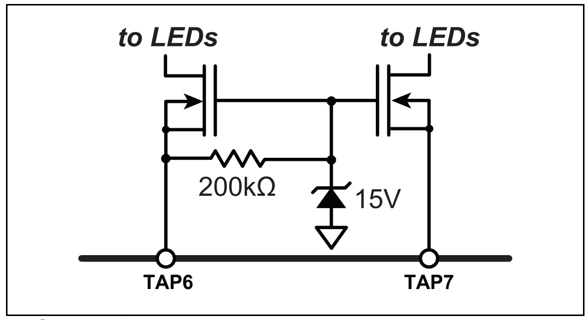


FIGURE 3-4: *Power Boost.*

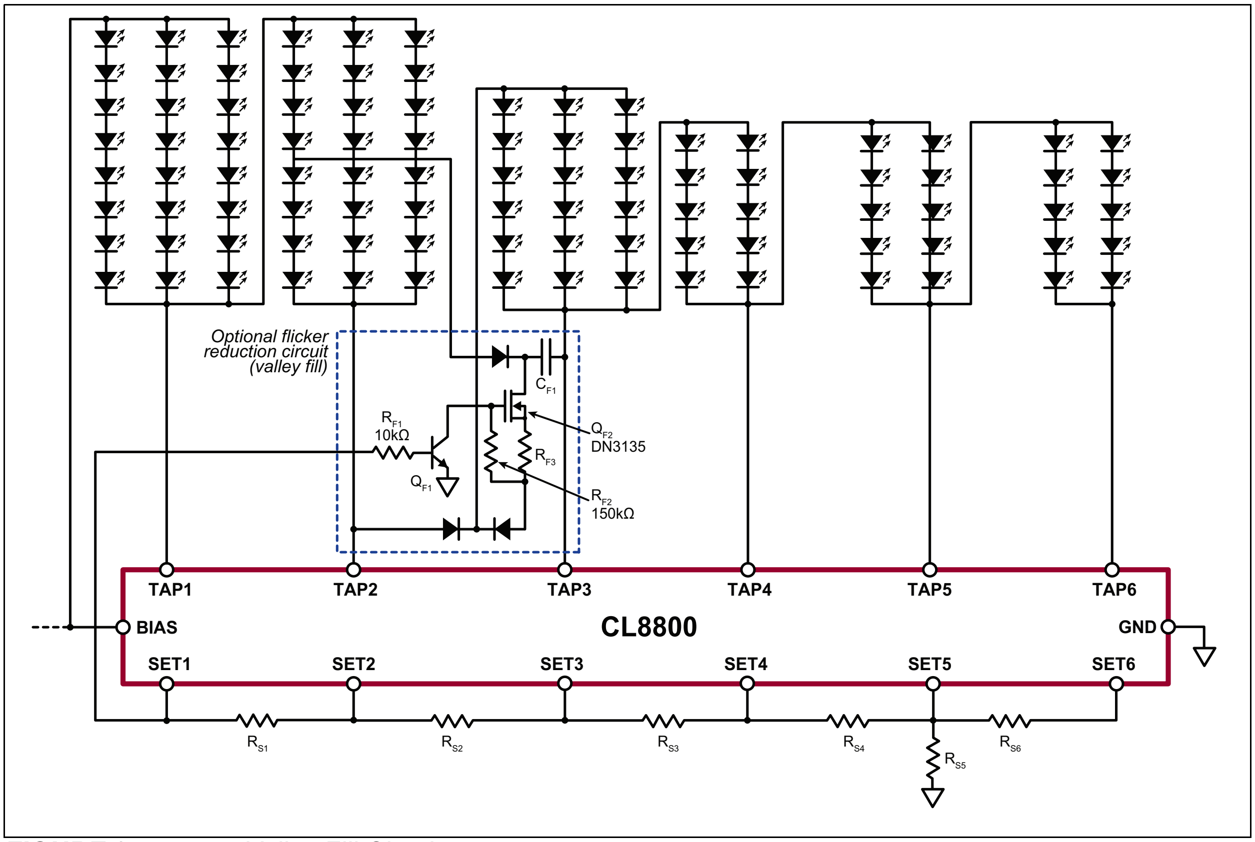


FIGURE 3-5: *Valley Fill Circuit.*

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

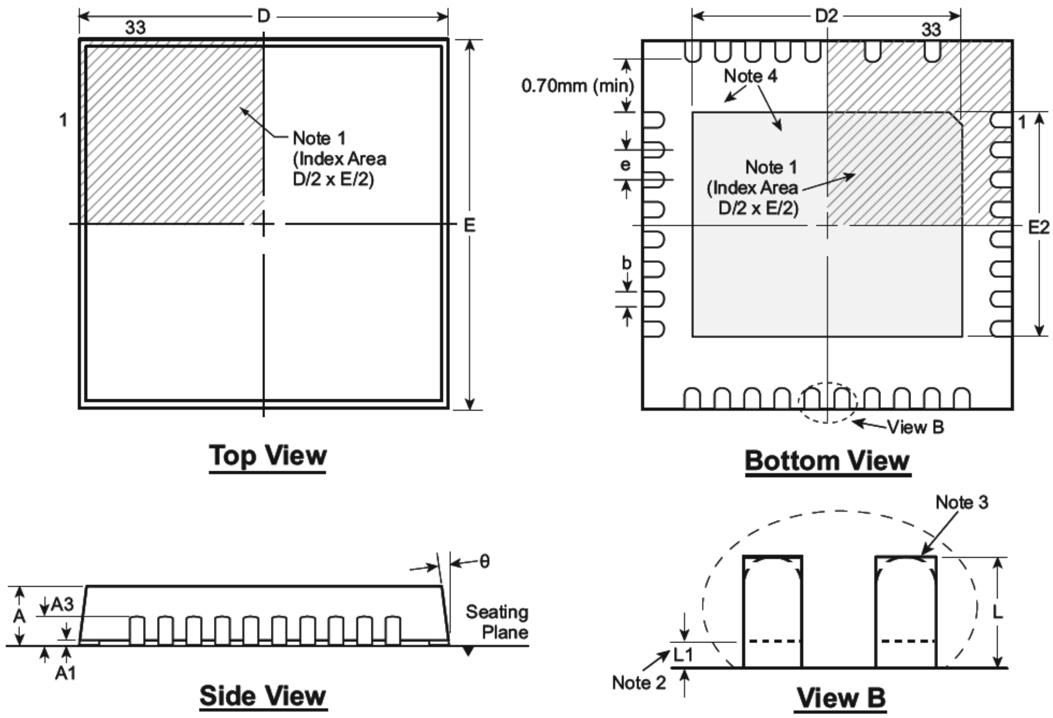
33-lead QFN	Example
●XXXXXXX XXXXXX(e3) YYWWNNN	●CL8801 K63(e3) 1749343

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or may not include the corporate logo.

33-Lead QFN Package Outline (K6)

6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*
4. *There will be an exposed DAP. A minimum of 0.7mm spacing will be maintained between the leads and the DAP.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ°
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	5.85	4.00	5.85	3.60	0.50 BSC	0.30	0.00	0
	NOM	0.90	0.02		0.25	6.00	4.15	6.00	3.75		0.40	-	-
	MAX	1.00	0.05		0.30	6.15	4.25	6.15	3.85		0.50	0.15	14

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (February 2017)

- Converted Supertex Doc# DSFP-CL8801 to Microchip DS20005601A
- Changed the quantity of the K6 M935 package from 2000/Reel to 3000/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	CL8801	=	Sequential Linear LED Driver (Base Configuration: CL8801 + 4 Resistors + Diode Bridge)
Package:	K6(3)	=	33-lead (6 x 6) QFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	490/Tray for a K6 Package
	M935	=	3000/Reel for a K6 Package

Examples:

a) CL8801K63-G: Sequential Linear LED Driver (Base Configuration: CL8801 + 4 Resistors + Diode Bridge), 33-lead QFN Package, 490/Tray

b) CL8801K63-G-M935: Sequential Linear LED Driver (Base Configuration: CL8801 + 4 Resistors + Diode Bridge), 33-lead QFN Package, 3000/Reel

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