24/48V Fan Driver/Controller With High-Side Drive

Features

- High-side drive allows use of tachs
- Direct interface to host controller
- Noise-immune linear speed control
- 4-bit digital speed control
- Operates from single +24/+48V supply
- Programmable PWM frequency
- Undervoltage lockout

Applications

- 24/48V chassis cooling tray
- Servers
- SAN equipment
- Cellular and fix wireless systems
- 24/48V PBX system
- Base stations

General Description

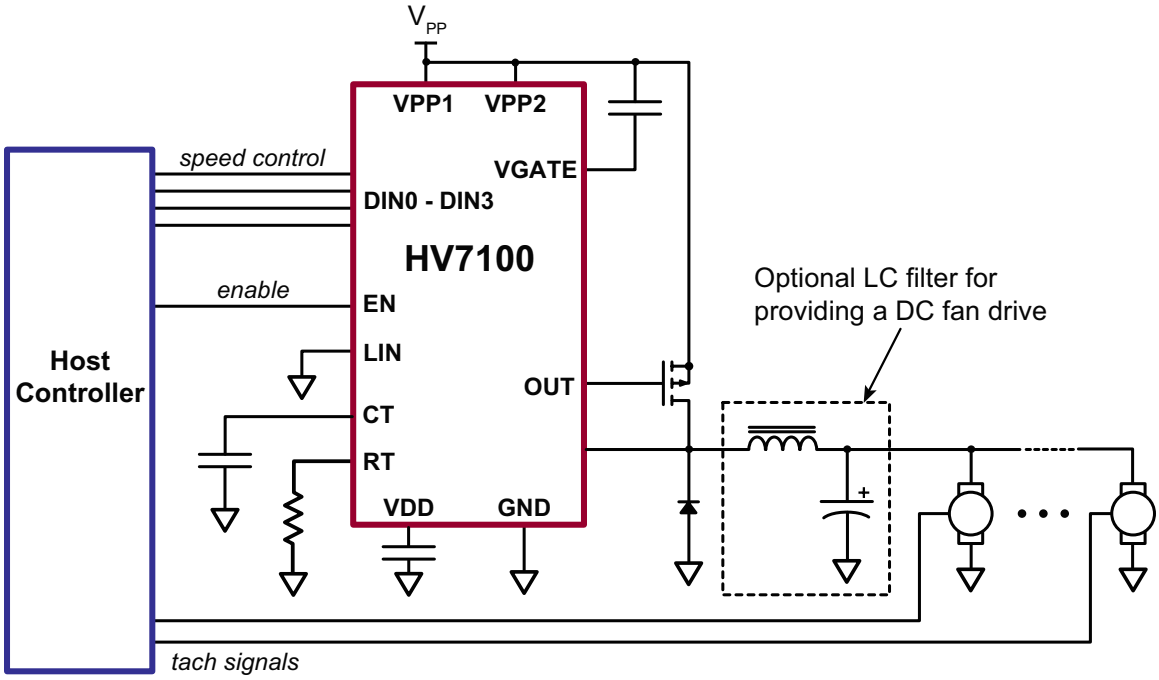
The HV7100 is an integrated PWM speed controller for driving 24 and 48VDC fans. The features and benefits provided by the HV7100 make driving fans simple and low cost. The HV7100 drives a high side external P-channel FET, allowing the use of fans having a ground-based tachometer signal. It has a wide input voltage range of +16 to +90V, ideal for +24 or +48V systems. No low voltage supply is needed.

A 4-bit digital control input provides direct interfacing with a micro controller or system processor to control the fan speed. It can also be used as a stand-alone fan controller, via a thermistor connection to the Linear Control pin.

The HV7100 has a wide PWM frequency range. When driving fans directly with a PWM supply voltage, frequency may be set low, around 50 - 120Hz. When used to drive fans requiring a DC supply, an LC filter may be employed. In this case, PWM frequency may be as high as 100kHz, reducing component sizes in the filter.

The HV7100 is an ideal device to incorporate in fan trays and fan control modules, as it reduces circuit complexity and minimizes parts count and overall cost for thermal management.

Typical Application Circuit



Ordering Information

Part Number	Package	Packing
HV7100NG-G	14-Lead SOIC (NB)	53/Tube
HV7100NG-G M903	14-Lead SOIC (NB)	2500/Reel

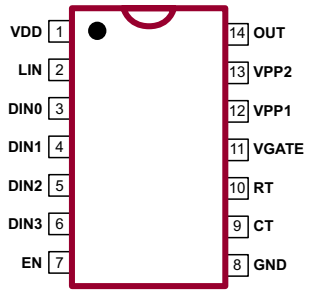
-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

Parameter	Value
V_{PP} to GND	-0.5V to 90V
V_{DD} to GND	-0.3V to +6V
Input voltage, LIN	-0.3V to (V_{DD} + 0.3V)
Input voltage, $D_{IN}0$ - $D_{IN}2$	-0.3V to (V_{DD} + 0.3V)
Gate to V_{PP}	+0.5V to -15V
Continuous power dissipation (T_A = +25°C)	750mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

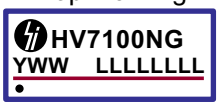
Pin Configuration



14-Lead SOIC
(top view)

Product Marking

Top Marking



Bottom Marking

Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
____ = "Green" Packaging

**May be part of top marking*

Package may or may not include the following marks: Si or

14-Lead SOIC

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units
V_{DD}	Externally applied V_{DD}	3.7	-	5.5	V
V_{PP}	High voltage supply	16	-	75	V
f_{OSC}	Oscillator frequency	50	-	100	kHz
R_T	Oscillator timing resistor	12	-	500	kΩ

Typical Thermal Resistance

Package	θ_{ja}
44-Lead PLCC	37°C/W

Electrical Characteristics

(Operating specifications are at T_A = 25°C, V_{PP} = 16 to 75V, V_{DD} = 3.0 to 5.5V, unless otherwise noted)

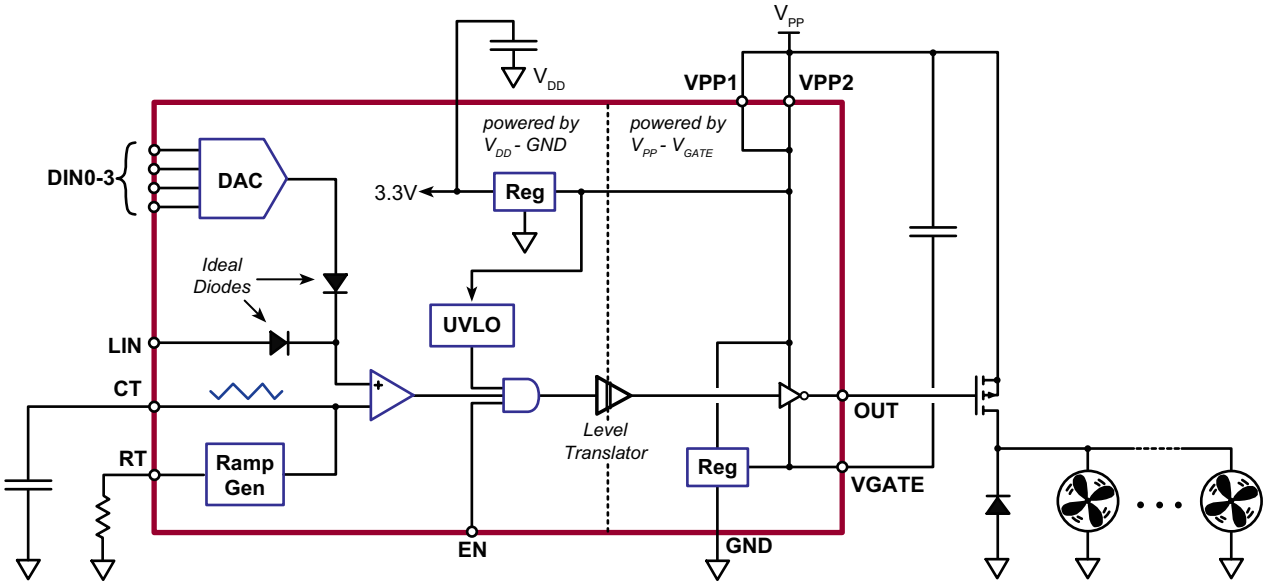
Sym	Parameter	Min	Typ	Max	Units	Conditions
Supplies						
I_{PP}	V_{PP} supply current	-	-	4.0	mA	No ext load on V_{DD}, f_{OSC} = 50kHz, 250pF on OUT pin
$UV_{PP(ON)}$	V_{PP} UVLO turn-on threshold	11.7	13.0	14.3	V	---
$UV_{PP(HYS)}$	V_{PP} UVLO hysteresis	1.5	2.0	2.5	V	---
V_{DD}	V_{DD} internal regulation	3.0	3.3	3.6	V	V_{PP} = 16V to 75V

Electrical Characteristics *(cont.)*

(Operating specifications are at T_A = 25°C, V_{PP} = 16 to 75V, V_{DD} = 3.0 to 5.5V, unless otherwise noted)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{DD(INT)}$	V_{DD} supply current	-	-	2.0	mA	External applied V_{DD} = 5.0V, f_{OSC} = 50kHz
$I_{DD(EXT)}$	Current available from internal V_{DD} regulator for external circuitry	-	-	2.0	mA	ΔV_{DD}<200mV
Gate Driver						
V_{GATE}	Gate regulator output voltage	-10.2	-12	-13.8	V	Referenced to V_{PP}
V_{OUTH}	Gate drive output voltage high	-10.2	-12	-13.8	V	Referenced to V_{PP}, Test current = 15mA
V_{OUTL}	Gate drive output voltage low	0	-	-0.8	V	
R_{SRC}	Pull-up resistance	-	-	25	Ω	Test Current = 15mA
R_{SINK}	Pull-down resistance	-	-	25	Ω	Test Current = -15mA
t_{RISE}	Rise time	-	-	100	ns	C_{LOAD} = 250pF
t_{FALL}	Fall time	-	-	100	ns	C_{LOAD} = 250pF
Oscillator						
f_{OSC}	Oscillator frequency	51	60	69	Hz	C_T = 100nF, R_T = 43.0kΩ
f_{OSC}	Oscillator frequency	34	40	46	kHz	C_T = 330pF, R_T = 19.5kΩ
Logic and Linear Inputs						
V_{DIN0-3}(hi), V_{EN}(hi)	Logic input voltage, high	0.7 x V_{DD}	-	-	V	---
V_{DIN0-3}(lo), V_{EN}(lo)	Logic input voltage, low	-	-	0.3 x V_{DD}	V	---
$T_{EN(ON)}$	Enable to gate turn on delay	0	-	150	ns	LIN = V_{DD}, D_{IN}0 - D_{IN}3 = 1111
$T_{EN(OFF)}$	Enable to gate turn off delay	0	-	150	ns	LIN = V_{DD}, D_{IN}0 - D_{IN}3 = 1111
I_{DIN0-3}	Digital input pull down resistance	200	330	460	kΩ	---
I_{LIN}	Linear control input current	-1.0	-	1.0	uA	-40C to +85C
Duty Cycle						
D	Duty cycle	16	20	24	%	V_{LIN} = 0.9V, D_{IN} = 0000
D	Duty cycle	75	80	85	%	V_{LIN} = 2.1V, D_{IN} = 0000
D	Duty cycle	16	20	24	%	V_{LIN} = 0V, D_{IN} = 0011
D	Duty cycle	75	80	85	%	V_{LIN} = 0V, D_{IN} = 1100
D	Duty cycle	-	-	0	%	V_{LIN} = 0V, D_{IN} = 0000
D	Duty cycle	100	-	-	%	V_{LIN} = 0V, D_{IN} = 1111

Functional Block Diagram



Functional Description

The HV7100 requires a single +16 to +75V supply to bias its internal circuitry. It internally generates 3.3V for V_{DD}, and -12V relative to V_{PP} for driving the external P-channel MOSFET. If an external V_{DD} is applied (greater than 3.6V but less than 5.5V), the internal regulator will shut off. The HV7100 drives an external P-channel FET to drive the 24V/48V DC fan.

An external diode, connected across the fan terminals, is required to clamp the voltage across the fan to a diode drop during the off period.

Pulse Width Modulator

The PWM circuit compares the internal triangle wave oscillator (0.5 – 2.5V pk-pk) with the linear control voltage or the DAC output. Its output is a square-wave PWM signal with duty cycle ranging from 0% to 100%.

When an external PWM signal is applied to the Enable input and the internal PWM generator is not needed, R_T and LIN should be connected to V_{DD} and C_T connected to GND.

Oscillator

A capacitor connected between the C_T and GND sets the frequency of the internal triangular frequency oscillator in conjunction with the timing resistor R_T. R_T sets the charge/discharge current into and out of C_T.

The frequency is determined by the following equation:

$$f = \frac{(0.258)}{(R_T \times C_T)}$$

P-Channel Gate Driver

The PWM output of the comparator circuit is level translated and is the input to the gate drive circuit. The gate drive circuit turns an external P-channel FET on and off by applying -12V and 0V (reference to V_{PP}), respectively, between its gate and source. The -12V supply to the gate drive circuit is generated internally from V_{PP}.

Enable

The EN pin directly controls the gate drive circuit. Pulling this pin to logic ground applies 0V to the external P-channel gate to turn it off. Applying a logic HIGH signal or pulling the voltage to V_{DD} resumes the switching cycle of the PWM signal.

Speed Control

The fan speed can be controlled in three ways:

Linear Control - Applying a DC voltage between 0.5V to 2.5V to the LIN pin varies the duty cycle of the voltage driving the fans from 0% to 100% according to:

$$D = \frac{V_{LIN}}{2} - 0.25$$

Linear control voltage below 0.5V will turn off the fan completely (0% duty cycle), while voltage greater than 2.5V will fully turn the fan on (100% duty cycle).

When using linear control mode, DIN0 – DIN3 should be set to logic 0. If desired, DIN may be used to set a lower limit on the fan speed. This input is immune to moderate noise on the control signal.

Digital Control - Applying logic signals to the DIN0 – DIN3 pins sets the duty cycle of the output. 0000 = 0% and 1111 = 100%. See Table 1 for details. In digital control mode, LIN should be set to 0V. DIN0 – DIN3 pins have internal pull downs so that the DAC output will default to 0V when it is not used.

External PWM - An external PWM signal can be applied to the Enable pin to directly control the duty cycle. A logic 0 turns the transistor off, and a logic 1 turns it on. When using this control method, connect DIN0 – DIN3, LIN, and R_T to V_{DD}. Connect C_T to GND.

The DAC output and the Linear Control signals are OR'd together. Whichever has the higher value dominates. This allows an analog temperature sensing circuit to override the digital inputs (DIN0 – DIN3) for added system protection.

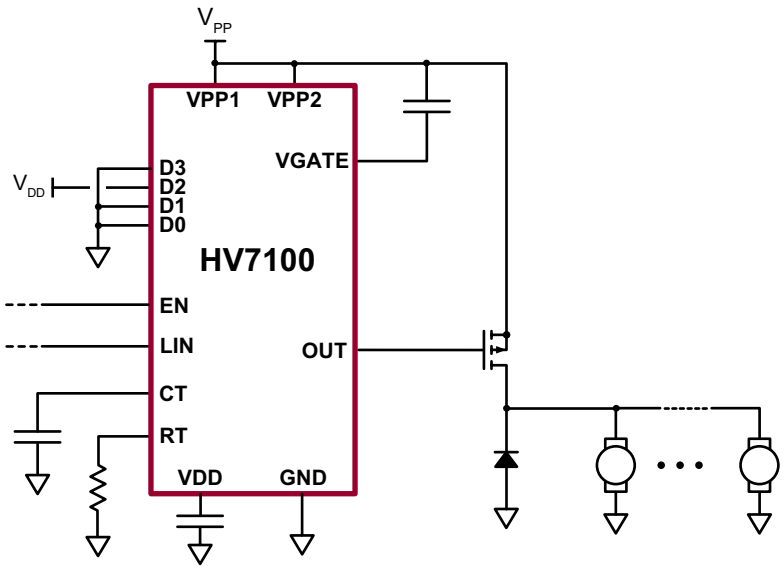
The following table illustrates the correlation between the digital inputs and LIN voltage to the PWM duty cycle.

Table 1. DAC signal and LIN voltage to Duty Cycle Programming.

DIN3	DIN2	DIN1	DIN0	LIN	Gate Drive Duty Cycle
0	0	0	0	0.500V	0%*
0	0	0	1	0.633V	6.7%
0	0	1	0	0.766V	13.3%
0	0	1	1	0.900V	20.0%
0	1	0	0	1.033V	26.7%
0	1	0	1	1.167V	33.3%
0	1	1	0	1.300V	40.0%
0	1	1	1	1.433V	46.7%
1	0	0	0	1.567V	53.3%
1	0	0	1	1.700V	60.0%
1	0	1	0	1.833V	66.7%
1	0	1	1	1.967V	73.3%
1	1	0	0	2.100V	80.0%
1	1	0	1	2.233V	86.7%
1	1	1	0	2.367V	93.3%
1	1	1	1	2.500V	100%*

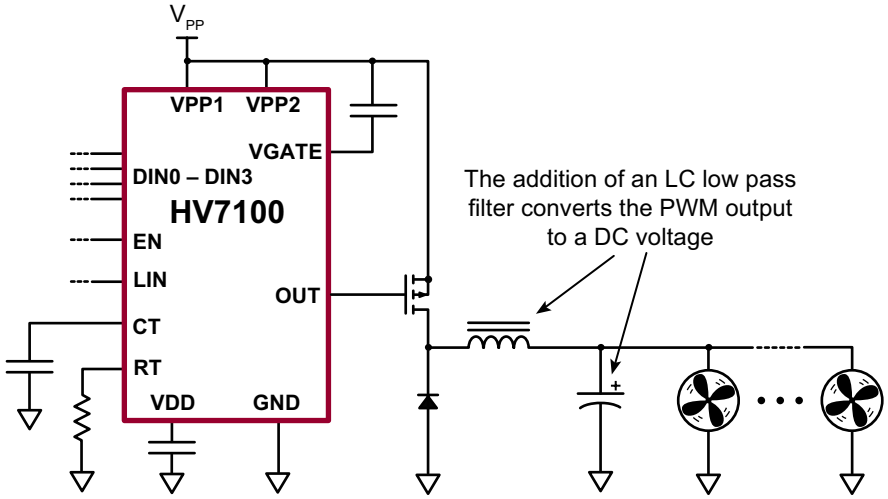
** Guaranteed 0% @ 0000 and 100% @ 1111*

PWM Fan Drive



When using direct PWM drive to the fans, it is best to set a low PWM frequency, in the range of 50Hz -120Hz.

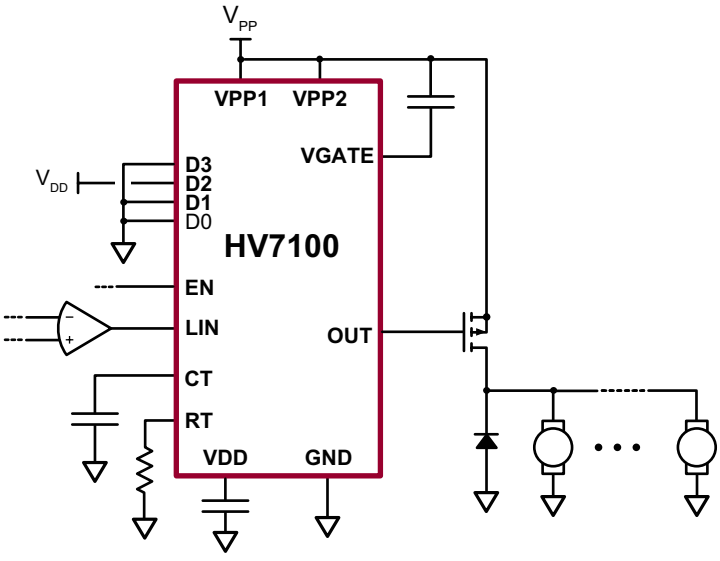
DC Fan Drive



The HV7100 controls the fans with a PWM supply voltage. However, some fans require a steady DC voltage for proper operation. In order for these fans to function properly, an LC low pass filter should be added to cancel the PWM output to a steady DC voltage.

The LC filter also provides another advantage. Some fans draw large spikes of current during start-up and/or during normal operation. Without the LC filter, these current spikes would be drawn directly from the +24 or +48V supply, causing potential conducted EMI problems. The LC filter prevents these spikes from occuring and/or reaching the +24 or +48V supply.

Setting a Lower Speed Limit



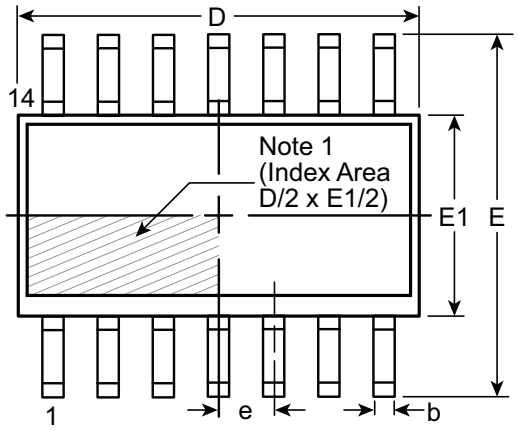
When using the linear control input, the digital control inputs may be used to set a lower limit on the duty cycle. This is based on the fact that the higher control setting, linear or digital, dominates. In the example above, duty cycle is prevented from falling below 25% even if the linear control signal goes to 0V.

Pin Description

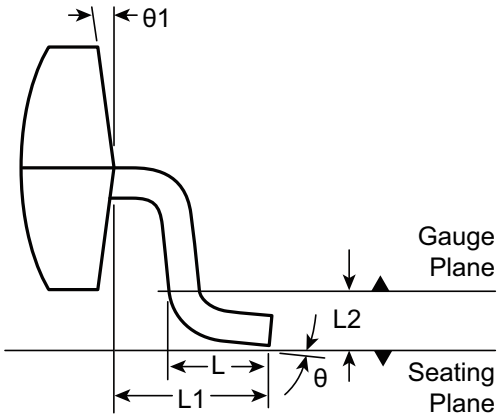
Pin #	Function	Description
1	VDD	Output of an internal linear voltage regulator, which in turn is powered by V_{PP}. It provides power to the internal low-side (ground referenced) circuitry. An external voltage may be applied to this pin, provided it is higher than 3.6V but less than 5.5V. Bypass this pin with a 100nF ceramic capacitor to ground.
2	LIN	A DC voltage ranging from 0.5 to 2.5V sets the duty cycle of the gate output from 0% to 100%. This input is immune to moderate noise on the control signal.
3	DIN0	Applying 0000 to 1111 to these logic input pins sets the duty cycle of the gate output from 0 to 100%. A 1-bit increment is equal to 6.67% increment in duty cycle. See Table 1 on page 5.
4	DIN1	
5	DIN2	
6	DIN3	
7	EN	Enable input. A logic high applied to this input enables the output.
8	GND	Ground return for all the internal circuitry. This pin must be electrically connected to the ground of the power train and logic return.
9	CT	In conjunction with RT, a capacitor from this pin to ground sets PWM frequency. A triangle wave appears on this pin, with an amplitude of 0.5 - 2.5V and at the PWM frequency.
10	RT	In conjunction with CT, a resistor from this pin to ground sets PWM frequency.
11	VGATE	This is the output pin of the internal linear regulator that biases the gate drive circuit. Bypass with 100nF ceramic capacitor to VPP.
12	VPP1	Supply voltage pins. Both must be connected to the supply voltage (+24V/+48V). Connect together as close as possible to the IC. Bypass locally with a ceramic capacitor to ground.
13	VPP2	
14	OUT	This pin is the output gate driver for an external P-channel power MOSFET.

14-Lead SOIC (Narrow Body) Package Outline (NG)

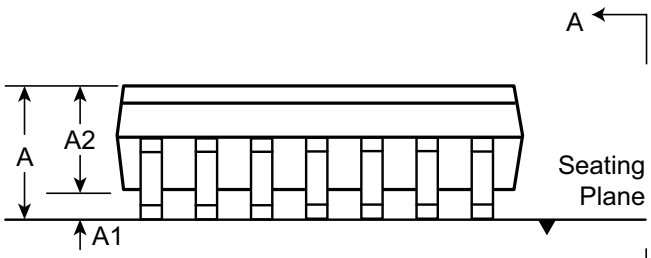
8.65x3.90mm body, 1.75mm height (max), 1.27mm pitch



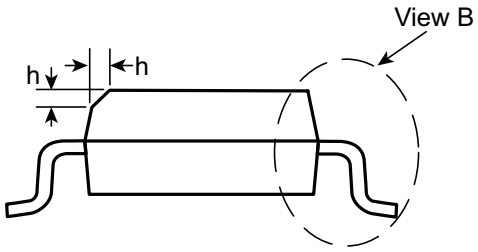
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	8.55*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	8.65	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	8.75*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AB, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-14SOICNG, Version F041309.*

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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