

SSC7150

Motion Coprocessor

Product Features

- · High Performance 32-bit Embedded Controller
- Low power 7.65mA (typ) in active mode
- System in deep sleep consumes 70µA (typ)
- 3.3-Volt I/O
- Package
 - 6mm x 6mm, 28-pin QFN

Sensor Firmware

- Sensor fusion firmware features include:
 - Self-contained 9-axis sensor fusion
 - Sensor data pass-through
 - Fast in-use background calibration of all sensors and calibration monitor
 - Magnetic immunity: Enhanced magnetic distortion detection and suppression
 - Gyroscope drift cancellation
- Easy to implement complete turnkey sensor fusion solution
- Sensor power management
- Sensors Supported
 - Bosch BMC150 Geomagnetic Sensor/Accelerometer
 - Bosch BMG160 Gyroscope

Hardware Features

The hardware features in the SSC7150 motion coprocessor include the following:

- Two I²C Controllers
 - Supports I²C bus speeds to 400kHz
 - Host Interface Supports Slave Operation
 - Sensor Interface Supports Master Operation
- · Low Power Modes

Target Markets

- · Remote Controls, Gaming
- Fitness Monitoring
- · Internet of Things Applications

Description

The SSC7150 motion coprocessor is a low-power, flexible, turnkey solution. SSC7150 makes implementing sensor fusion easy for motion-based embedded applications. Microchip created this solution, enabling faster time to market without the need for sensor-fusion expertise. The SSC7150 is extremely efficient. Low average current while running complex sensor-fusion algorithms results in lower power consumption for multiple applications.

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1.0 PIN CONFIGURATION

1.1 Description

The Pin Configuration chapter includes a Pin Diagram, Pin List, Pin Description and Package Details.

1.2 Terminology and Symbols for Pins/Buffers

Term	Definition
#	The '#' sign at the end of a signal name indicates an active-low signal.

1.3 Pin Diagram

FIGURE 1-1: 28 PIN QFN PIN DIAGRAM



Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

1.4 Pin List

The Pin List is shown in Table 1-1.

TABLE 1-1: SSC7150 28 QFN PIN CONFIGURATION

28 QFN	
Number	Pin Name
1	NC
2	NC
3	I2C_DA2
4	I2C_CL2
5	VSS
6	NC
7	I2C_D2_WAKE#
8	I2C2_WAKE
9	VSENSOR_EN
10	VDD
11	NC
12	VSS
13	I2C2_ALERT#
14	I2C_CL1
15	I2C_DA1
16	VSS
17	VCAP
18	NC
19	NC
20	VDD
21	NC
22	VSS
23	NC
24	AVSS
25	AVDD
26	MCLR#
27	I2C2_RESET#
28	NC

1.4.1 FIVE VOLT TOLERANT PINS

Table 1-2 lists the 5 Volt tolerant pins in the SSC7150. All other pins in the device are 3.3V only.

TABLE 1-2: 5V-TOLERANT PINS

Pin Number	Pin Name
13	I2C2_ALERT#
14	I2C_CL1
15	I2C_DA1
26	MCLR#

1.5 Pin Description

1.5.1 OVERVIEW

The following tables describe the signal functions in the SSC7150 pin configuration. See Section 1.6, "Notes for Tables in this Chapter," on page 7 for notes that are referenced in the Pin Description tables.

1.5.2 HOST INTERFACE

The SSC7150 can be used with an I^2C host interface. The pins required for each interface are shown in Table 1-3 and Table 1-4. See the associated Notes for board connection information for the unused interface.

TABLE 1-3: I²C HOST INTERFACE

I2C Interface Signals	5		
Pin Ref. Number	Signal Name	Description	Notes
4	I2C_CL2	I2C Controller Clock to Host Interface	
3	I2C_DA2	I2C Controller Data to Host Interface	
		Alert Interrupt signal from motion coprocessor	
13	12C2 ALEDT#	to Host. Used to tell Host data from motion	
15	12C2_ALERT#	coprocessor is ready to be sent out. Active low	
		output.	
	I2C_D2_WAKE#	Used to wake the motion coprocessor from a	
7		low power state due to host I2C	
1		communication. Active low input. Connect to	
		I2C_DA2.	
		Used to wake motion coprocessor from a Sleep	
8	I2C2_WAKE	state. This signal must be driven high at least	
		11ms prior to sending any I2C traffic to the	
		motion coprocessor. Active high input.	
27	12C2 DESET#	Reset input. Used to reset the host I2C	
21		interface.	

1.5.3 I²C SENSOR INTERFACE

TABLE 1-4: I²C SENSOR INTERFACE

I2C Sensor Interface			
Pin Ref. Number	Signal Name	Description	Notes
14	I2C_CL1	I2C Controller Clock to Sensor Interface	
15	I2C_DA1	I2C Controller Data to Sensor Interface	

1.5.4 MISCELLANEOUS FUNCTIONS

TABLE 1-5: MISCELLANEOUS FUNCTIONS

Miscellaneous Functions			
Pin Ref. Number Signal Name		Description	Notes
26	MCLR#	Master Clear (Reset) Input	Note 1
9	VSENSOR_EN	Sensor voltage switch control output.	
1, 2, 6, 11, 18, 19, 21,	NC	Pins labelled NC should be left unconnected on	
23, 28	NC	the board	

1.5.5 POWER INTERFACE

TABLE 1-6: POWER INTERFACE

Power Interface			
Pin Ref. Number	Signal Name	Description	Notes
17	VCAP	Internal Voltage Regulator Capacitor	Note 2
10, 20	VDD	VDD supply	
5, 12, 16, 22	VSS	VDD associated ground	
25	AVDD	AVDD supply	
24	AVSS	AVDD associated ground	

1.6 Notes for Tables in this Chapter

Note 1	A pull-up to VDD is required on the MCLR# pin. Use a 10K ohm pull-up resistor.
Note 2	A low-ESR (1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage
	regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at
	least a 6V rating, connected to ground. The type can be ceramic or tantalum.

1.7 Package Details

This section provides the technical details of the packages.

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	Units		MILLIMETERS		
Dimensior	n Limits	MIN	NOM	MAX	
Number of Pins	Ν		28		
Pitch	е		0.65 BSC		
Overall Height	Α	0.80	0.90	1.00	
Standoff	A1	0.00 0.02 0.05		0.05	
Contact Thickness	A3	0.20 REF			
Overall Width	E	6.00 BSC			
Exposed Pad Width	E2	3.65 3.70 4.20			
Overall Length	D	6.00 BSC			
Exposed Pad Length	D2	3.65 3.70 4.20			
Contact Width	b	0.23 0.30 0.35		0.35	
Contact Length	L	0.50 0.55 0.70			
Contact-to-Exposed Pad	К	0.20 – –			

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2	4.25		4.25
Contact Pad Spacing	C1	5.70		
Contact Pad Spacing	C2	5.70		
Contact Pad Width (X28)	X1	0.37		0.37
Contact Pad Length (X28) Y1				1.00
Distance Between Pads	G 0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

2.0 SYSTEM BLOCK DIAGRAM

The SSC7150 system block diagram is shown in Figure 2-1.

FIGURE 2-1: SSC7150 SYSTEM BLOCK DIAGRAM



3.0 GUIDELINES FOR GETTING STARTED

3.1 Basic Connection Requirements

Getting started with the SSC7150 requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see Section 3.2 "Decoupling Capacitors")
- All AVDD and AVSS pins, even if the ADC module is not used (see Section 3.2 "Decoupling Capacitors"). Note that there is no ADC support in this device. See Note below.
- VCAP pin (see Section 3.3 "Capacitor on Internal Voltage Regulator (Vcap)")
- MCLR# pin (see Section 3.4 "Master Clear (MCLR#) Pin")

Note: The AVDD and AVss pins must be connected, regardless of ADC use and the ADC voltage reference source.

Refer to the following schematic for connection information:

SSC7150 Sensor Hub Module, Assy. 6753, Schematic Revision 1.4.

3.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 3-1.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high frequency noise: If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μ F in parallel with 0.001 μ F.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.





3.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 μ F to 47 μ F. This capacitor should be located as close to the device as possible.

3.3 Capacitor on Internal Voltage Regulator (VCAP)

3.3.1 INTERNAL REGULATOR MODE

A low-ESR (1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **Section 4.0 "Electrical Characteristics**" for additional information on CEFC specifications.

3.4 Master Clear (MCLR#) Pin

The MCLR# pin is the Device Reset pin. Pulling the MCLR# pin low generates a device Reset. Figure 3-2 illustrates a typical MCLR# circuit.





- MCLR# from the external capacitor C, in the event of MCLR# pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).
- 2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

4.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the SSC7150 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the SSC7150 devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias	40°C to +85°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss (Note 3)	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD $\ge 2.3V$ (Note 3)	0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 2.3V (Note 3)	0.3V to +3.6V
Maximum current out of Vss pin(s)	300 mA
Maximum current into VDD pin(s) (Note 2)	300 mA
Maximum output current sunk by any I/O pin	15 mA
Maximum output current sourced by any I/O pin	15 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports (Note 2)	200 mA

Note 1: Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 4-1).

3: See the "Pin List" section for the 5V tolerant pins.

4.1 DC Characteristics

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – S IOH) I/O Pin Power Dissipation: I/O = S (({VDD – VOH} x IOH) + S (VOL x IOL))	PD		Pint + Pi/c)	W
Maximum Allowed Power Dissipation	PDMAX	(Tj — Ta)/θj	A	W

TABLE 4-2: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 28-pin QFN	θJA	35	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

TABLE 4-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHAF	RACTERIS	STICS	Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$				
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Conditions
Operating	Voltage						
DC10	Vdd	Supply Voltage (Note 2)	2.3		3.6	V	_
DC12	Vdr	RAM Data Retention Voltage (Note 1)	1.75	_		V	_
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	1.75	_	2.1	V	_
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.00005		0.115	V/µs	_

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. Refer to parameter BO10 in Table 4-7 for BOR values.

TABLE 4-4: DC CHARACTERISTICS: OPERATING/POWER-DOWN CURRENT

DC CHARA	CTERIST	ICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$					
Parameter No.	Symbol	Typical ⁽³⁾	Max.	Units	Conditions				
Operating/F	ower-Dow	n Current (N	ote 1, 2)	•					
DC20	IPEAK	19.5	20.0	mA	—				
DC30	IACTIVE	7.65	7.90	mA	—				
DC40	IIDLE	1.77	1.95	mA	—				
DC50	IPD	70	150	μA	—				

Note 1: A device's supply current is mainly a function of the operating voltage and frequency, as well as temperature.

2: The current measurements are as follows:

• Peak current (IPEAK):

This is the peak active current value when a sensor is actively providing environmental changes.

• Active current (IACTIVE):

This is the average operating current value when a sensor is actively providing environmental changes.

• Idle current (IIDLE):

This is the average idle current value when no sensor is actively providing environmental changes (and the device is not in power-down mode).

- Power-Down current (IPD):
 - This is the current value when the device is in power-down mode. This is the state entered when the Host issues the SET_POWER (Sleep) Command.
 - Wakeup from power-down mode requires the I2C2_WAKE pin.
- **3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

DC CHA	RACTER	ISTICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature-40°C \leq TA \leq +85°C					
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions	
	VIL	Input Low Voltage						
DI10		I/O Pins	Vss	_	0.2 Vdd	V		
DI18		I2C_DAx, I2C_CLx	Vss	_	0.3 Vdd	V	I ² C disabled (Note 4)	
DI19		I2C_DAx, I2C_CLx	Vss	_	0.8	V	l ² C enabled (Note 4)	
	Vih	Input High Voltage						
DI20		I/O Pins not 5V-tolerant ⁽⁵⁾	0.65 VDD	_	Vdd	V	(Note 4,6)	
		I/O Pins 5V-tolerant ⁽⁵⁾	0.65 VDD	_	5.5	V		
DI28		I2C_DAx, I2C_CLx	0.65 VDD	_	5.5	V	I ² C disabled (Note 4,6)	
DI29		I2C_DAx, I2C_CLx	2.1	_	5.5	V	I ² C enabled, 2.3V ≤ VPIN ≤ 5.5 (Note 4,6)	
	lı∟	Input Leakage Current (Note 3)						
DI50		I/O Ports	_	_	<u>+</u> 1	μA	$Vss \le VPIN \le VDD$, Pin at high-imped- ance	
DI55		MCLR# ⁽²⁾	—	_	<u>+</u> 1	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$	

TABLE 4-5: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR# pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- **3:** Negative current is defined as current sourced by the pin.
- 4: This parameter is characterized, but not tested in manufacturing.
- 5: See the "Pin List" section for the 5V-tolerant pins.
- **6:** The VIH specifications are only in relation to externally applied inputs, and not with respect to the userselectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the device are provided to be recognized only as a logic "high" internally to the device. For External "input" logic inputs that require a pull-up source, to ensure the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the device.

TABLE 4-6: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHA	RACTERI	STICS	Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$				
Param.	Symbol	Characteristic	Min. Typ. Max. Units				Conditions
DO10	Vol	Output Low Voltage	—	—	0.4	V	$IOL \le 10 \text{ mA}, \text{VDD} = 3.3 \text{V}$
		I/O Pins					
DO20	Vон	Output High Voltage	1.5 ⁽¹⁾	—	—	V	ІОН ≥ -14 mA, VDD = 3.3V
		I/O Pins	2.0 ⁽¹⁾	—	—		IOH \ge -12 mA, VDD = 3.3V
			2.4	—	_		ІОН ≥ -10 mA, VDD = 3.3V
			3.0 (1)		_		$IOH \ge -7 \text{ mA}, \text{ VDD} = 3.3 \text{ V}$

Note 1: Parameters are characterized, but not tested.

TABLE 4-7: ELECTRICAL CHARACTERISTICS: BROWN-OUT RESET (BOR)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$					
Param. No.	Symbol	Characteristics	Min. ⁽¹⁾ Typical Max. Units Conditions					
BO10	Vbor	BOR Event on VDD transition high-to-low ⁽²⁾	2.0	—	2.3	V	_	

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized.

TABLE 4-8: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS			Standa (unles Operat	ard Operat s otherwis	ting Cor se stated ature	nditions d) -40°C ≤	: 2.3V to 3.6V Ta ≤ +85°C
Param. No.	Symbol	Characteristics	Min. Typical Max. Units Comments				
D321	Cefc	External Filter Capacitor Value	8	10	_	μF	Capacitor must be low series resistance (1 ohm). Typical voltage on the VCAP pin is 1.8V.

4.2 AC Characteristics and Timing Parameters

The information contained in this section defines SSC7150 AC characteristics and timing parameters.





TABLE 4-9: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$				
Param. No.	Symbol	Characteristics	Min. Typical ⁽¹⁾ Max. Units				Conditions	
DO56	Сю	All I/O pins	—	_	50	pF		
DO58	Св	I2C_DAx, I2C_CLx	— — 400 pF In I ² C™ mode				In I ² C™ mode	

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 4-2: POWER-ON RESET TIMING CHARACTERISTICS



- **Note 1:** The power-up period will be extended if the power-up sequence completes before the device exits from BOR (VDD < VDDMIN).
 - 2: Includes interval voltage regulator stabilization delay.

FIGURE 4-3: EXTERNAL RESET TIMING CHARACTERISTICS



TABLE 4-10: RESET TIMING

AC CHA	RACTERI	STICS	Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Conditions				
SY00	Τρυ	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μs	_	
SY02	Tsysdly	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK ⁽³⁾ Delay before First instruction is Fetched.	_	1 μs + 8 SYSCLK cycles	_	_	_	
SY20	Tmclr	MCLR# Pulse Width (low)	2	_	_	μs	—	
SY30	TBOR	BOR Pulse Width (low)		1		μs	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

3: SYSCLK is 48MHz







TABLE 4-11: I²C BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHA	RACTER	ISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$				
Param. No.	Symbol	Charact	eristics	Min. ⁽¹⁾	Max.	Units	Conditions	
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Трв * (BRG + 2)		μs	—	
			400 kHz mode	Трв * (BRG + 2)	_	μs		
IM11	THI:SCL	Clock High Time	100 kHz mode	Трв * (BRG + 2)	—	μs	—	
			400 kHz mode	Трв * (BRG + 2)	—	μs		
IM20	TF:SCL	I2C_DAx and	100 kHz mode	—	300	ns	CB is specified to be	
		I2C_CLx Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF	
IM21	TR:SCL	I2C_DAx and	100 kHz mode	_	1000	ns	CB is specified to be	
		I2C_CLx Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF	
IM25	TSU:DAT	Data Input	100 kHz mode	250		ns		
		Setup Time	400 kHz mode	100		ns		
IM26	THD:DAT	Data Input	100 kHz mode	0	—	μs		
		Hold Time	400 kHz mode	0	0.9	μs		
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	Трв * (BRG + 2)	—	μs	Only relevant for	
			400 kHz mode	Трв * (BRG + 2)	—	μs	Repeated Start condition	
IM31	THD:STA	Start Condition	100 kHz mode	Трв * (BRG + 2)	—	μs	After this period, the	
		Hold Time	400 kHz mode	Трв * (BRG + 2)	—	μs	first clock pulse is generated	
IM33	Tsu:sto	Stop Condition	100 kHz mode	Трв * (BRG + 2)		μs	—	
		Setup Time	400 kHz mode	Трв * (BRG + 2)	—	μs		
IM34	THD:STO	Stop Condition	100 kHz mode	Трв * (BRG + 2)	—	ns		
		Hold Time	400 kHz mode	Трв * (BRG + 2)	—	ns		
IM40	TAA:SCL	Output Valid	100 kHz mode	—	3500	ns		
		from Clock	400 kHz mode	—	1000	ns		
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time	
			400 kHz mode	1.3	—	μs	the bus must be free before a new transmission can start	
1M50	CB	Bus Capacitivo I	l oading		400	nE		
IM51		Pulse Gobbler D	olauniy olav	52	312	ns	See Note 2	
	IFOD		July	52	512	113		

Note 1: BRG is the value of the I^2C^{TM} Baud Rate Generator.

2: The typical value for this parameter is 104 ns.







	AC	S	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$					
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions	
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	_	μs	—	
			400 kHz mode	1.3	_	μs	—	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	—	
			400 kHz mode	0.6	—	μs	—	
IS20	TF:SCL	I2C_DAx and I2C_CLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF	
			400 kHz mode	20 + 0.1 Св	300	ns		
IS21	TR:SCL	I2C_DAx and I2C_CLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from	
			400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	_	ns	. —	
			400 kHz mode	100	—	ns		
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	_	
			400 kHz mode	0	0.9	μs		
IS30	Tsu:sta	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition	
			400 kHz mode	600	—	ns		
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated	
			400 kHz mode	600	—	ns		
IS33	Tsu:sto	Stop Condition Setup Time	100 kHz mode	4000	—	ns	_	
			400 kHz mode	600	—	ns		
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	_	
			400 kHz mode	600		ns		
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—	
			400 kHz mode	0	1000	ns		
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	4.7 — μs The amou		The amount of time the bus	
			400 kHz mode	1.3		μs	must be free before a new transmission can start	
IS50	Св	Bus Capacitive Lo		400	pF	—		

TABLE 4-12: I²Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

APPENDIX A: REVISION HISTORY

Revision	Section/Figure/Entry	Correction		
DS00001885A (01-30-15)	Document Release			

TABLE A-1: REVISION HISTORY

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PART NO. ⁽¹⁾	- <u>xxx</u> ⁽²⁾	- <u>xxx</u>	- <u>[X]</u> ⁽³⁾	Examp	le:
Device Series	Package	Sensor Fusion Firmware	Tape and Reel Option	SSC715 sensor f	50-ML-AB0 = 28-QFN, Bosch 9-axis fusion.
Device:	SSC7150 ⁽¹⁾				
Package:	ML = 28 pir	n QFN ⁽²⁾			
Sensor Fusion Firmware:	AB0 = Bosch	n 9-axis Senso	r Fusion	Note 1:	These products meet the halogen maximum concentration values per IEC61249-2-21.
Tape and Reel Option:	Blank = Tray pa TR = Tape a	ickaging nd Reel ⁽³⁾		Note 2:	All package options are RoHS compliant. For RoHS compliance and environmental information, please visit <u>http://www.micro- chip.com/pagehandler/en-us/aboutus/</u> ehs.html.
				Note 3:	Tape and Reel identifier only appears in the catalog part number description. This identi- fier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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