

# **MICREL**

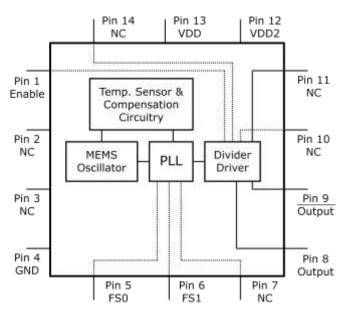
# Low-Jitter Configurable LVDS Oscillator

#### **General Description**

The DSC2030 series of high performance LVDS oscillators utilize a proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device functionality. The DSC2030 allows the user to easily modify the frequency of the oscillator using pins. The DSC2030 has provision for up to four user-defined pre-programmed, pin-selectable output frequencies.

DSC2030 is packaged in a 14-pin 3.2x2.5 mm QFN package and available in temperature grades from Ext. Commercial to Automotive.

# **Block Diagram**



#### **Features**

- Low RMS Phase Jitter: <1 ps (typ)
- High Stability: ±10, ±25, ±50 ppm
- Wide Temperature Range

   Industrial: -40° to 85° C
   Ext. commercial: -20° to 70° C
- High Supply Noise Rejection: -50 dBc
- 4 Pin-Selectable Output Frequencies
- Short Lead Times: 2 Weeks
- Wide Freq. Range: • LVDS Output: 2.3 to 460 MHz
- Miniature Footprint of 3.2x2.5mm
- Excellent Shock & Vibration Immunity • Qualified to MIL-STD-883
- High Reliability o 20x better MTF than quartz oscillators
- Supply Range of 2.25 to 3.6 V
- Lead Free & RoHS Compliant

### **Applications**

- Consumer Electronics
- Storage Area Networks
   SATA, SAS, Fibre Channel
- Passive Optical Networks • EPON, 10G-EPON, GPON, 10G-PON
- Ethernet o 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video & Surveillance
- PCI Express



#### **Pin Description**

Pin No.	Pin Name	Pin Type	Description
1	Enable	Ι	Enables outputs when high and disables when low
2	NC	NA	Leave unconnected or grounded
3	NC	NA	Leave unconnected or grounded
4	GND	Power	Ground
5	FS0	I	Least significant bit for frequency selection
6	FS1	I	Most significant bit for frequency selection
7	NC	NA	Leave unconnected or grounded
8	Output+	0	Positive LVDS Output
9	Output-	0	Negative LVDS Output
10	NC	NA	Leave unconnected or grounded
11	NC	NA	Leave unconnected or grounded
12	VDD2	Power	Power Supply
13	VDD	Power	Power Supply
14	NC	NA	Leave unconnected or grounded

#### **Operational Description**

The DSC2030 is a LVDS oscillator consisting of a MEMS resonator and a support PLL IC. The LVDS output is generated through independent 8-bit programmable dividers from the output of the internal PLL.

The actual frequency output by the DSC2030 is controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for up to four

#### **Output Clock Frequencies**

different frequencies. Two control pins (FS0 – FS1) select the output frequency. Discera supports customer defined versions of the DSC2030. Standard frequency options are described in the following sections.

When Enable (pin 1) is floated or connected to VDD, the DSC2030 is in operational mode. Driving Enable to ground will tri-state output driver (hi-impedance mode).

Table 1 lists the standard frequency configurations and the associated ordering information to be used in conjunction with the ordering code. Customer defined combinations are available.

Ordering	Freq	Freq Select Bits [FS1, FS0] – <b>Default is [11]</b>				
Info	(MHz)	00	01	10	11	
C0001	f <sub>out</sub>	148.35165	74.17582	148.5	74.25	
C0002	f <sub>out</sub>	100	0*	0*	100	
C0003	f <sub>оит</sub>	100	150	156.25	312.5	
C0004	f <sub>оит</sub>	148.5	148.35	0*	0*	
C0005	f <sub>оит</sub>	315	0*	0*	315	
C000X	f <sub>оит</sub>	Contact factory for additional configurations.				

 Table 1. Pre-programmed pin-selectable output frequency combinations

Frequency select bit are weakly tied high so if left unconnected the default setting will be [11] and the device will output the associated frequency highlighted in **Bold**.  $0^*$  – denotes invalid selection, output frequency is not specified.

DSC2030

**Ordering Code** 

F I 2

Package F: 3.2x2.5mm

Temp Range

E: -20 to 70

I: -40 to 85

-

XXXXX

Stability

1: ±50ppm

2: ±25ppm 5: ±10ppm



<u>Packing</u>

T: Tape & Reel

Т

Freq (MHz)

See Freq. table

: Tube

#### **Absolute Maximum Ratings**

Item	Min	Мах	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V <sub>DD</sub> +0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
HBM		4000		
MM		400		
CDM		1500		

Note: 1000+ years of data retention on internal memory

#### **Specifications** (Unless specified otherwise: T=25° C)

#### Condition **Parameter** Min. Max. Unit Typ. Supply Voltage<sup>1</sup> $V_{\text{DD}}$ 2.25 3.6 V Supply Current EN pin low - output is disabled 23 $\mathbf{I}_{\mathsf{D}\mathsf{D}}$ 21 mΑ EN pin high - outputs are enabled Supply Current<sup>2</sup> $I_{DD}$ 29 32 mΑ $R_L = 100\Omega$ , $F_O = 156.25$ MHz Includes frequency variations due $\pm 10$ Frequency Stability to initial tolerance, temp. and ±25 Δf ppm power supply voltage ±50 1 year @25°C ±5 Aging Δf ppm Startup Time<sup>3</sup> T=25°C 5 t<sub>su</sub> ms Input Logic Levels $0.75 \text{xV}_{\text{DD}}$ Input logic high VTH V $V_{\rm IL}$ Input logic low $0.25 \text{xV}_{DD}$ Output Disable Time<sup>4</sup> $t_{\text{DA}}$ 5 ns **Output Enable Time** 20 t<sub>EN</sub> ns Pull-Up Resistor<sup>2</sup> Pull-up exists on all digital IO 40 kΩ **LVDS Output** Output Offset Voltage R=100Ω Differential 1.125 V 1.4 Delta Offset Voltage 50 mV Pk to Pk Output Swing Single-Ended 350 mV Output Transition time<sup>4</sup> 20% to 80% Rise Time 200 350 t<sub>R</sub> ps $R_L = 100\Omega, C_L = 2pF$ Fall Time t<sub>F</sub> 2.3 460 Frequency $f_0$ Single Frequency MHz SYM **Output Duty Cycle** 48 52 % Differential Period Jitter<sup>5</sup> 2.5 $J_{PER}$ Fo=156.25 MHz **ps**<sub>RMS</sub> 0.28 200kHz to 20MHz @156.25MHz ps<sub>RMS</sub> Integrated Phase Noise 100kHz to 20MHz @156.25MHz 0.4 J<sub>CC</sub> 12kHz to 20MHz @156.25MHz 1.7 2

Notes:

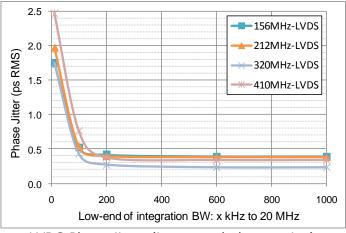
1. Pin 4  $V_{DD}$  should be filtered with 0.01uf capacitor.

Output is enabled if Enable pad is floated or not connected.
 t<sub>sv</sub> is time to 100PPM stable output frequency after V<sub>DD</sub> is applied and outputs are enabled.

Period Jitter includes crosstalk from adjacent output.

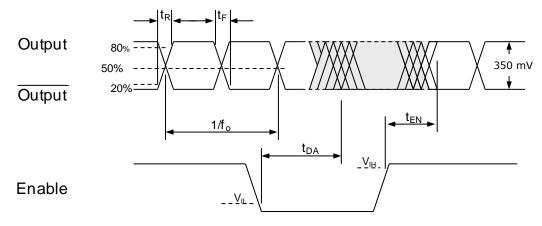


## **Nominal Performance Parameters** (Unless specified otherwise: T=25° C, V<sub>DD</sub>=3.3 V)



LVDS Phase jitter (integrated phase noise)

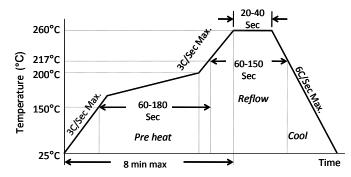
# **Output Waveform: LVDS**



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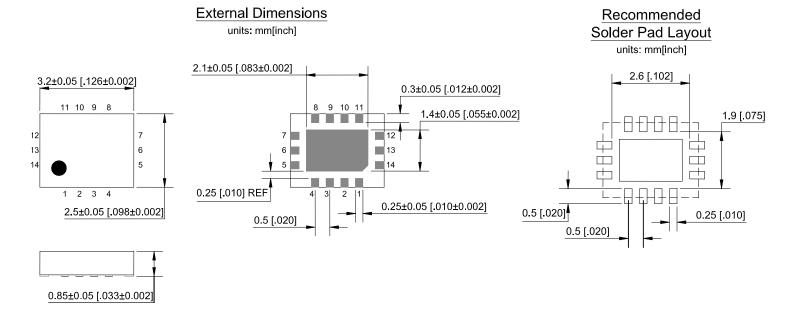
#### **Solder Reflow Profile**



MSL 1 @ 260°C refer to JSTD-020C				
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.			
Preheat Time 150°C to 200°C	60-180 Sec			
Time maintained above 217°C	60-150 Sec			
Peak Temperature	255-260°C			
Time within 5°C of actual Peak	20-40 Sec			
Ramp-Down Rate	6°C/Sec Max.			
Time 25°C to Peak Temperature	8 min Max.			

#### **Package Dimensions**





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