PL60203X

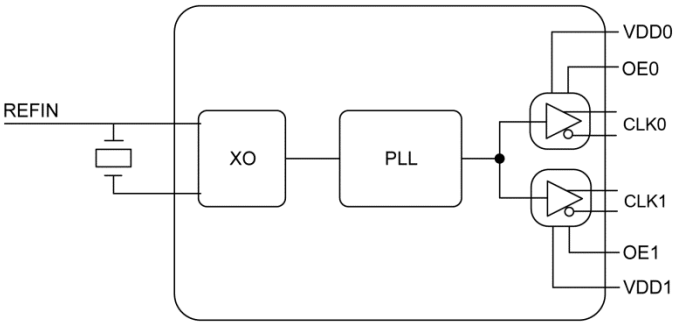
HCSL-Compatible Clock Generator for PCI Express

General Description

The PL60203X is the smallest, high performance, lowest power, 2 differential output clock IC available for HCSL timing applications. PL60203X offers -130dBc at 10kHz offset at 100MHz, with a very low jitter (2ps TIE RMS), making it ideal for HCSL applications requiring small size and low power.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Block Diagram



Features

- Input frequency:
  - Fundamental crystal or reference input: 25MHz.
- Output frequency:
  - PL602031: 2 x 25MHz differential outputs.
  - PL602032: 2 x 100MHz differential outputs.
  - PL602033: 2 x 125MHz differential outputs.
  - PL602034: 2 x 200MHz differential outputs.
- Very low jitter: 28ps peak-to-peak typical.
- Very low phase noise:
  - -130dBc at 10kHz offset at 100MHz.
- Compliant with PCI-Express Gen1, Gen2, and Gen3.
- Power supply range: 2.25V to 3.63V.
- Operating temperature range: -40°C to +85°C.
- Available in 16-pin QFN, RoHS and PFOS compliant package.

Applications

- Servers
- Storage systems
- Switches and routers
- Gigabit Ethernet
- Set-top boxes/DVRs

Ordering Information

Part Number[1]	Marking	Shipping	Junction Temperature Range	Package
PL602031UMG	602031	Tube	–40° to +85°C	16-Pin 3mm x 3mm QFN
PL602031UMG TR	602031	Tape and Reel	–40° to +85°C	16-Pin 3mm x 3mm QFN
PL602032UMG	602032	Tube	–40° to +85°C	16-Pin 3mm x 3mm QFN
PL602032UMG TR	602032	Tape and Reel	–40° to +85°C	16-Pin 3mm x 3mm QFN
PL602033UMG	602033	Tube	–40° to +85°C	16-Pin 3mm x 3mm QFN
PL602033UMG TR	602033	Tape and Reel	–40° to +85°C	16-Pin 3mm x 3mm QFN
PL602034UMG	602034	Tube	–40° to +85°C	16-Pin 3mm x 3mm QFN
PL602034UMG TR	602034	Tape and Reel	–40° to +85°C	16-Pin 3mm x 3mm QFN

Note:

1. The devices are RoHS and PFOS compliant.

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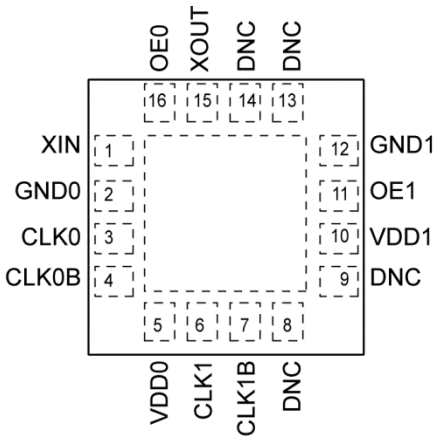
Pin Configuration



16-Pin QFN (Top View)

Pin Description

Pin Number	Pin Name	Pin Type	Pin Function
1	XIN, FIN	I	Crystal input pin or reference clock input.
2	GND0	I	GND connection for CLK0.
3, 4	CLK0[0:1]	O	Differential clock output pair
5	VDD0	P	VDD connection for CLK0
6, 7	CLK1[0:1]	O	Differential clock output pair
10	VDD1	P	VDD connection for CLK1
11	OE1	I	Output enable pin for CLK1. High=Enabled, Low=Disabled. OE1 has a 60KΩ pull-up resistor.
12	GND1	P	GND connection for CLK1
15	XOUT	O	Crystal output pin
16	OE0	I	Output enable pin for CLK0. High=Enabled, Low=Disabled. OE0 has a 60KΩ pull-up resistor.
8, 9 13, 14	DNC		Do not connect.
	ePad		Center pad for thermal relief. Connect to GND.

Absolute Maximum Ratings[2]

Supply Voltage (V_{IN}) ..... +4.6V
Lead Temperature (soldering, 10s) ..... 260°C
Storage Temperature (T_S) ..... 150°C
ESD Rating[3] 2.0kV

Operating Ratings[4]

Supply Voltage (V_{IN}) ..... –0.5V to +4.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[5]
QFN Still-air (θ_{JA}) ..... 60°C/W
QFN Junction-to-board (ψ_{JB}) ..... 33°C/W

AC Electrical Characteristics[6]

V_{DD} = 3.3V ±10% or 2.5V ±10%, T_A = -40°C to +85°C, HCSL termination applied.

Parameter	Condition	Min.	Typ.	Max.	Units
Crystal input frequency	Fundamental crystal		25		MHz
Input (F_{IN}) frequency			25		MHz
Input (F_{IN}) signal amplitude	Internally AC coupled	0.9		V_{DD}	Vpp
Output frequency	PL602031		25		MHz
	PL602032		100		MHz
	PL602033		125		MHz
	PL602034		200		MHz
Output enable time	OE function, T_A=25°C, add one clock period to this measurement for a useable clock output.			10	ns
Output disable time	OE function, T_A=25°C			10	ns
Setting time	At power up (V_{DD} ≥ 2.25V)			10	ms
VDD sensitivity	Frequency vs. V_{DD} ±10%, crystal input only.	-2		2	ppm
Output rise time	20/80%		0.3	0.5	ns
Output fall time	20/80%		0.3	0.5	ns
Duty cycle	At V_{DD}/2	45	50	55	%
Period jitter, peak-to-peak	With capacitive decoupling between V_{DD} and GND at 100MHz; 10,000 samples measured		28		ps
Phase jitter, RMS	For 10kHz to 10MHz integration range		2.1		ps

DC Electrical Characteristics[6]

V_{DD} = 3.3V ±10% or 2.5V ±10%, T_A = -40°C to +85°C, HCSL termination applied.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DD}	Supply current, dynamic	At 100MHz, no load		50	70	mA
V_{DD}	Operating voltage		2.25		3.63	V
V_{OL}	Output low voltage	HCSL termination, (RS = 150Ω, RT = 49.9Ω) 3.3V (RS = 100Ω, RT = 49.9Ω) 2.5V			0.05	V
V_{OH}	Output high voltage		0.65	0.75	0.85	V

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Crystal Characteristics[6]

V_{DD} = 3.3V ±10% or 2.5V ±10%, T_A = -40°C to +85°C.

Symbol	Parameter	Min.	Typ.	Max.	Units
F_{XIN}	Fundamental crystal resonator		25		MHz
$C_{L\ (XTAL)}$	Crystal load rating		18		pF
	Maximum sustainable drive level			500	µW
	Operating drive level		100		µW
C0	Crystal shunt capacitance			6	pF
ESR	Effective series resistance, fundamental			45	Ω

Notes:

2. Exceeding the absolute maximum ratings may damage the device.
3. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5k in series with 100pF.
4. The device is not guaranteed to function outside its operating ratings.
5. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. θ_{JA} and ψ_{JB} values are determined for a 4-layer board in still-air number, unless otherwise stated.
6. Specification for packaged product only

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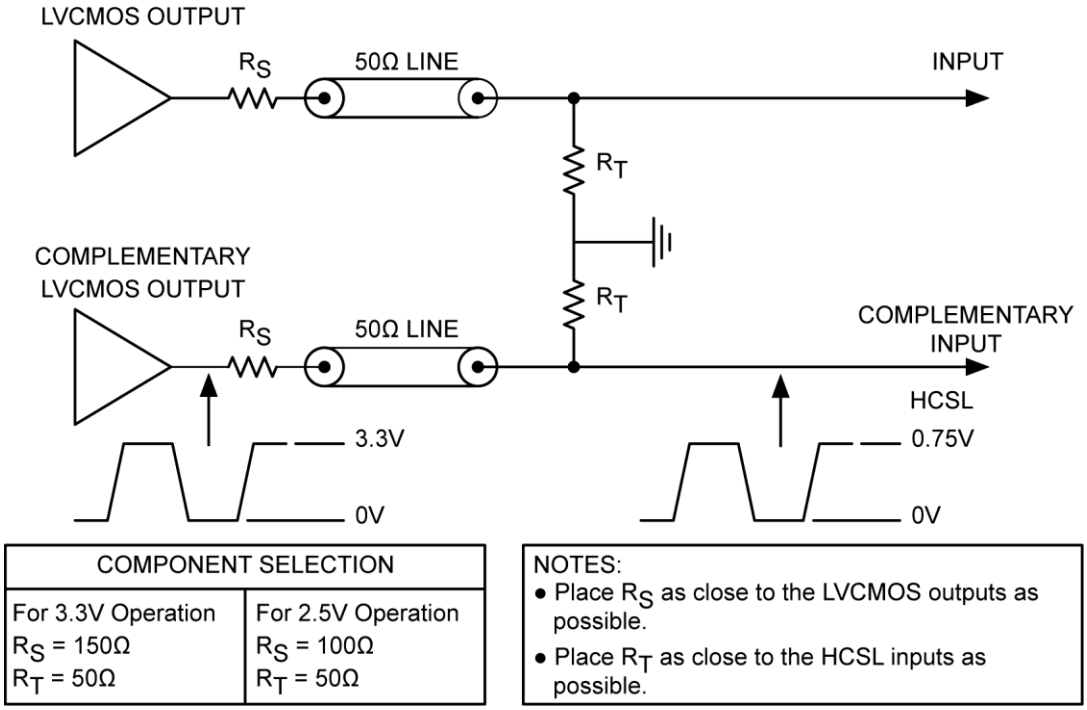
PCI Express/HCSL Compatible Layout Guidelines

Figure 1 below demonstrates how to terminate the complementary LVCMOS outputs of PL60203X for use with HCSL inputs.



COMPONENT SELECTION	
For 3.3V Operation R_S = 150Ω R_T = 50Ω	For 2.5V Operation R_S = 100Ω R_T = 50Ω

NOTES:
- Place R_S as close to the LVCMOS outputs as possible.
- Place R_T as close to the HCSL inputs as possible.

Figure 1. Terminating the complementary LVCMOS outputs for use with HCSL inputs.

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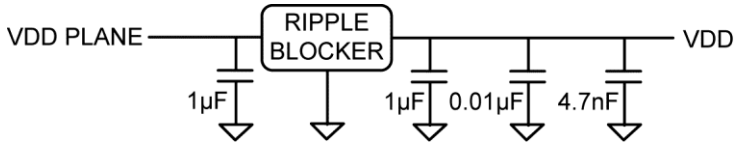
PCB Layout Considerations for Performance Optimization

The following guidelines are designed to assist you with a performance-optimized PCB design:

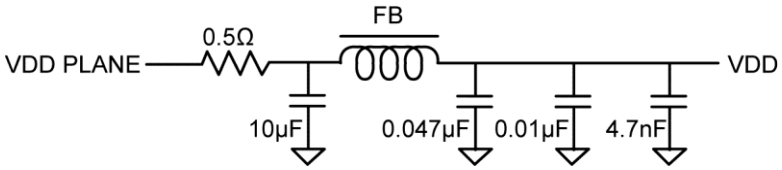
- Keep all the PCB traces to PL60203X as short as possible. Also keep all other traces as far away from PL60203X as possible.
- Place the crystal as close as possible to both crystal pins of the device. This will reduce the cross-talk between the crystal and the other signals.
- Separate crystal pin traces from the other signals on the PCB, but allow ample distance between the two crystal pin traces.
- Place a 0.01µF decoupling capacitor between VDD and GND on the component side of the PCB, close to the VDD pin. It is not recommended to place this component on the backside of the PCB.
- It is highly recommended to keep the VDD and GND traces as short as possible.
- When connecting long traces (>1 inch) to a CMOS output, it is important to design the traces as a transmission line, or “stripline”, to avoid reflections or ringing. In this case, the CMOS output needs to be matched to the trace impedance. Usually, “striplines” are designed for 50Ω impedance and CMOS outputs usually have an impedance of less than 50Ω, so matching can be achieved by adding a resistor in series with the CMOS output pin to the “stripline” trace.

Power Supply Filtering Recommendations

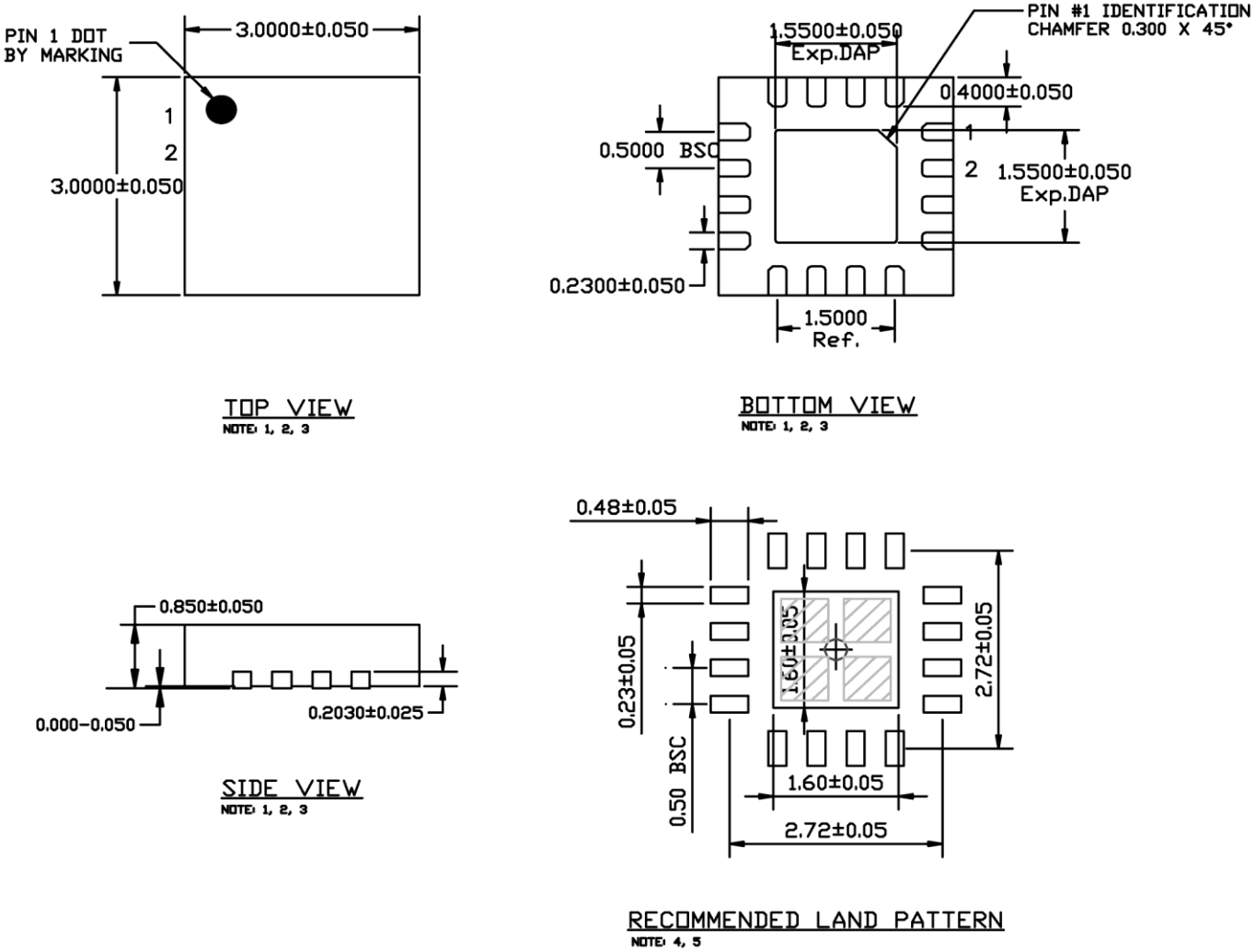
Preferred filter, using Micrel MIC94300 or MIC94310 Ripple Blocker™:



Alternative, traditional filter, using a ferrite bead:



Package Information[7]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

16-Pin QFN

Note:

7. Package information is correct as of the publication date. For updates and most current information, go to: www.micrel.com.

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