



# SY56017R

Low Voltage 1.2V/1.8V/2.5V CML 2:1 MUX  
6.4Gbps with Equalization

Preliminary

## General Description

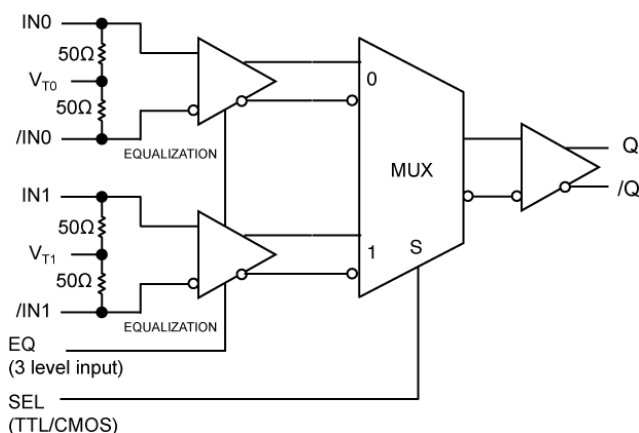
The SY56017R is a fully differential, low voltage 1.2V/1.8V/2.5V CML 2:1 MUX with input equalization. The SY56017R can process clock signals as fast as 4.5 GHz or data patterns up to 6.4Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to CML differential signals, without any level-shifting or termination resistor networks in the signal path. The differential input can also accept AC-coupled LVPECL and LVDS signals. Input voltages as small as 200mV (400mV<sub>pp</sub>) are applied before the 9", 18" or 27" FR4 transmission line. For AC-coupled input interface applications, an internal voltage reference is provided to bias the V<sub>T</sub> pin. The outputs are CML, with extremely fast rise/fall times guaranteed to be less than 80ps.

The SY56017R operates from a 2.5V ±5% core supply and a 1.2V, 1.8V or 2.5V ±5% output supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). The SY56017R is part of Micrel's high-speed, Precision Edge<sup>®</sup> product line.

Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

## Functional Block Diagram



Precision Edge<sup>®</sup>

## Features

- 1.2V/1.8V/2.5V CML 2:1 MUX
- Equalizes 9, 18, 27 inches of FR4
- Guaranteed AC performance over temperature and voltage:
  - DC-to > 6.4Gbps Data throughput
  - DC-to > 4.5GHz Clock throughput
  - <280 ps propagation delay (IN-to-Q)
  - <20ps input skew
  - <80ps rise/fall times
- Ultra-low jitter design
  - <1ps<sub>RMS</sub> cycle-to-cycle jitter
- High-speed CML outputs
- 2.5V ±5% V<sub>CC</sub>, 1.2/1.8V/2.5V ±5% V<sub>CCO</sub> power supply operation
- Industrial temperature range: -40°C to +85°C
- Available in 16-pin (3mm x 3mm) QFN package

## Applications

- Data Distribution:
- SONET clock and data distribution
- Fiber Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

## Markets

- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Metro area network equipment

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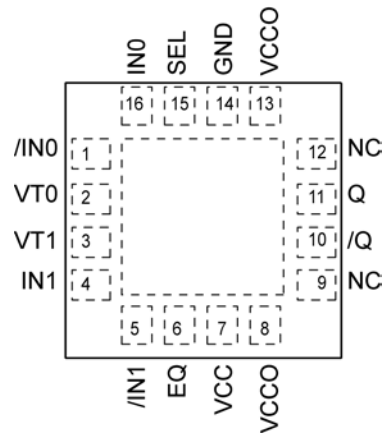
### Ordering Information<sup>(1)</sup>

| Part Number                 | Package Type | Operating Range | Package Marking                      | Lead Finish       |
|-----------------------------|--------------|-----------------|--------------------------------------|-------------------|
| SY56017RMG                  | QFN-16       | Industrial      | R017 with Pb-Free bar-line indicator | NiPdAu<br>Pb-Free |
| SY56017RMGTR <sup>(2)</sup> | QFN-16       | Industrial      | R017 with Pb-Free bar-line indicator | NiPdAu<br>Pb-Free |

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.

### Pin Configuration



16-Pin QFN

### Truth Table

| SEL | OUTPUT             |
|-----|--------------------|
| 0   | IN0 Input Selected |
| 1   | IN1 Input Selected |

| EQ    | EQUALIZATION |
|-------|--------------|
| LOW   | 27"          |
| FLOAT | 18"          |
| HIGH  | 9"           |

## Pin Description

| Pin Number  | Pin Name               | Pin Function   |
|-------------|------------------------|--|
| 16,1<br>4,5 | IN0, /IN0<br>IN1, /IN1 | Differential Inputs: Signals as small as 200mV $V_{PK}$ (400mV $_{PP}$ ) applied to the input of 9, 18 or 27 inches 6 mil FR4 stripline transmission line are then terminated with the differential input. Each input pin internally terminates with 50 $\Omega$ to the VT pin.  |
| 2<br>3      | VT0<br>VT1             | Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. An internal high impedance resistor divider biases VT to allow input AC-coupling. For AC-coupling, bypass VT with 0.1 $\mu$ F low ESR capacitor to VCC. See "Interface Applications" subsection and Figure 2a. |
| 6           | EQ                     | Three level input for equalization control. High, float, low. EQ pin applies the same EQ setting to both inputs.   |
| 15          | SEL                    | This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25k $\Omega$ pull-up resistor and will default to a logic HIGH state if left open.  |
| 7           | VCC                    | Positive Power Supply: Bypass with 0.1 $\mu$ F//0.01 $\mu$ F low ESR capacitors as close to the VCC pins as possible. Supplies input and core circuitry.   |
| 8,13        | VCCO                   | Output Supply: Bypass with 0.1 $\mu$ F//0.01 $\mu$ F low ESR capacitors as close to the VCCO pins as possible. Supplies the output buffers.  |
| 14          | GND,<br>Exposed pad    | Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pins.   |
| 11,10       | Q, /Q                  | CML Differential Output Pair: Differential buffered copy of the input signal. The output swing is typically 390mV. See "Interface Applications" subsection for termination information.  |

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +3.0V  
 Supply Voltage ( $V_{CCO}$ ) ..... -0.5V to +3.0V  
 $V_{CC} - V_{CCO}$  ..... <1.8V  
 $V_{CCO} - V_{CC}$  ..... <0.5V  
 Input Voltage ( $V_{IN}$ ) ..... -0.5V to  $V_{CC}$   
 CML Output Voltage ( $V_{OUT}$ ) ..... 0.6V to 3.0V  
 Current ( $V_T$ )  
     Source or sink on VT pin .....  $\pm 100$ mA  
 Input Current  
     Source or sink Current on (IN, /IN) .....  $\pm 50$ mA  
 Maximum operating Junction Temperature ..... 125°C  
 Lead Temperature (soldering, 20sec.) ..... 260°C  
 Storage Temperature ( $T_s$ ) ..... -65°C to +150°C

### Operating Ratings<sup>(2)</sup>

Supply Voltage ( $V_{CC}$ ) ..... 2.375V to 2.625V  
 ( $V_{CCO}$ ) ..... 1.14V to 2.625V  
 Ambient Temperature ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance<sup>(3)</sup>  
 QFN  
     Still-air ( $\theta_{JA}$ ) ..... 75°C/W  
     Junction-to-board ( $\psi_{JB}$ ) ..... 33°C/W

### DC Electrical Characteristics<sup>(4)</sup>

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

| Symbol         | Parameter   | Condition   | Min   | Typ | Max          | Units    |
|----------------|---|---|-------|-----|--------------|----------|
| $V_{CC}$       | Power Supply Voltage Range                          | $V_{CC}$  | 2.375 | 2.5 | 2.625        | V        |
|                |   | $V_{CCO}$   | 1.14  | 1.2 | 1.26         | V        |
|                |   | $V_{CCO}$   | 1.7   | 1.8 | 1.9          | V        |
|                |   | $V_{CCO}$   | 2.375 | 2.5 | 2.625        | V        |
| $I_{CC}$       | Power Supply Current                                | Max. $V_{CC}$   |       | 55  | 80           | mA       |
| $I_{CCO}$      | Power Supply Current                                | No Load. $V_{CCO}$  |       | 16  | 21           | mA       |
| $R_{IN}$       | Input Resistance<br>(IN-to- $V_T$ , /IN-to- $V_T$ ) |   | 45    | 50  | 55           | $\Omega$ |
| $R_{DIFF\_IN}$ | Differential Input Resistance<br>(IN-to-/IN)        |   | 90    | 100 | 110          | $\Omega$ |
| $V_{IH}$       | Input HIGH Voltage<br>(IN, /IN)                     | IN, /IN   | 1.42  |     | $V_{CC}$     | V        |
| $V_{IL}$       | Input LOW Voltage<br>(IN, /IN)                      | IN, /IN<br>1.22V = 1.7-0.475                                  | 1.22  |     | $V_{IH}-0.2$ | V        |
| $V_{IN}$       | Input Voltage Swing<br>(IN, /IN)                    | see Figure 3a, Note 5, applied to input of transmission line. | 0.2   |     | 1.0          | V        |
| $V_{DIFF\_IN}$ | Differential Input Voltage Swing<br>( IN - /IN )    | see Figure 3b, Note 5, applied to input of transmission line. | 0.4   |     | 2.0          | V        |
| $V_{T\_IN}$    | Voltage from Input to $V_T$                         |   |       |     | 1.28         | V        |

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.  $\psi_{JB}$  and  $\theta_{JA}$  values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5.  $V_{IN(max)}$  is specified when  $V_T$  is floating.

### CML Outputs DC Electrical Characteristics<sup>(6)</sup>

$V_{CCO} = 1.14V$  to  $1.26V$   $R_L = 50\Omega$  to  $V_{CCO}$ ,

$V_{CCO} = 1.7V$  to  $1.9V$ ,  $2.375V$  to  $2.625V$ ,  $R_L = 50\Omega$  to  $V_{CCO}$  or  $100\Omega$  across the outputs,

$V_{CC} = 2.375V$  to  $2.625V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

| Symbol          | Parameter                         | Condition                     | Min            | Typ            | Max      | Units    |
|-----------------|-----------------------------------|-------------------------------|----------------|----------------|----------|----------|
| $V_{OH}$        | Output HIGH Voltage               | $R_L = 50\Omega$ to $V_{CCO}$ | $V_{CC}-0.020$ | $V_{CC}-0.010$ | $V_{CC}$ | V        |
| $V_{OUT}$       | Output Voltage Swing              | See Figure 3a                 | 300            | 390            | 475      | mV       |
| $V_{DIFF\_OUT}$ | Differential Output Voltage Swing | See Figure 3b                 | 600            | 780            | 950      | mV       |
| $R_{OUT}$       | Output Source Impedance           |                               | 45             | 50             | 55       | $\Omega$ |

### LVTTL/CMOS DC Electrical Characteristics<sup>(6)</sup>

$V_{CC} = 2.375V$  to  $2.625V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

| Symbol   | Parameter          | Condition | Min  | Typ | Max      | Units   |
|----------|--------------------|-----------|------|-----|----------|---------|
| $V_{IH}$ | Input HIGH Voltage |           | 2.0  |     | $V_{CC}$ | V       |
| $V_{IL}$ | Input LOW Voltage  |           |      |     | 0.8      | V       |
| $I_{IH}$ | Input HIGH Current |           | -125 |     | 30       | $\mu A$ |
| $I_{IL}$ | Input LOW Current  |           | -300 |     |          | $\mu A$ |

### Three Level EQ Input DC Electrical Characteristics<sup>(6)</sup>

$V_{CC} = 2.375V$  to  $2.625V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

| Symbol   | Parameter          | Condition         | Min          | Typ | Max          | Units   |
|----------|--------------------|-------------------|--------------|-----|--------------|---------|
| $V_{IH}$ | Input HIGH Voltage |                   | $V_{CC}-0.3$ |     | $V_{CC}$     | V       |
| $V_{IL}$ | Input LOW Voltage  |                   | 0            |     | $V_{EE}+0.3$ | V       |
| $I_{IH}$ | Input HIGH Current | $V_{IH} = V_{CC}$ |              |     | 400          | $\mu A$ |
| $I_{IL}$ | Input LOW Current  | $V_{IL} = GND$    | -480         |     |              | $\mu A$ |

**Note:**

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC Electrical Characteristics

$V_{CC0} = 1.14V$  to  $1.26V$   $R_L = 50\Omega$  to  $V_{CC0}$ ,

$V_{CC0} = 1.7V$  to  $1.9V$ ,  $2.375V$  to  $2.625V$ ,  $R_L = 50\Omega$  to  $V_{CC0}$  or  $100\Omega$  across the outputs,

$V_{CC} = 2.375V$  to  $2.625V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

| Symbol       | Parameter                                      | Condition               | Min | Typ | Max | Units             |
|--------------|--|-------------------------|-----|-----|-----|-------------------|
| $f_{MAX}$    | Maximum Frequency                              | NRZ Data                | 6.4 |     |     | Gbps              |
|              |  | $V_{OUT} > 200mV$ Clock | 4.5 |     |     | GHz               |
| $t_{PD}$     | Propagation Delay<br>IN-to-Q<br>SEL-to-Q       | Note 7, Figure 1        | 100 | 180 | 280 | ps                |
|              |  | Figure 1                | 90  | 210 | 350 | ps                |
| $t_{Skew}$   | Input-to-Input Skew                            | Note 8                  |     |     | 20  | ps                |
|              | Part-to-Part Skew                              | Note 9                  |     |     | 100 | ps                |
| $t_{Jitter}$ | Random Jitter                                  | Note 10                 |     |     | 1   | ps <sub>RMS</sub> |
|              | Crosstalk Induced Jitter<br>(Adjacent Channel) | Note 11                 |     |     | 0.7 | ps <sub>PP</sub>  |
| $t_R$ $t_F$  | Output Rise/Fall Time<br>(20% to 80%)          | At full output swing.   | 20  | 50  | 80  | ps                |

### Notes:

7. Propagation delay is measured with no attenuating transmission line connected to the input.
8. Input-to-Input skew is the difference in time between both inputs and the output for the same temperature, voltage and transition.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
10. Random jitter is measured with a K28.7 pattern, measured at  $\leq f_{MAX}$ .
11. Crosstalk induced jitter is defined as the added jitter that results from signals applied to the adjacent channel. It is measured at the output while applying a similar, differential clock frequencies that are asynchronous with respect to each other at the adjacent input.

## Interface Applications

For Input Interface Applications see Figures 4a-e and for CML Output Termination see Figures 5a-d.

### CML Output Termination with VCCO 1.2V

For VCCO of 1.2V, Figure 5a, terminate the output with 50 Ohms to 1.2V, not 100 ohms differentially across the outputs. If AC-coupling is used, Figure 5d, terminate into 50 ohms to 1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage. Any unused output pair needs to be terminated, do not leave floating.

### CML Output Termination with VCCO 1.8V

For VCCO of 1.8V, Figure 5a and Figure 5b, terminate with either 50 ohms to 1.8V or 100 ohms differentially across the outputs. AC- or DC-coupling is fine.

### Input Termination

1.8V CML driver: Terminate input with VT tied to 1.8V. Don't terminate 100 ohms differentially.

2.5V CML driver: Terminate input with either VT tied to 2.5V or 100 ohms differentially.

The input cannot be DC coupled from a 1.2V CML driver.

## Timing Diagrams

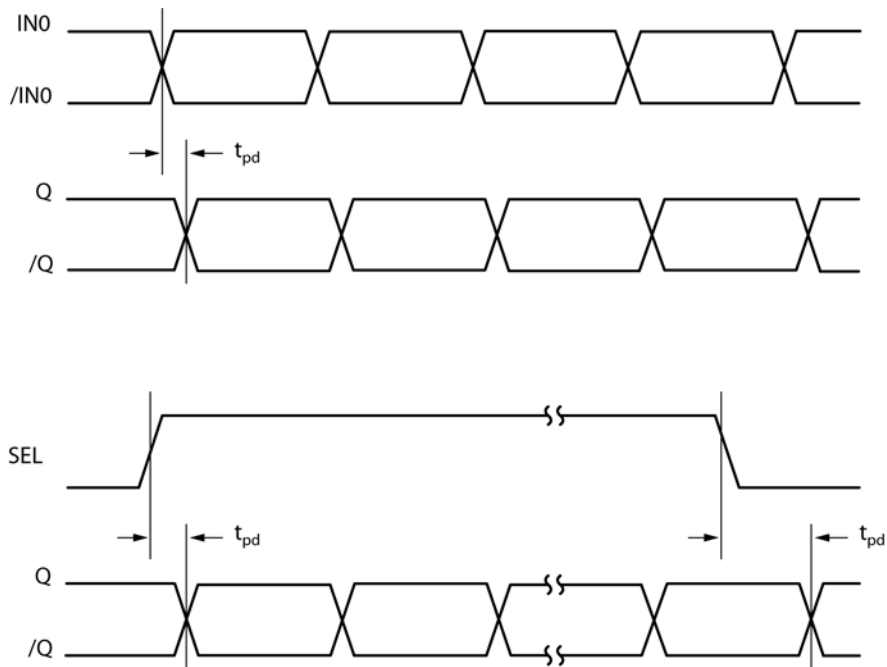
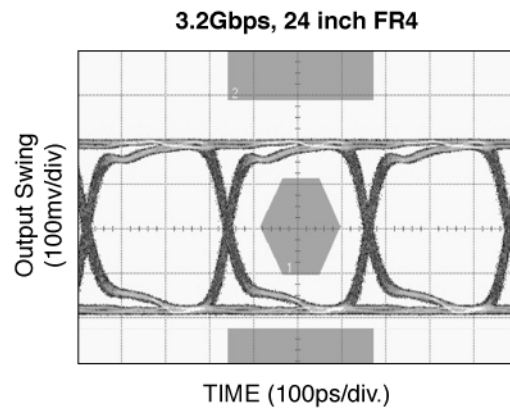
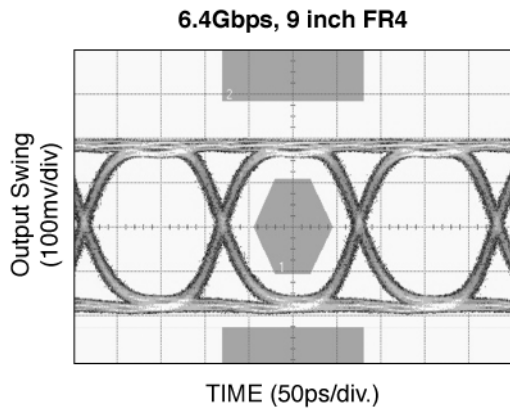
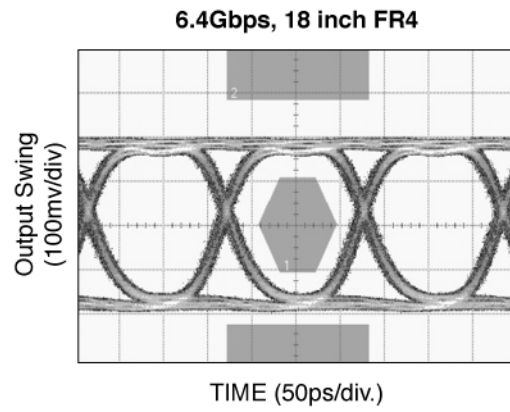
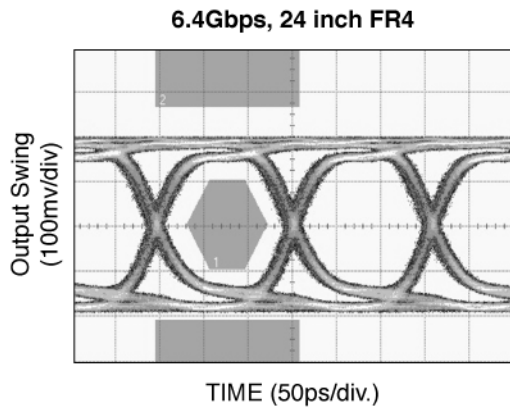


Figure 1. Propagation Delay

### Typical Characteristics

$V_{CC} = 2.5$ ,  $V_{CCO} = 1.2V$ ,  $GND = 0V$ ,  $V_{IN} = 400mV$ ,  $R_L = 50\Omega$  to  $1.2V$ , Data Pattern:  $2^{23}-1$ ,  $T_A = 25^\circ C$ , unless otherwise stated.





## Input and Output Stage

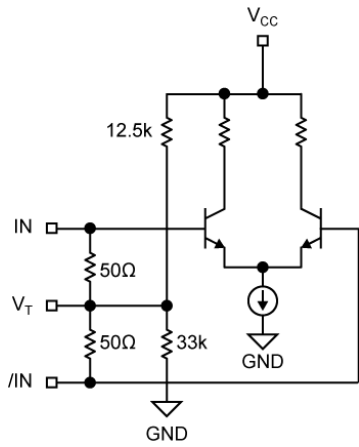


Figure 2a. Simplified Differential Input Buffer

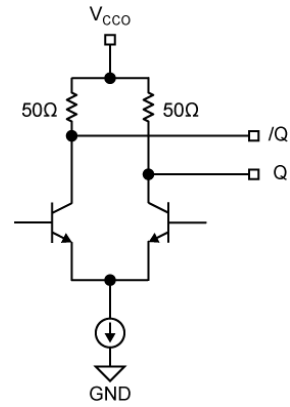


Figure 2b. Simplified CML Output Buffer

## Single-Ended and Differential Swings

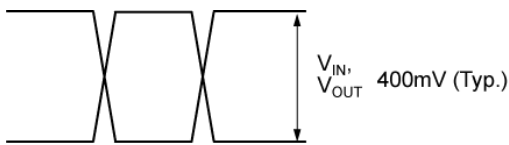


Figure 3a. Single-Ended Swing

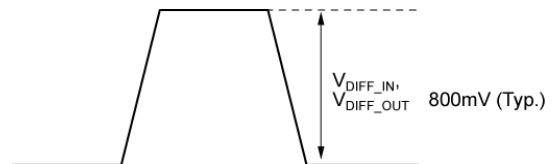
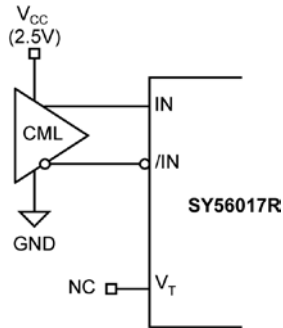
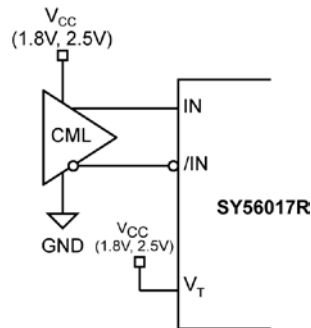


Figure 3b. Differential Swing

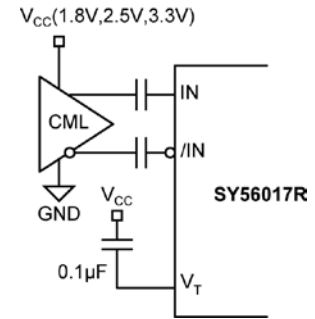
## Input Interface Applications



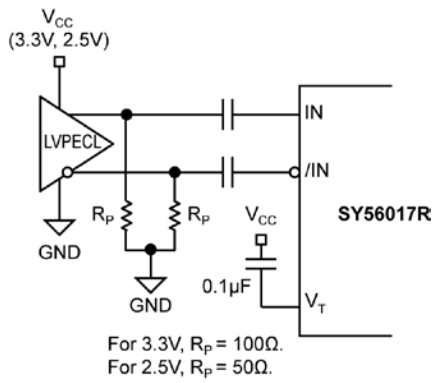
**Figure 4a. CML Interface**  
**100Ω Differential**  
**(DC-Coupled, 2.5V)**



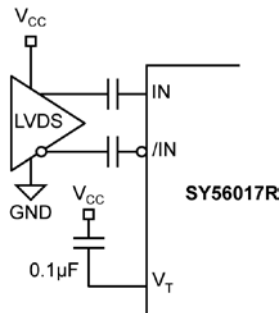
**Figure 4b. CML Interface**  
**50Ω to V<sub>CC</sub>**  
**(DC-Coupled, 1.8V, 2.5V)**



**Figure 4c. CML Interface**  
**(AC-Coupled)**



**Figure 4d. LVPECL Interface**  
**(AC-Coupled)**



**Figure 4e. LVDS Interface**  
**(AC-Coupled)**

### CML Output Termination

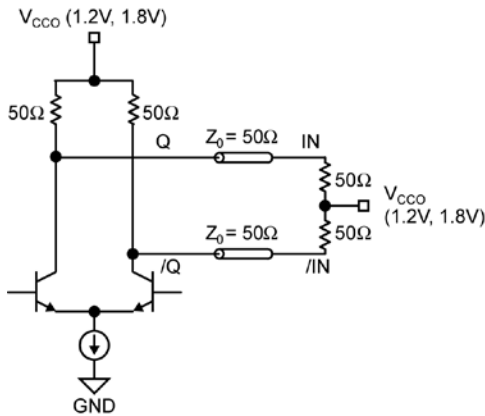


Figure 5a. 1.2V or 1.8V CML DC-Coupled Termination

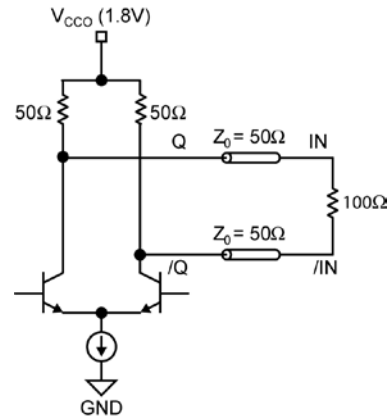


Figure 5b. 1.8V CML DC-Coupled Termination

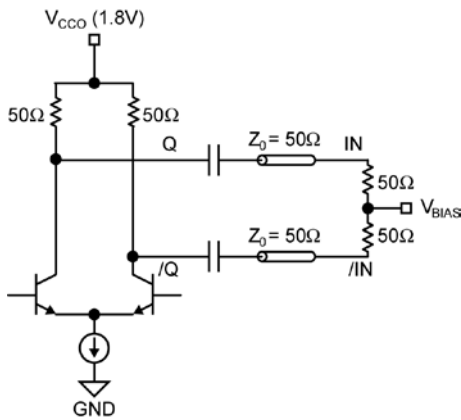


Figure 5c. CML AC-Coupled Termination  
V<sub>CCO</sub> 1.8V Only

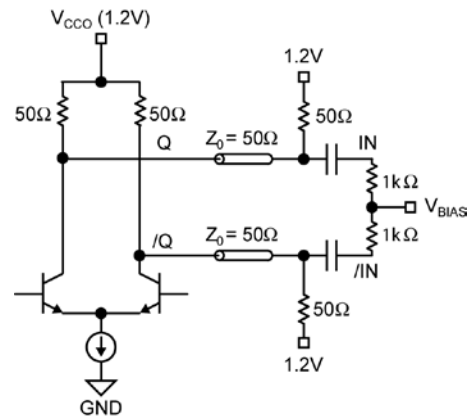
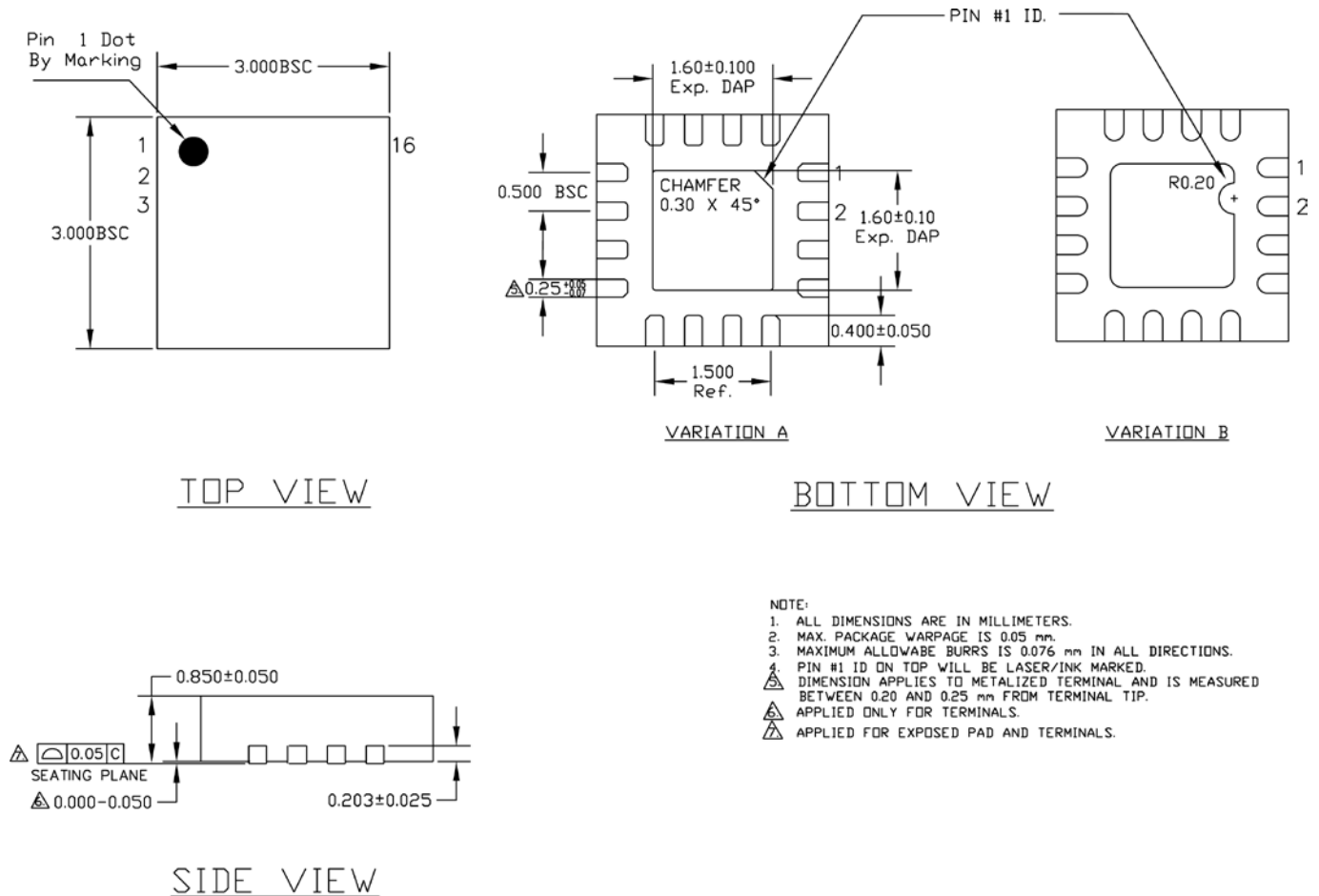


Figure 5d. CML AC-Coupled Termination  
V<sub>CCO</sub> 1.2V Only

### Related Product and Support Documents

| Part Number   | Function                                       | Datasheet Link  |
|---------------|--|---|
| HBW Solutions | New Products and Termination Application Notes | <a href="http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml">http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml</a> |

**Package Information**



**16-Pin QFN**

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