SCH3221

LPC I/O with Quad UARTs, GPIO and Wake

Product Features

- General Features
  - 3.3 Volt Operation (5 Volt Tolerant)
  - PC99, PC2001 Compliant
  - ACPI Compliant
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - Two Address Options for Power On Configuration Port
  - System Management Interrupt (SMI)
- Low Pin Count Bus (LPC) Interface
- 33 General Purpose I/O pins
- Programmable Wake-up Event (PME) Interface
  - Serial Modem RI Inputs
  - GPIOs
  - Watchdog
- 4 Full Function Serial Ports
  - High Speed NS16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
- Infrared Communications Controller
  - IrDA v1.2 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - 2 IR Ports
  - 96 Base I/O Address, 15 IRQ, and 4 DMA Options
- Two LED Drivers with Blinking Options
- Watchdog Timer
- Temperature Ranges Available
  - Industrial (+85°C to -40°C)
  - Commercial (+70°C to 0°C)
- 64-Ball WFBGA RoHS Compliant Package

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Table of Contents

1.0 INTRODUCTION

1.1 Description

The SCH3221 is a 3.3V (5V tolerant) PC99/PC2001 compliant I/O controller with an LPC interface. The SCH3221 includes 4 Full-Function Serial Ports, IrDA and Consumer IR capability, GPIOs, and extensive PME Wake support from these features.

The SCH3221 is ACPI compatible and supports multiple low power-down modes.

I/O functionality includes four serial ports. The serial ports are fully functional NS16550 compatible UARTs that support data rates up to 460 Kbps. They all have the full 8 pin interface.

The PME Wake logic includes the ability to wake from a watchdog timer, any of the UART Ring Indicator (RI) Inputs, or GPIOs.

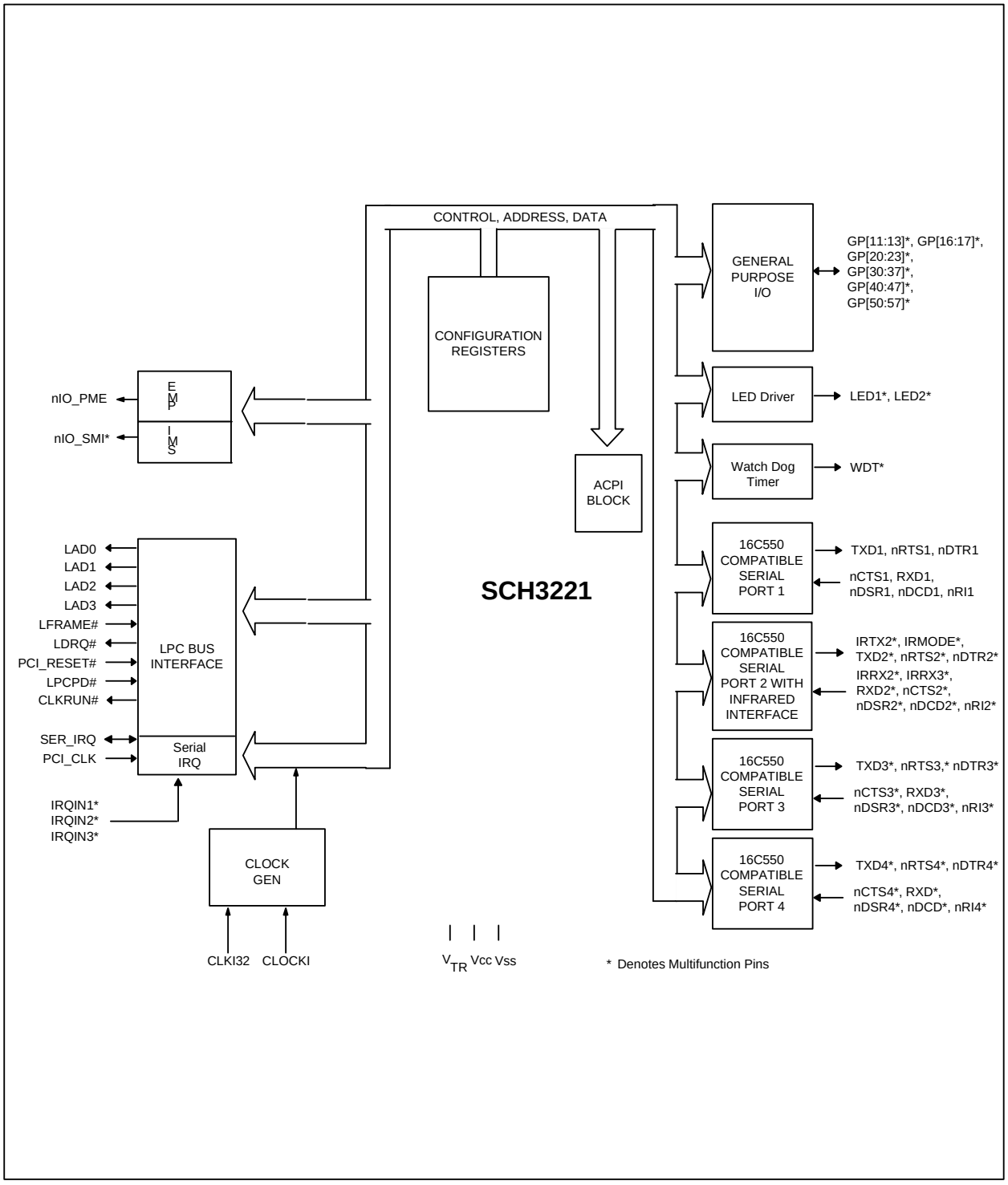
SMI Generation is also supported.

System related functionality, which offers flexibility to the system designer, includes General Purpose I/O control functions, a Watchdog Timer, and control of two LED's.

CAUTION: This device contains circuits which must not be used because their pins are not brought out of the package, and are pulled to known states internally. Any features, and especially SIO blocks that are not listed in this document, must not be activated or accessed. Doing so may cause unpredictable behavior and/or excessive currents, and therefore may damage the device and/or the system.
As part of this, it is also necessary to pull the GP57/nDTR2 pin low, as a strap, to disable LPC Memory cycle handling. See Note 3-12 on page 13.

1.2 Block Diagram

FIGURE 1-1: SCH3221 BLOCK DIAGRAM



1.3 References

1. SMSC Infrared Communications Controller (IrCC) Specification, dated 5/10/96
2. PCI Bus Power Management Interface Specification, Revision 1.0, Draft, March 18, 1997
3. Low Pin Count (LPC) Interface Specification, Revision 1.0, September 29, 1997, Intel Document
4. Advanced Configuration and Power interface Specification, Revision 1.0

2.0 PIN LAYOUT

Figure 2-1 shows the ball footprint for the SCH3221. See Table 2-1 below it for the pin function assignments.

FIGURE 2-1: SCH3221 FOOTPRINT DIAGRAM, TOP VIEW

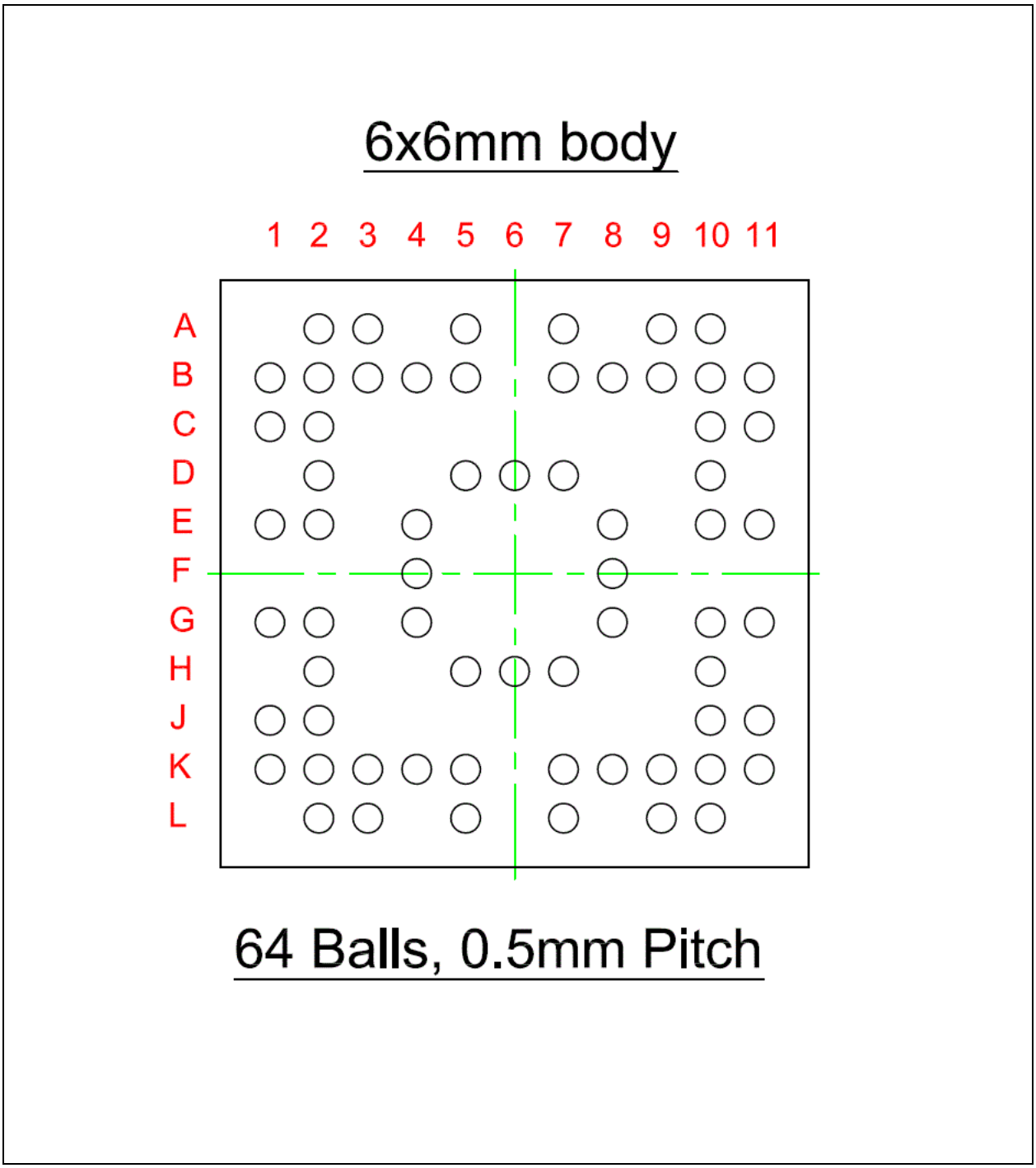


TABLE 2-1: SCH3221 SUMMARY

BALL#	FUNCTION
B3	GP11
A3	TEST=VSS
B5	CLOCKI
D6	VSS
B2	CLKI32
B1	IO_PME#
F4	VTR
C1	GP23 / nLED2 / IRQIN2
E2	LAD0
D2	LAD1
E1	LAD2
G1	LAD3
E4	VCC
G2	LFRAME#
H5	VSS
B4	LDRQ#
A2	PCI_RESET#
J1	LPCPD#
J2	CLKRUN#
K1	PCI_CLK
K2	SER_IRQ
K3	GP30 / nRI3
L2	GP31 / nDCD3
L3	GP32 / RXD3
K4	GP33 / TXD3
H2	GP34 / nDSR3
L5	GP35 / nRTS3
K5	GP36 / nCTS3
L7	GP37 / nDTR3
G4	GP40 / nRI4
A5	GP41 / nDCD4
C2	GP42 / RXD4
L9	GP43 / TXD4
F8	GP44 / nDSR4
H6	GP45 / nRTS4
G8	GP46 / nCTS4
E8	VCC
K7	GP47 / nDTR4
J11	GP12 / IO_SMI#
H7	VSS
L10	GP13 / IRQIN1 / nLED1
K11	GP16
K8	GP17
K9	GP20 / IRRX2 / IRQIN3

TABLE 2-1: SCH3221 SUMMARY (CONTINUED)

BALL#	FUNCTION
J10	GP21 / IRTX2 / WDT
K10	GP22 / IRMODE / IRRX3
G11	RXD1
G10	TXD1
H10	nDSR1
A7	nRTS1 / SYSOPT
B7	nCTS1
E10	nDTR1
B8	nRI1
E11	nDCD1
C11	GP50 / nRI2
D10	GP51 / nDCD2
B9	GP52 / RXD2 / IRRX
C10	GP53 / TXD2 / IRTX
B10	GP54 / nDSR2
B11	GP55 / nRTS2
A10	GP56 / nCTS2
A9	GP57 / nDTR2
D5	VCC
D7	VSS

3.0 DESCRIPTION OF PIN FUNCTIONS

The following section describes the functionality of the pins for the SCH3221.

TABLE 3-1: PIN FUNCTIONS

Name	Function	Buffer Type (Note 3-1)	Power Well
POWER PINS			
VCC	+3.3 Volt Supply Voltage (Note 3-8)		
VTR	+3.3 Volt Standby Supply Voltage (Note 3-8)		
VSS	Ground		
CLOCK PINS			
CLKI32	32.768kHz Standby Clock Input (Note 3-3)	IS	VTR
CLOCKI	14.318MHz Clock Input	IS	VCC
SERIAL PORT 1 INTERFACE			
RXD1	Receive Data 1	IS	VCC
TXD1	Transmit Data 1	O12	VCC
nDSR1	Data Set Ready 1	I	VCC
nRTS1 /SYSOPT	Request to Send 1 /(System Option) (Note 3-4)	OP14	VCC
nCTS1	Clear to Send 1	I	VCC
nDTR1	Data Terminal Ready 1	OP14	VCC
nRI1	Ring Indicator 1	I	VCC (Note 3-13)
nDCD1	Data Carrier Detect 1	I	VCC
SERIAL PORT 2 INTERFACE			
GP50 /nRI2	General Purpose I/O /Ring Indicator 2	IO8	VCC (Note 3-13)
GP51 /nDCD2	General Purpose I/O /Data Carrier Detect 2	IO8	VCC
GP52 /RXD2 /IRRX	General Purpose I/O /Receive Data 2 /IRRX	IS/O8	VCC
GP53 /TXD2 /IRTX	General Purpose I/O /Transmit Data 2 /IRTX (Note 3-6, Note 3-7)	IO12	VCC
GP54 /nDSR2	General Purpose I/O /Data Set Ready 2	IO8	VCC
GP55 /nRTS2	General Purpose I/O /Request to Send 2	IO8	VCC
GP56 /nCTS2	General Purpose I/O /Clear to Send 2	IO8	VCC
GP57 /nDTR2	General Purpose I/O /Data Terminal Ready 2 **CAUTION:** External pull-down is required on this pin (Note 3-12).	IOP14	VCC
SERIAL PORT 3 INTERFACE			
GP30 /nRI3	General Purpose I/O (Note 3-11) /Ring Indicator 3	IO8	VCC (Note 3-13)
GP31 /nDCD3	General Purpose I/O (Note 3-11) /Data Carrier Detect 3	IO8	VCC (Note 3-13)
GP32 /RXD3	General Purpose I/O (Note 3-11) /Receive Data 3	IS/O8	VCC (Note 3-13)

TABLE 3-1: PIN FUNCTIONS (CONTINUED)

Name	Function	Buffer Type (Note 3-1)	Power Well
GP33 /TXD3	General Purpose I/O (Note 3-11) /Transmit Data 3	IO12	VCC (Note 3-13)
GP34 /nDSR3	General Purpose I/O (Note 3-11) /Data Set Ready 3	IO8	VCC (Note 3-13)
GP35 /nRTS3	General Purpose I/O (Note 3-11) /Request to Send 3	IO8	VCC (Note 3-13)
GP36 /nCTS3	General Purpose I/O (Note 3-11) /Clear to Send 3	IO8	VCC (Note 3-13)
GP37 /nDTR3	General Purpose I/O (Note 3-11) /Data Terminal Ready 3	IO8	VCC (Note 3-13)
SERIAL PORT 4 INTERFACE			
GP40 /nRI4	General Purpose I/O (Note 3-11) /Ring Indicator 4	IO8	VCC (Note 3-13)
GP41 /nDCD4	General Purpose I/O (Note 3-11) /Data Carrier Detect 4	IO8	VCC
GP42 /RXD4	General Purpose I/O (Note 3-11) /Receive Data 4	IS/O8	VCC
GP43 /TXD4	General Purpose I/O (Note 3-11) /Transmit Data 4	IO12	VCC
GP44 /nDSR4	General Purpose I/O (Note 3-11) /Data Set Ready 4	IO8	VCC
GP45 /nRTS4	General Purpose I/O (Note 3-11) /Request to Send 4	IO8	VCC
GP46 /nCTS4	General Purpose I/O (Note 3-11) /Clear to Send 4	IO8	VCC
GP47 /nDTR4	General Purpose I/O (Note 3-11) /Data Terminal Ready 4	IO8	VCC
IR INTERFACE			
GP20 /IRRX2 /IRQIN3	General Purpose I/O /IR Receive /IRQ Input 3	IS/O8	VCC (Note 3-13)
GP21 /IRTX2 /WDT	General Purpose I/O (Note 3-11) /IR Transmit (Note 3-5, Note 3-7) /Watch Dog Timer	IO12	VCC (Note 3-13)
MISCELLANEOUS AND GPIO PINS			
GP11	General Purpose I/O	IO12	VCC (Note 3-13)
GP12 /IO_SMI#	General Purpose I/O /System Mgt. Interrupt	IO12	VCC (Note 3-13)
GP13 /IRQIN1 /nLED1	General Purpose I/O / IRQ Input 1 /nLED1 (Note 3-9)	IO12	VCC (Note 3-13)
GP16	General Purpose I/O	IO8	VTR (Note 3-13)
GP17	General Purpose I/O	IO8	VCC
GP22 /IRMODE /IRRX3	General Purpose I/O (Note 3-11) /IR Mode /IR Receive 3	IS/O8	VCC (Note 3-13)

TABLE 3-1: PIN FUNCTIONS (CONTINUED)

Name	Function	Buffer Type (Note 3-1)	Power Well
GP23 /nLED2 /IRQIN2	General Purpose I/O /nLED2 (Note 3-10) /IRQ Input 2	IO12	VTR (Note 3-13)
TEST	Test Input **Tie to VSS except in Test modes.**	IS	VCC
LPC AND ASSOCIATED INTERFACE PINS			
IO_PME#	Power Management Event Output	OD12	VTR
PCI_CLK	PCI Clock	PCI_ICLK	VCC
SER_IRQ	Serial IRQ	PCI_IO	VCC
LAD0	Multiplexed Command Address and Data 0	PCI_IO	VCC
LAD1	Multiplexed Command Address and Data 1	PCI_IO	VCC
LAD2	Multiplexed Command Address and Data 2	PCI_IO	VCC
LAD3	Multiplexed Command Address and Data 3	PCI_IO	VCC
LFRAME#	Frame	PCI_I	VCC
LDRQ#	Encoded DMA Request	PCI_O	VCC
PCI_RESET#	PCI Reset	PCI_I	VCC
LPCPD#	Power Down (Note 3-1)	PCI_I	VCC
CLKRUN#	PCI Clock Controller	PCI_OD	VCC

Note: The "n" as the first letter of a signal name or the “#” as the suffix of a signal name indicates an "Active Low" signal.

Note 3-1 Pins that have input buffers must always be held to either a logical low or a logical high state when powered. Bi-directional buses that may be tristated should have either weak external pull-ups or pull-downs to prevent the pins from floating.

Note 3-2 The LPCPD# pin may be tied high. The LPC interface will function properly if the PCI_RESET# signal follows the protocol defined for the LRESET# signal in the “Low Pin Count Interface Specification”.

Note 3-3 If the 32kHz input clock is not used the CLKI32 pin must be grounded. There is a bit in the configuration register at CR1E that determines whether the 32KHz clock input is used as the clock source for the WDT and the LED’s. Set this bit to ‘1’ if the clock is not connected.

Note 3-4 The nRTS1/SYSOPT pin requires an external pulldown resistor to put the base I/O address for configuration at 0x02E. An external pullup resistor is required to move the base I/O address for configuration to 0x04E.

Note 3-5 The GP21/IRTX2/WDT pin is tristate when VCC=0. The pin comes up as an output and low following a VCC POR and Hard Reset if configured for IRTX2 function. The GP21/IRTX2/WDT pin will remain low following a power-up (VCC POR) if configured for IRTX2 until serial port 2 is enabled by setting the UART2 Power bit to ‘1’. Once the power has been applied the pin will reflect the state of the IR transmit output of the IRCC block. If this pin is configured for GPIO function, the pin will reflect the state of the GPIO on a VCC POR.

Note 3-6 The GP53/TXD2/IRTX pin defaults to tristate when the part is under VTR power (VCC=0). The pin comes up tristate following a VTR POR, VCC POR, and Hard Reset. If the pin is configured for alternate functions TXD2 or IRTX the GP53/TXD2/IRTX pin will remain tristate following a power-up (VCC POR) until the UART2 Power bit is set to ‘1’. Once the power has been applied to the UART, the pin will reflect the current state of the output transmit buffer. If this pin is configured for GPIO function, the pin will reflect the state of the GPIO on a VCC POR.

Note 3-7 VTR can be connected to VCC if no wakeup functionality is required.

Note 3-8 VCC must not be greater than 0.5V above VTR.

Note 3-9 The nLED1 pin is powered by VCC and can only be controlled when the part is under VCC power.

Note 3-10 The nLED2 pin is powered by VTR so that the LED can be controlled when the part is under VTR power.

Note 3-11 These GPIO pins only have push-pull buffers. They cannot be configured for open drain outputs.

Note 3-12 **CAUTION:** This pin floats during VCC POR and must be pulled low externally during this time for correct LPC bus operation. A weak external pull-down resistor may be used for this. Failure to provide this may cause this device to improperly react to LPC Memory traffic, and this in turn can cause excessive current, unpredictable system operation, and damage to the device.

Note 3-13 These pins have input buffers into the wakeup logic that are powered by VTR.

Note 3-14 This buffer type is different from the buffer types shown per function because it is a pin that supports alternate functions that require additional buffer types.

3.1 Buffer Type Description

I	Input TTL Compatible.
IS	Input with Schmitt Trigger.
IPD	Input with 30uA Integrated Pull-Down
O6	Output, 6mA sink, 3mA source.
O8	Output, 8mA sink, 4mA source.
OD8	Open Drain Output, 8mA sink.
IO8	Input/Output, 8mA sink, 4mA source.
O12	Output, 12mA sink, 6mA source.
OD12	Open Drain Output, 12mA sink.
IO12	Input/Output, 12mA sink, 6mA source.
OD14	Open Drain Output, 14mA sink.
OP14	Output, 14mA sink, 14mA source.
IOP14	Input/Output, 14mA sink, 14mA source. Backdrive protected.
PCI_I	Input. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 3-15)
PCI_O	Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 3-15)
PCI_OD	Open Drain Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 3-15)
PCI_IO	Input/Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 3-15)
PCI_ICLK	Clock Input. These pins meet the PCI 3.3V AC and DC Characteristics and timing. (Note 3-16)

Note 3-15 See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2.

Note 3-16 See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2. and 4.2.3.

3.2 Design Guidelines for Implemented Buffer Types

The characteristics of the I/O buffers implemented in this device are defined in Section 9.2, "DC Electrical Characteristics," on page 102. Care should be taken to ensure that external devices maintain acceptable voltage levels on all inputs and open drain outputs. It is not advisable to allow input buffers to float or remain in an indeterminate state.

Note:	It is important not to cross power domains when attaching pull-ups to pins. Pins that are located on the VCC power well must be pulled either to ground or to VCC. This includes GPIO pins with wakeup capability that are located on the VCC power well (see Table 3-1, “Pin Functions,” on page 10).

Pins that are located on the VTR power well must be pulled either to ground or to VTR.

The following is a list of design guidelines to help identify which pins require external pull-up/pull-down resistors:

1. Input buffers that are of type I or IS must be driven to a logic high or a logic low when power is applied to the buffer. If the external device controlling the input buffer tristates while power is applied to the buffer, an external pull-up/pull-down resistor should be added to prevent the pin from floating.
2. All output pins that are implemented as open drain outputs, must be pulled through an external resistor to the proper VCC or VTR power plane.
3. All GPIO registers default to a GPIO input on a VTR POR. On a cold boot, a VCC POR will implement these pins as GPIO inputs. It is suggested that these pins are pulled to their inactive state (either to the proper VCC or VTR power plane or ground) depending on the function being implemented on the pin.

4.0 3.3 VOLT OPERATION / 5 VOLT TOLERANCE

The SCH3221 is a 3.3 Volt part. It is intended solely for 3.3V applications. Non-LPC bus pins are 5V tolerant; that is, the input voltage is 5.5V max, and the I/O buffer output pads are backdrive protected.

The LPC interface pins are 3.3 V only. These signals meet PCI DC specifications for 3.3V signaling. These pins are:

- LAD[3:0]
- LFRAME#
- LDRQ#
- LPCPD#

The input voltage for all other pins is 5.5V max. These pins include all non-LPC Bus pins and the following pins:

- PCI_RESET#
- PCI_CLK
- SER_IRQ
- CLKRUN#
- IO_PME#

5.0 POWER FUNCTIONALITY

The SCH3221 has two power planes: VCC and VTR.

5.1 VCC Power

The SCH3221 is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). See the Operational Description Section and the Maximum Current Values subsection.

5.2 VTR Support

The SCH3221 requires a trickle supply (VTR) to provide sleep current for the programmable wake-up events in the PME interface when VCC is removed. The VTR supply is 3.3 Volts (nominal). See the Operational Description Section. The maximum VTR current that is required depends on the functions that are used in the part. See Trickle Power Functionality subsection and the Maximum Current Values subsection. If the SCH3221 is not intended to provide wake-up capabilities on standby current, VTR can be connected to VCC. The VTR pin generates a VTR Power-on-Reset signal to initialize these components.

Note:	If VTR is to be used for programmable wake-up events when VCC is removed, VTR must be at its full minimum potential at least 10 s before VCC begins a power-on cycle. When VTR and VCC are fully powered, the potential difference between the two supplies must not exceed 500mV.

5.3 32.768 kHz Trickle Clock Input

The SCH3221 utilizes a 32.768 kHz trickle input to supply a clock signal for the Watchdog Timer (WDT) and LED blink function.

Note:	LED1 has a VCC powered output pin and will only generate a signal when the device is powered by VCC. LED2 has a VTR powered output pin and may be used under VTR power.

The SCH3221 has two different methods of deriving a 32.768kHz signal:

- From an external single-input clock source driven on the CLKI32 pin
- From an internal PLL that divides down the14MHz clock input to make the 32kHz signal

If the 32kHz input clock is not used the CLKI32 pin must be grounded and the CLK32_PRSN bit should be set to '1'. This bit in the configuration register block at register index CR1E determines whether the internal 32KHz clock is derived from the CLKI32 pin or the 14MHz clock input. This clock input is used as the clock source for the WDT and the LEDs. This register is powered by VTR and reset on a VTR POR.

Bit[0] (CLK32_PRSN) is defined as follows:

0=32kHz clock is connected to the CLKI32 pin (default)

1=32kHz clock is not connected to the CLKI32 pin (pin is grounded).

Bit 0 controls the source of the 32kHz (nominal) clock for the LED blink logic and the WDT. When the external 32kHz clock is connected, bit[0] should be set to '0' so that the external clock will be the source for the LED blink logic and the WDT. When the external 32kHz clock is not connected, bit[0] should be set to '1' so that an internal 32kHz clock source will be derived from the 14MHz clock for the LED blink logic and the WDT.

The following functions will not work under VTR power (VCC removed) if the external 32kHz clock is not connected. These functions will work under VCC power even if the external 32kHz clock is not connected.

- LED blink
- WDT

5.4 Internal PWRGOOD

An internal PWRGOOD logical control is included to minimize the effects of pin-state uncertainty in the host interface as VCC cycles on and off. When the internal PWRGOOD signal is "1" (active), VCC > 2.3V (nominal), and the SCH3221 host interface is active. When the internal PWRGOOD signal is "0" (inactive), VCC 2.3V (nominal), and the SCH3221 host interface is inactive; that is, LPC bus reads and writes will not be decoded.

The SCH3221 device pins IO_PME#, nRI1, nRI2, nRI3, nRI4, and most GPIOs (as input) are part of the PME interface and remain active when the internal PWRGOOD signal has gone inactive, provided VTR is powered. See Trickle Power Functionality section.

5.5 Trickle Power Functionality

When the SCH3221 is running under VTR only, the PME wakeup events are active and (if enabled) able to assert the IO_PME# pin active low. The following lists the wakeup events:

- UART 1 Ring Indicator
- UART 2 Ring Indicator
- UART 3 Ring Indicator
- UART 4 Ring Indicator
- WDT
- GPIOs for wakeup. See below.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.
- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means they will, at a minimum, source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup inputs are GP11-GP13, GP16-GP17, GP20-GP23, GP30-GP37, GP40, and GP50. These GPIOs function as follows:

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are for PME wakeup as a GPIO function (or alternate function).

See the Table in the GPIO section for more information.

The following list summarizes the blocks, registers and pins that are powered by VTR.

- PME interface block
- CLKI32
- WDT block
- LED block
- LED2 pin
- Runtime register block (includes all PME, SMI, WDT, LED, and GP data registers)
- Pins for PME Wakeup:
  - GPIOs (GP11-GP13, GP16-GP17, GP20-GP23, GP30-GP37, GP40, and GP50)
  - IO_PME#
  - nRI1, nRI2, nRI3, nRI4

5.6 Maximum Current Values

See Section 9.0, "Operational Description" for the maximum current values.

The maximum VTR current, ITR, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V). The total maximum current for the part is the unloaded value PLUS the maximum current sourced by the pin that is driven by VTR. The pins that are powered by VTR (as output) are IO_PME#, LED2 and nPME. These pins, if configured as a push-pull output, will source a minimum of 6mA at 2.4V when driving.

The maximum VCC current, ICC, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V).

5.7 Power Management Events (PME/SCI)

The SCH3221 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME output signal. See the "PME Support" section.

6.0 FUNCTIONAL DESCRIPTION

6.1 Super I/O Registers

The address map, shown below in Table 6-1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the serial ports, runtime register block and configuration register block can be moved via the configuration registers. Some addresses are used to access more than one register.

6.2 Host Processor Interface

The host processor communicates with the SCH3221 through a series of read/write registers via the host processor interface. The port addresses for these registers are shown in Table 6-1. Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide.

TABLE 6-1: SUPER I/O BLOCK ADDRESSES

Address	Block Name
Base+(0-7)	Serial Port Com 1
Base1+(0-7) Base2+(0-7)	Serial Port Com 2 (IR Support)
Base+(0-7)	Serial Port Com 3
Base+(0-7)	Serial Port Com 4
Base + (0-F)	Runtime Registers
Base + (0-1)	Configuration

Note 6-1 Refer to the configuration register descriptions for setting the base address.

6.3 LPC Interface

The SCH3221 communicates with the host over a Low Pin Count (LPC) interface. For a complete description of the LPC interface, see the Intel Low Pin Count Specification, Rev 1.0. The following sections define the LPC signals implemented, the cycles supported, and protocols implemented that are specific to this device.

Note: The LPC interface uses 3.3V signaling. For electrical specifications see the Intel Low Pin Count Specification, Rev 1.0 and the PCI Local Bus Specification, Rev 2.2.

6.3.1 LPC INTERFACE SIGNAL DEFINITION

The signals required for the LPC bus interface are described in the table below. LPC bus signals use PCI 33MHz electrical signal characteristics.

TABLE 6-2: LPC BUS INTERFACE SIGNALS

Signal Name	Type	Description
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
LFRAME#	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
PCI_RESET#	Input	PCI Reset. Used as LPC Interface Reset.
LDRQ#	Output	Encoded DMA/Bus Master request for the LPC interface.
IO_PME#	OD	Power Mgt Event signal. Allows the SCH3221 to request wakeup.
LPCPD#	Input	Powerdown Signal. Indicates that the SCH3221 should prepare for power to be shut on the LPC interface.
PCI_CLK	Input	PCI Clock
CLKRUN#	I/OD	Clock Run. Allows the SCH3221 to request the stopped PCI_CLK be started.
IO_SMI#	OD	System Mgt Interrupt signal. Allows the SCH3221 to notify the host system that an event has occurred.

Note 6-2 The IO_PME#, IO_SMI#, and PCI_CLK signals are considered part of the host interface.

6.3.2 LPC CYCLES

The following cycle types are supported by the LPC protocol.

TABLE 6-3: LPC CYCLE TYPES

Cycle Type (Note 6-3)	Transfer Size
I/O Write	1 Byte
I/O Read	1 Byte
DMA Write	1 Byte
DMA Read	1 Byte

Note 6-3 The SCH3221 ignores cycles that it does not support.
CAUTION: A pull-down strap is necessary on the GP57/nDTR2 pin to ensure this, as well as to prevent chip damage. See Note 3-12 on page 13.

6.3.3 LFRAME# USAGE

LFRAME# is used by the host to indicate the start of cycles and the termination of cycles due to an abort or time-out condition. This signal is to be used by the SCH3221 to know when to monitor the bus for a cycle.

This signal is used as a general notification that the LAD[3:0] lines contain information relative to the start or stop of a cycle, and that the SCH3221 monitors the bus to determine whether the cycle is intended for it. The use of LFRAME# allows the SCH3221 to enter a lower power state internally. There is no need for the SCH3221 to monitor the bus when it is inactive, so it can decouple its state machines from the bus, and internally gate its clocks.

When the SCH3221 samples LFRAME# active, it immediately stops driving the LAD[3:0] signal lines on the next clock and monitor the bus for new cycle information.

The LFRAME# signal functions as described in the Low Pin Count (LPC) Interface Specification Revision 1.0.

6.3.4 FIELD DEFINITIONS

LPC transactions are defined as being comprised of multiple fields. These fields may be one or more nibbles in length (nibble=4 bits). All LPC transactions begin with a START field and a Cycle Type/Direction field. The START field is used to initiate/terminate LPC transactions. The Cycle Type/Direction field is used to define the cycle type (I/O, DMA) and direction (read/write) for LPC cycles. The remaining fields of data being transfered are based on specific fields that are used in various combinations, depending on the cycle type. These remaining fields are driven on to the LAD[3:0] signal lines to communicate address, control and data information over the LPC bus between the host and the SCH3221. See the *Low Pin Count (LPC) Interface Specification* Revision 1.0 from Intel, Section 4.2 for definition of these fields. The following sections describe the supported cycle types.

Note: I/O and DMA cycles use a START field of 0000.

6.3.4.1 I/O Read and Write Cycles

The SCH3221 is the target for I/O cycles. I/O cycles are initiated by the host for register or FIFO accesses, and will generally have minimal Sync times. The minimum number of wait-states between bytes is 1.

Data transfers are assumed to be exactly 1-byte. If the CPU requested a 16 or 32-bit transfer, the host will break it up into 8-bit transfers.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 5.2, for the sequence of cycles for the I/O Read and Write cycles.

6.3.4.2 DMA Read and Write Cycles

DMA read cycles involve the transfer of data from the host (main memory) to the SCH3221. DMA write cycles involve the transfer of data from the SCH3221 to the host (main memory). Data will be coming from or going to a FIFO and will have minimal Sync times. Data transfers to/from the SCH3221 are 1 byte.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 6.4, for the field definitions and the sequence of the DMA Read and Write cycles.

6.3.4.3 DMA Protocol

DMA on the LPC bus is handled through the use of the LDRQ# lines from the SCH3221 and special encodings on LAD[3:0] from the host.

The DMA mechanism for the LPC bus is described in the Low Pin Count (LPC) Specification Revision 1.0.

6.3.5 POWER MANAGEMENT

6.3.5.1 CLOCKRUN Protocol

See the Low Pin Count (LPC) Interface Specification Reference, Section 8.1.

6.3.5.2 LPCPD Protocol

The SCH3221 will function properly if the LPCPD# signal goes active and then inactive again without PCI_RESET# becoming active. This is a requirement for notebook power management functions.

Although the LPC Bus spec 1.0 section 8.2 states, "After LPCPD# goes back inactive, the LPC I/F will always be reset using LRST#", this statement does not apply for mobile systems. LRST# (PCI_RESET#) will not occur if the LPC Bus power was not removed. For example, when exiting a "light" sleep state (ACPI S1, APM POS), LRST# (PCI_RESET#) will not occur. When exiting a "deeper" sleep state (ACPI S3-S5, APM STR, STD, soft-off), LRST# (PCI_RESET#) will occur.

The LPCPD# pin is implemented as a “local” powergood for the LPC bus in the SCH3221. It is not used as a global powergood for the chip. It is used to reset the LPC block and hold it in reset.

An internal powergood is implemented in SCH3221 to minimize power dissipation in the entire chip.

Prior to going to a low-power state, the system will assert the LPCPD# signal. It will go active at least 30 microseconds prior to the LCLK# (PCI_CLK) signal stopping low and power being shut to the other LPC I/F signals.

Upon recognizing LPCPD# active, the SCH3221 will drive the LDRQ# signal low or tri-state, and do so until LPCPD# goes back active.

Upon recognizing LPCPD# inactive, the SCH3221 will drive its LDRQ# signal high.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 8.2.

6.3.5.3 SYNC Protocol

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 4.2.1.8 for a table of valid SYNC values.

The SYNC pattern is used to add wait states. For read cycles, the SCH3221 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the SCH3221 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The SCH3221 will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value.

The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks. The SCH3221 uses a SYNC of 0101 for all wait states in a DMA transfer.

The SYNC value of 0110 is intended to be used where the number of wait states is large. The SCH3221 uses a SYNC of 0110 for all wait states in an I/O transfer. The SYNC value is driven within 3 clocks.

6.3.5.4 SYNC Timeout

The SYNC value is driven within 3 clocks. If the host observes 3 consecutive clocks without a valid SYNC pattern, it will abort the cycle.

The SCH3221 does not assume any particular timeout. When the host is driving SYNC, it may have to insert a very large number of wait states, depending on PCI latencies and retries.

6.3.5.5 SYNC Patterns and Maximum Number of SYNCS

If the SYNC pattern is 0101, then the host assumes that the maximum number of SYNCs is 8.

If the SYNC pattern is 0110, then no maximum number of SYNCs is assumed. The SCH3221 has protection mechanisms to complete the cycle.

6.3.5.6 SYNC Error Indication

The SCH3221 reports errors via the LAD[3:0] = 1010 SYNC encoding.

If the host was reading data from the SCH3221, data will still be transferred in the next two nibbles. This data may be invalid, but it will be transferred by the SCH3221. If the host was writing data to the SCH3221, the data had already been transferred.

In the case of multiple byte cycles, such as DMA cycles, an error SYNC terminates the cycle. Therefore, if the host is transferring 4 bytes from a device, if the device returns the error SYNC in the first byte, the other three bytes will not be transferred.

6.3.5.7 Reset Policy

The following rules govern the reset policy:

1. When PCI_RESET# goes inactive (high), the clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.
2. When PCI_RESET# goes active (low):
   a) the host drives the LFRAME# signal high, tristates the LAD[3:0] signals, and ignores the LDRQ# signal.
   b) the SCH3221 ignores LFRAME#, tristate the LAD[3:0] pins and drive the LDRQ# signal inactive (high).

6.3.6 LPC TRANSFERS

6.3.6.1 Wait State Requirements

I/O Transfers

For I/O transfers in which long indeterminate wait states are required (i.e., IrCC transfers) the sync pattern of 0110 is used and a large number of syncs may be inserted (up to 330 which corresponds to a timeout of 10us).

Note:	Wait states are required for all I/O transfers. Three wait states are required for an I/O read and two wait states are required for an I/O write. A SYNC of 0110 is used for all I/O transfers.

DMA Transfers

The SCH3221 inserts three wait states for a DMA read and four wait states for a DMA write cycle. A SYNC of 0101 is used for all DMA transfers.

Note 6-4 Long sync cycles are always followed by one ready sync cycle (0\H).

See the example timing for the LPC cycles in Section 10.0, "Timing Diagrams".

6.4 Serial Port (UART)

The SCH3221 incorporates four full function UARTs. They are compatible with the 16450, the 16450 ACE registers and the 16C550A. The UARTS perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt. The second UART also supports IrDA 1.2 (4Mbps), HP-SIR, ASK-IR and Consumer IR infrared modes of operation.

6.4.1 REGISTER DESCRIPTION

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The SCH3221 contains two serial ports, each of which contain a register set as described below.

TABLE 6-4: ADDRESSING THE SERIAL PORT

DLAB*	A2	A1	A0	Register Name
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

Note 6-5 DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

6.4.1.1 Receive Buffer Register (RB)

Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

6.4.1.2 Transmit Buffer Register (TB)

Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

6.4.1.3 Interrupt Enable Register (IER)

Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the SCH3221. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0

This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

Bit 1

This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2

This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3

This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7

These bits are always logic "0".

6.4.1.4 FIFO Control Register (FCR)

Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported. The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (CR15) and UART2 FIFO Control Shadow Register (CR16). See the Configuration section for description on these registers.

Bit 0

Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1

Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2

Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3

Writing to this bit has no effect on the operation of the UART. DMA modes are not supported in this chip.

Bit 4,5

Reserved

Bit 6,7

These bits are used to set the trigger level for the RCVR FIFO interrupt.

Bit 7	Bit 6	RCVR FIFO Trigger Level (Bytes)
0	0	1
0	1	4
1	0	8
1	1	14

6.4.1.5 Interrupt Identification Register (IIR)

Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Bits 1 and 2

These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

Bit 3

In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5

These bits of the IIR are always logic "0".

Bits 6 and 7

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

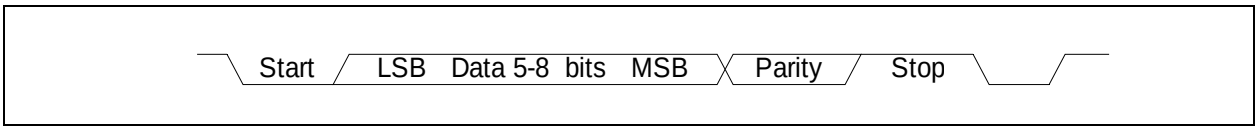
TABLE 6-5: INTERRUPT CONTROL TABLE

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

6.4.1.6 Line Control Register (LCR)

Address Offset = 3H, DLAB = 0, READ/WRITE

FIGURE 6-1: SERIAL DATA



This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1

These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

The Start, Stop and Parity bits are not included in the word length.

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2

This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

Bit 2	Word Length	Number of Stop Bits
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3

Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4

Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

Bit 5

Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled.

Bit 6

Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7

Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

6.4.1.7 Modem Control Register (MCR)

Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0

This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

Bit 1

This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2

This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3

Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4

This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State(logic "1").
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7

These bits are permanently set to logic zero.

6.4.1.8 Line Status Register (LSR)

Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0

Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1

Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrunn error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2

Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Bit 3

Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4

Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

Note:	Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5

Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6

Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty.

Bit 7

This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

6.4.1.9 Modem Status Register (MSR)

Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0

Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1

Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2

Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

Bit 3

Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

Note:	Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4

This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

Bit 5

This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

Bit 6

This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Bit 7

This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

6.4.1.10 Scratchpad Register (SCR)

Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

6.4.2 PROGRAMMABLE BAUD RATE GENERATOR (AND DIVISOR LATCHES DLH, DLL)

The Serial Ports contains a programmable Baud Rate Generator that is capable of dividing the internal PLL clock by any divisor from 1 to 65535. The internal PLL clock is divided down to generate a 1.8462MHz frequency for Baud Rates less than 38.4k, a 1.8432MHz frequency for 115.2k, a 3.6864MHz frequency for 230.4k and a 7.3728MHz frequency for 460.8k. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.

Table 6-6 shows the baud rates possible.

6.4.3 EFFECT OF THE RESET ON REGISTER FILE

The Reset Function (Table 6-7) details the effect of the Reset input on each of the registers of the Serial Port.

6.4.4 FIFO INTERRUPT MODE OPERATION

a) When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

b) The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.

c) The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.

d) The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.

e) The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

a) A FIFO timeout interrupt occurs if all the following conditions exist:
- At least one character is in the FIFO.
- The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay).
- The most recent CPU read of the FIFO was longer than 4 continuous character times ago.
- This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12 bit character.

b) Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate.

c) When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

d) When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

a) The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

b) The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

6.4.5 FIFO POLLED MODE OPERATION

With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

Bit 0=1 as long as there is one byte in the RCVR FIFO.

Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.

Bit 5 indicates when the XMIT FIFO is empty.

Bit 6 indicates that both the XMIT FIFO and shift register are empty.

Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

TABLE 6-6: BAUD RATES

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual (Note 6-6)	High Speed Bit (Note 6-7)
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note 6-6 The percentage error for all baud rates, except where indicated otherwise, is 0.2%.

Note 6-7 The High Speed bit is located in the Device Configuration Space.

TABLE 6-7: RESET FUNCTION TABLE

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High

TABLE 6-7: RESET FUNCTION TABLE (CONTINUED)

Register/Signal	Reset Control	Reset State
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low
XMIT FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low

TABLE 6-8: REGISTER SUMMARY FOR AN INDIVIDUAL UART CHANNEL

Register Address (Note 6-8)	Register Name	Register Symbol	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 6-9)	Data Bit 1	Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1	Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit	Interrupt ID Bit	Interrupt ID Bit (Note 6-13)	0	0	FIFOs Enabled (Note 6-13)	FIFOs Enabled (Note 6-13)
ADDR = 2	FIFO Control Register (Write Only)	FCR (Note 6-15)	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select (Note 6-14)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)	Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)	OUT1 (Note 6-11)	OUT2 (Note 6-11Note 6-11	Loop	0	0	0
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)	Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 6-10)	Error in RCVR FIFO (Note 6-13)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)	Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)

TABLE 6-8: REGISTER SUMMARY FOR AN INDIVIDUAL UART CHANNEL (CONTINUED)

Register Address (Note 6-8)	Register Name	Register Symbol	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
ADDR = 7	Scratch Register (Note 6-13)	SCR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 6-8 DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 6-9 Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 6-10 When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Note 6-11 This bit no longer has a pin associated with it.

Note 6-12 When operating in the XT mode, this register is not available.

Note 6-13 These bits are always zero in the non-FIFO mode.

Note 6-14 Writing a one to this bit has no effect. DMA modes are not supported in this chip.

Note 6-15 The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (CR15) and UART2 FIFO Control Shadow Register (CR16).

6.4.6 NOTES ON SERIAL PORT OPERATION

6.4.6.1 FIFO Mode Operation

General

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

6.4.6.2 TX and RX FIFO Operation

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. The UART will prevent loads to the Tx FIFO if it currently holds 16 characters. Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

6.5 Infrared Interface

The SCH3221 infrared interface provides a two-way wireless communications port using infrared as the transmission medium. Several infrared protocols have been provided in this implementation including IrDA v1.2 (SIR/FIR), ASKIR, and Consumer IR (Figure 6-2). For more information, consult the Infrared Communication Controller (IRCC) specification.

The IrDA v1.0 (SIR) and ASKIR formats are driven by the ACE registers found in UART2. The UART2 registers are described in “Serial Port (UART)” section. The base address for UART2 is programmed in CR25, the UART2 Base Address Register (see CR25 subsection in the Configuration section).

The IrDA V1.2 (FIR) and Consumer IR formats are driven by the SCE registers. Descriptions of these registers can be found in the Infrared Communications Controller Specification. The Base Address for the SCE registers is programmed in CR2B, the SCE Base Address Register (see CR28 subsection in the Configuration section).

6.5.1 IRDA SIR/FIR AND ASKIR

IrDA SIR (v1.0) specifies asynchronous serial communication at baud rates up to 115.2Kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a single infrared pulse at the beginning of the serial bit time. A one is signaled by the absence of an infrared pulse during the bit time. Please refer to “Timing Diagrams” section for the parameters of these pulses and the IrDA waveforms.

IrDA FIR (v1.2) includes IrDA v1.0 SIR and additionally specifies synchronous serial communications at data rates up to 4Mbps.

Data is transferred LSB first in packets that can be up to 2048 bits in length. IrDA v1.2 includes 576Mbps and 1.152Mbps data rates using an encoding scheme that is similar to SIR. The 4Mbps data rate uses a pulse position modulation (PPM) technique.

The ASKIR infrared allows asynchronous serial communication at baud rates up to 19.2Kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a 500KHz carrier waveform for the duration of the serial bit time. A one is signaled by the absence of carrier during the bit time. Refer to “Timing Diagrams” section for the parameters of the ASKIR waveforms.

6.5.2 CONSUMER IR

The SCH3221 Consumer IR interface is a general-purpose Amplitude Shift Keyed encoder/decoder with programmable carrier and bit-cell rates that can emulate many popular TV Remote encoding formats; including, 38KHz PPM, PWM and RC-5. The carrier frequency is programmable from 1.6MHz to 6.25KHz. The bit-cell rate range is 100KHz to 390Hz.

6.5.3 HARDWARE INTERFACE

The SCH3221 IR hardware interface is shown in Figure 6-2. This interface supports two types of external FIR transceiver modules. One uses a mode pin (IR Mode) to program the data rate, while the other has a second Rx data pin (IRRX3). These functions are selected through CR29 as shown in Table 6-9.

TABLE 6-9: FIR TRANSCEIVER MODULE-TYPE SELECT

HP Mode (Note 6-16)	Function
0	IR Mode
1	IRRX3

Note 6-16 HPMODE is CR29, BIT 4 (see CR29 subsection in the Configuration section). Refer to the Infrared Interface Block Diagram on the following page for HPMODE implementation.

The FAST bit is used to select between the SIR mode and FIR mode receiver, regardless of the transceiver type. If FAST = 1, the FIR mode receiver is selected; if FAST = 0, the SIR mode receiver is selected (Table 6-10, "IR Rx Data Pin Selection").

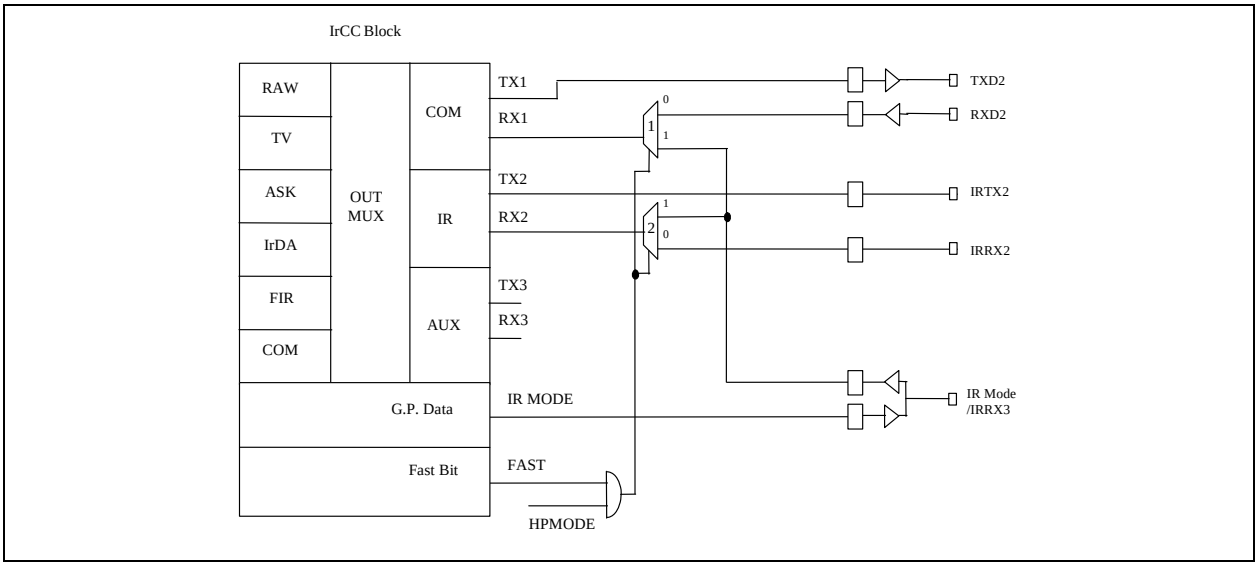
TABLE 6-10: IR RX DATA PIN SELECTION

Control Signal		Inputs	
Fast	**HP Mode**	**RX1**	**RX2**
0	X	RX1=RXD2	RX2=IRRX2
X	0	RX1=RXD2	RX2=IRRX2
1	1	RX1=IR Mode/IRRX3	RX2=IR Mode/IRRX3

6.5.4 IR HALF DUPLEX TURNAROUND DELAY TIME

If the Half Duplex option is chosen there is an IR Half Duplex Time-out that constrains IRCC direction mode changes. This time-out starts as each bit is transferred and prevents direction mode changes until the time-out expires. The timer is restarted whenever new data arrives in the current direction mode. For example, if data is loaded into the transmit buffer while a character is being received, the transmission will not start until the last bit has been received and the time-out expires. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received. The Half Duplex Time-out is programmable from 0 to 25.5ms in 100 s increments. (See subsection CR2D in the Configuration section.)

FIGURE 6-2: INFRARED INTERFACE BLOCK DIAGRAM



6.5.5 IR TRANSMIT PINS

The IR transmit signal may be brought out onto the GP53/TXD2/IRTX pin or the GP21/IRTX2/WDT pin. These pins, which are not powered by VTR, function as described below.

The following defines the acceptable states for the GP53/TXD2/IRTX output pin following a VCC POR or Hard Reset.

- If VCC=0V the GP53/TXD2/IRTX pin will be tristate.
- If VCC>2.4V and TXD2/IRTX functions are selected the following states are possible.
  - If UART2 Power bit = 0 **OR** bits[7:6] IR Output Mux EQUAL ‘11’ at offset CR0A the output will be tristate
  - If UART2 Power bit = 1 **AND** bits[7:6] IR Output Mux EQUAL ‘00’ at offset CR0A **AND** the transmit buffer is empty the output will be set to the inactive state.
  - If UART2 Power bit = 1 **AND** bits[7:6] IR Output Mux EQUAL ‘00’ at offset CR0A **AND** the transmit buffer has data and is ready to transmit the output will reflect the state of the data being transmitted.
  - If UART2 Power bit = 1 **AND** bits[7:6] IR Output Mux EQUAL ‘01’ at offset CR0A the output will be low.
- If VCC>2.4V and GP53 function is selected the pin will reflect the current state of GP53.

The following defines the acceptable states for the GP21/IRTX2/WDT output pin following a VCC POR or Hard Reset.

- If VCC=0V the GP21/IRTX2/WDT pin will be tristate.
- If VCC>2.4V and IRTX2 function is selected the following states are possible.
  - If bits[7:6] IR Output Mux EQUAL ‘11’ at offset CR0A the output will be tristate
  - If UART2 Power bit = 0 AND bits[7:6] IR Output Mux NOT EQUAL ‘11’ at offset CR0A the output will be low.
  - If UART2 Power bit = 1 AND bits[7:6] IR Output Mux EQUAL ‘01’ at offset CR0A AND the transmit buffer is empty the output will be set to the inactive state.
  - If UART2 Power bit = 1 AND bits[7:6] IR Output Mux EQUAL ‘01’ at offset CR0A AND the transmit buffer has data and is ready to transmit the output will reflect the state of the data being transmitted.
  - If UART2 Power bit=1 AND bits[7:6] IR Output Mux EQUAL ‘00’ the output will be low.
- If VCC>2.4V and GP21 function is selected the pin will reflect the current state of GP21.
- If VCC>2.4 and WDT function is selected the pin will reflect the current state of the WDT.

Note:	The inactive state for GP53/TXD2/IRTX pin or GP21/IRTX2/WDT pin is determined by a combination of the mode selected and the function enabled on the pin. If the TXD2/IRTX or IRTX2 functions are enabled the inactive state is determined by the IR Output Mux bits located in CR0A IR MUX register and the UART Mode register located at CR0C.

6.6 Watchdog Timer

The SCH3221's Watchdog Timer (WDT) has a programmable time-out ranging from 1 to 255 minutes with one minute resolution, or 1 to 255 seconds with 1 second resolution. The units of the WDT timeout value are selected via bit[7] of the WDT_TIMEOUT register (Runtime Register at offset 0x11). The WDT time-out value is set through the WDT_VAL Runtime register. Setting the WDT_VAL register to 0x00 disables the WDT function (this is its power on default). Setting the WDT_VAL to any other non-zero value will cause the WDT to reload and begin counting down from the value loaded. When the WDT count value reaches zero the counter stops and sets the Watchdog time-out status bit in the WDT_CTRL Runtime register. Note: Regardless of the current state of the WDT, the WDT time-out status bit can be directly set or cleared by the Host CPU.

The Watchdog Timer may be configured to generate an interrupt on the rising edge of the Time-out status bit. This interrupt can be used to generate an IO_PME#, an IO_SMI#, a signal on the WDT output pin, or it may be mapped onto the Serial IRQ stream. The following list describes the registers used to enable these events.

Note:

- The WDT, PME, and SMI registers are located in the Runtime Register block.
- The WDT defaults to generating an active high signal. The polarity of this output may be inverted to generate an active low signal through bit[1] GP21 located in GPIO Polarity Register 2 at offset CR34.

Four methods of enabling Watchdog Timer interrupt events:

1. The WDT can generate an IO_PME#. If a watchdog timer event occurs the WDT status bit in the PME_STS2 register at offset 0x03 will be set. If bit[0] PME_En in the PME_En registers at offset 0x01 is set to ‘1’ and bit[7] WDT in the PME_EN2 register at offset 0x06 is set to ‘1’ an interrupt will be generated on the IO_PME# pin.
2. The WDT can generate an IO_SMI#. If a watchdog timer event occurs the WDT status bit in the SMI_STS3 register at offset 0x18 will be set. If bits[5:4] GP12 Alternate Function Select in the GPIO Alternate Function Select Register 1 at offset CR44 are set to ‘01’ and bit[0]EN_WDT in the SMI_EN3 at offset 0x19 is set to ‘1’ an interrupt will be generated on the IO_SMI# pin.
3. The WDT can generate a signal on the GP21/IRTX2/WDT pin. If a watchdog timer event occurs and bits[3:2] GP21 Alternate Function Select in the GPIO Alternate Function Select Register 3 at offset CR46 are set to ‘10’ an interrupt will be generated on the WDT pin.
4. The WDT can generate an interrupt on the Serial IRQ stream. If a watchdog timer event occurs and bits[7:4] WDT Interrupt Mapping located in the WDT_CFG register at offset 0x13 are programmed to a value other than ‘0000’ an interrupt will be generated on the SER_IRQ output pin. See Section 6.9, "Serial IRQ," on page 39 for a description of generating interrupts on the SER_IRQ pin.

The host may force a Watchdog time-out to occur by writing a "1" to bit 2 of the WDT_CTRL (Force WD Time-out) Runtime register. Writing a "1" to this bit forces the WDT count value to zero and sets bit 0 of the WDT_CTRL (Watchdog Status). Bit 2 of the WDT_CTRL is self-clearing. See Section 7.0, "Runtime Registers," on page 52 for description of these registers.

6.7 LED Functionality

The SCH3221 provides LED functionality on two pins:

- GP13/IRQIN1/LED1
- GP23/LED2/IRQIN2

The LED logic and supporting registers are powered by VTR. The LED1 pin is powered by VCC and the LED2 pin is powered by VTR. These pins can be configured to turn an LED on and off and blink independent of each other through the LED1 and LED2 runtime registers at offset 0x15 and 0x16, when the device is powered by VCC. See Section 7.0, "Runtime Registers" for a description of these registers.

The LED2 pin (GP23) is capable of controlling an LED while the device is under VTR power with VCC removed. In order to control an LED while the part is under VTR power, the GPIO pin must have been configured for the LED2 function while the device was powered by VCC.

Note:

- The LED2 pin will not support the blink function under VTR power (VCC removed) if an external 32kHz clock source is not connected.
- LED1 and LED2 may be configured for either open drain or push-pull buffer type. In the case of open-drain buffer type, the pin is capable of sinking current to control the LED. In the case of push-pull buffer type the part will source current.

6.8 Power Management

Power management capabilities are provided for UARTs 1--4. For each of these logical devices, two types of power management are provided: direct powerdown and auto powerdown.

6.8.1 UART POWER MANAGEMENT

Direct power management is controlled by CR02. Refer to the Configuration section for more information.

Auto Power Management may be enabled by the UART1, UART2, UART3, or UART4 enable bits in CR07. When set, these bits allow the following auto power management operations:

1. The transmitter enters auto powerdown when the transmit buffer and shift register are empty.
2. The receiver enters powerdown when the following conditions are all met:
   a) Receive FIFO is empty.
   b) The receiver is waiting for a start bit.

Note: While in powerdown the Ring Indicator interrupt is still valid and transitions when the RI input changes.

6.8.1.1 Exit Auto Powerdown

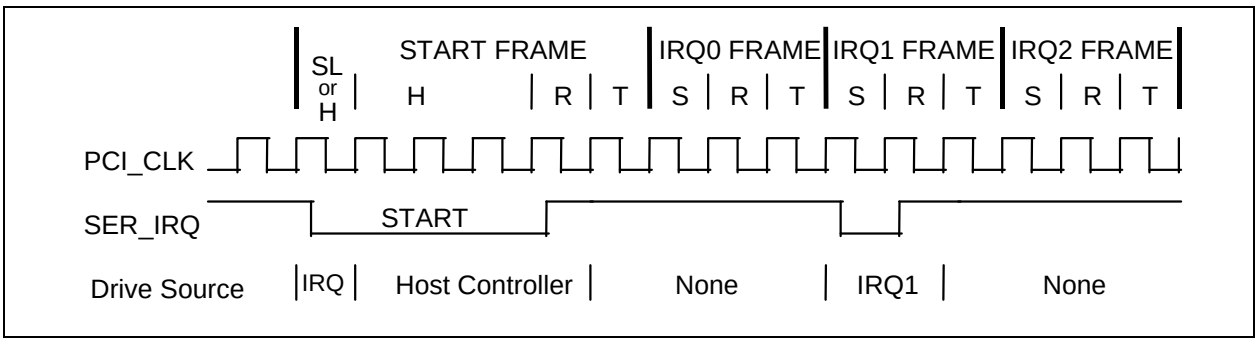
The transmitter exits powerdown on a write to the XMIT buffer. The receiver exits auto powerdown when RXDx changes state.

6.9 Serial IRQ

The SCH3221 supports the serial interrupt to transmit interrupt information to the host system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems, Version 6.0. The PCI_CLK, SER_IRQ and nCLKRUN pins are used for this interface. The Serial IRQ/CLKRUN Enable bit D7 in CR29 activates the serial interrupt interface.

6.9.1 TIMING DIAGRAMS FOR SER_IRQ CYCLE

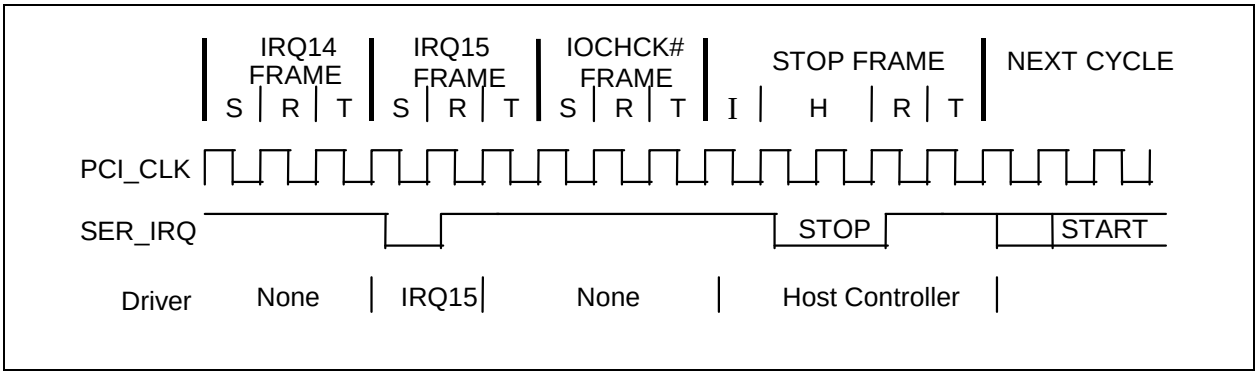
a) Start Frame timing with source sampled a low pulse on IRQ1.



Note: H=Host Control; R=Recovery; T=Turn-Around; SL=Slave Control; S=Sample

Note 6-17 Start Frame pulse can be 4-8 clocks wide depending on the location of the device in the PCI bridge hierarchy in a synchronous bridge design.

b) Stop Frame Timing with Host using 17 SER_IRQ sampling period.



Note: H=Host Control; R=Recovery; T=Turn-Around; S=Sample; I=Idle

Note 6-18 Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.

Note 6-19 There may be none, one or more Idle states during the Stop Frame.

Note 6-20 The next SER_IRQ cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

6.9.1.1 SER_IRQ Cycle Control

There are two modes of operation for the SER_IRQ Start Frame.

1. Quiet (Active) Mode:

Any device may initiate a Start Frame by driving the SER_IRQ low for one clock, while the SER_IRQ is Idle. After driving low for one clock the SER_IRQ is immediately tri-stated without at any time driving high. A Start Frame may not be initiated while the SER_IRQ is Active. The SER_IRQ is Idle between Stop and Start Frames. The SER_IRQ is Active between Start and Stop Frames. This mode of operation allows the SER_IRQ to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated the Host Controller will take over driving the SER_IRQ low in the next clock and will continue driving the SER_IRQ low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the Host Controller will drive the SER_IRQ back high for one clock, then tri-state.

Any SER_IRQ Device (i.e., The SCH3221) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the Host Controller unless the SER_IRQ is already in an SER_IRQ Cycle and the IRQ/Data transition can be delivered in that SER_IRQ Cycle.

2. Continuous (Idle) Mode:

Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other SER_IRQ agents become passive and may not initiate a Start Frame. SER_IRQ will be driven low for four to eight clocks by Host Controller. This mode has two functions. It can be used to stop or idle the SER_IRQ or the Host Controller can operate SER_IRQ in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An SER_IRQ mode transition can only occur during the Stop Frame. Upon reset, SER_IRQ bus is defaulted to Continuous mode, therefore only the Host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next SER_IRQ Cycle's mode.

6.9.1.2 SER_IRQ Data Frame

Once a Start Frame has been initiated, the SCH3221 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase the SCH3221 drives the SER_IRQ low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, SER_IRQ is left tri-stated. During the Recovery phase the SCH3221

drives the SER_IRQ high, if and only if, it had driven the SER_IRQ low during the previous Sample Phase. During the Turn-around Phase the SCH3221 tri-states the SER_IRQ. The SCH3221 will drive the SER_IRQ line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one. (e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, (6 x 3) - 1 = 17th clock after the rising edge of the Start Pulse).

TABLE 6-11: SER_IRQ SAMPLING PERIODS

SER_IRQ Period	Signal Sampled	# of Clocks Past Start
1	Not Used	2
2	IRQ1	5
3	IO_SMI#/IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The SER_IRQ data frame supports IRQ2 from a logical device on Period 3, which can be used for the System Management Interrupt (nSMI). When using Period 3 for IRQ2 the user should mask off the SMI via the SMI Enable Register. Likewise, when using Period 3 for nSMI the user should not configure any logical devices as using IRQ2.

SER_IRQ Period 14 is used to transfer IRQ13. Logical devices Serial Port 1, Serial Port 2, Serial Port 3, Serial Port 4, and WDT have IRQ13 as a choice for their primary interrupt.

The SMI is enabled onto the SMI frame of the Serial IRQ via bit 6 of SMI Enable Register 2 and onto the IO_SMI# pin via bit 7 of the SMI Enable Register 2.

The following devices may be mapped into the Serial IRQ stream.

- Serial Port 1
- Serial Port 2
- Serial Port 3
- Serial Port 4
- WDT

6.9.1.3 Stop Cycle Control

Once all IRQ/Data Frames have completed the Host Controller will terminate SER_IRQ activity by initiating a Stop Frame. Only the Host Controller can initiate the Stop Frame. A Stop Frame is indicated when the SER_IRQ is low for two or three clocks. If the Stop Frame's low time is two clocks then the next SER_IRQ Cycle's sampled mode is the Quiet mode; and any SER_IRQ device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks then the next SER_IRQ Cycle's sampled mode is the Continuous mode; and only the Host Controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

6.9.1.4 Latency

Latency for IRQ/Data updates over the SER_IRQ bus in bridge-less systems with the minimum Host supported IRQ/Data Frames of seventeen, will range up to 96 clocks (3.84μS with a 25MHz PCI Bus or 2.88uS with a 33MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

6.9.1.5 EOI/ISR Read Latency

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the SER_IRQ Cycle latency in order to ensure that these events do not occur out of order.

6.9.1.6 AC/DC Specification Issue

All SER_IRQ agents must drive / sample SER_IRQ synchronously related to the rising edge of PCI bus clock. The SER_IRQ pin uses the electrical specification of PCI bus. Electrical parameters will follow PCI spec. section 4, sustained tri-state.

6.9.1.7 Reset and Initialization

The SER_IRQ bus uses PCI_RESET# as its reset signal. The SER_IRQ pin is tri-stated by all agents while PCI_RESET# is active. With reset, SER_IRQ Slaves are put into the (continuous) IDLE mode. The Host Controller is responsible for starting the initial SER_IRQ Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent SER_IRQ Cycles. It is Host Controller's responsibility to provide the default values to 8259's and other system logic before the first SER_IRQ Cycle is performed. For SER_IRQ system suspend, insertion, or removal application, the Host controller should be programmed into Continuous (IDLE) mode first. This is to ensure SER_IRQ bus is in IDLE state before the system configuration changes.

6.9.2 ROUTABLE IRQ INPUTS

The routable IRQ input (IRQINx) functions are on the pins GP13/IRQIN1/LED1, GP23/nLED2/IRQIN2 and GP20/IRRX2/IRQIN3. The IRQINx pin's IRQ time slot in the Serial IRQ stream is selected via a 4-bit control register for each IRQIN function (CR29 for IRQIN1, CR2A for IRQIN2 and IRQIN3). A value of 0000 disables the IRQ function.

Note:	In order to use an IRQ for one of the IRQINx inputs that are muxed on the GPIO pins, the corresponding IRQ must not be used for any of the devices in the SCH3221. Otherwise contention may occur.

IRQIN1, IRQIN2, and IRQIN3 are capable of generating PME wake events. If an IRQINx pin generates an event, the associated PME Wake Status bit will be set to '1'. The following is a list of the PME status and enable bits associated with the IRQINx pins.

- IRQIN1 will generate an event on bit[3] GP13 of the PME_STS1 register at offset 0x02. If bit[3] GP13 of the PME_EN1 register at offset 0x05 is set to '1' and the PME_EN bit is set to '1' in the PME_EN register offset 0x01 the IO_PME# pin will be asserted.
- IRQIN2 will generate an event on bit[5] GP23 of the PME_STS2 register at offset 0x03. If bit[5] GP23 of the PME_EN2 register at offset 0x06 is set to '1' and the PME_EN bit is set to '1' in the PME_EN register offset 0x01 the IO_PME# pin will be asserted.
- IRQIN3 will generate an event on bit[2] GP20 of the PME_STS2 register at offset 0x03. If bit[2] GP20 of the PME_EN2 register at offset 0x06 is set to '1' and the PME_EN bit is set to '1' in the PME_EN register offset 0x01 the IO_PME# pin will be asserted.

IRQIN1 and IRQIN2 are capable of generating SMI events. If an IRQINx pin generates an event, the associated SMI Status bit will be set to '1'. The following is a list of the SMI status and enable bits associated with the IRQINx pins.

- IRQIN1 will generate an event on bit[3] GP13 of the SMI_STS1 register at offset 0x08. If bit[3] GP13 of the SMI_EN1 register at offset 0x0A is set to '1' the IO_SMI# pin will be asserted.
- IRQIN2 will generate an event on bit[4] GP23 of the SMI_STS2 register at offset 0x09. If bit[4] GP23 of the SMI_EN2 register at offset 0x0B is set to '1' the IO_SMI# pin will be asserted.

Note:	IRQIN3 is not capable of generating an SMI event. The edge is programmable through the polarity bit of the GPIO control register.

APPLICATION NOTE: If GPIO function is selected on GP13/IRQIN1, GP23/nLED2/IRQIN2, or GP20/IRRX2/IRQIN3 pins and if IRQ is selected using the routing registers (CR29 for IRQIN1 and CR2A for IRQIN2 and IRQIN3), IRQs will be generated on the Serial IRQ stream. The state of the GPIO pins will be reflected on the serial IRQ stream. The IRQ selection bits should be '0000' in the IRQ routing registers when GPIO functions are used. These IRQ selection bits default to '0000' on VCC POR.

6.10 PCI CLKRUN Support

6.10.1 OVERVIEW

The SCH3221 supports the PCI CLKRUN# signal. CLKRUN# is used to indicate the PCI clock status as well as to request that a stopped clock be started. The SCH3221 CLKRUN# signal is on pin number 28. See Figure 6-3 for an example of a typical system implementation using CLKRUN#.

If the SCH3221 SIRQ_CLKRUN_EN signal is disabled, it will disable the CLKRUN# support related to LDRQ# in addition to disabling the SER_IRQ and the CLKRUN# associated with SER_IRQ.

CLKRUN# is an open drain output and an input. Refer to the *PCI Mobile Design Guide Rev 1.0* for a description of the CLKRUN# function.

6.10.2 CLKRUN# FOR SERIAL IRQ

The SCH3221 supports the PCI CLKRUN# signal for the Serial IRQs. If an SIO interrupt occurs while the PCI clock is stopped, CLKRUN# is asserted before the serial interrupt signal is driven active.

See Section 6.10.4, "Using CLKRUN#" below for more details.

6.10.3 CLKRUN# FOR LDRQ#

CLKRUN# support is also provided in the SCH3221 for the LDRQ# signal. If a device requests DMA service while the PCI clock is stopped, CLKRUN# is asserted to restart the PCI clock. This is required to drive the LDRQ# signal active.

See Section 6.10.4 below for more details.

6.10.4 USING CLKRUN#

If CLKRUN# is sampled "high", the PCI clock is stopped or stopping. If CLKRUN# is sampled "low", the PCI clock is starting or started (running). If a device in the SCH3221 asserts or de-asserts an interrupt or asserts a DMA request, and CLKRUN# is sampled "high", the SCH3221 requests the restoration of the clock by asserting the CLKRUN# signal asynchronously (Table 6-12). The SCH3221 holds CLKRUN# low until it detects two rising edges of the clock. After the second clock edge, the SCH3221 disables the open drain driver (Figure 6-4).

The SCH3221 will not assert CLKRUN# under any conditions if SIRQ_CLKRUN_EN is inactive ("0"). The SIRQ_-CLKRUN_EN bit is D7 in CR29.

The SCH3221 will not assert CLKRUN# if it is already driven low by the central resource; i.e., the PCI CLOCK GENERATOR in Figure 6-3. The SCH3221 will not assert CLKRUN# unless the line has been deasserted for two successive clocks; i.e., before the clock was stopped (Figure 6-4).

TABLE 6-12: SCH3221 CLKRUN# FUNCTION

SIRQ_CLKRUN_EN	Internal Interrupts/ DMA Requests	CLKRUN#	Action
0	X	X	None
1	NO CHANGE	X	None
	CHANGE/ASSERTION (Note 6-21)	0	None
		1	Assert CLKRUN# (Note 6-22)

Note 6-21 "Change/Assertion" means either-edge change on any internal IRQs routed to the SIRQ block or assertion of an internal DMA request by a device in SCH3221. The "assertion" detection logic runs asynchronously to the PCI Clock and regardless of the Serial IRQ mode; i.e., "continuous" or "quiet".

Note 6-22 The CLKRUN# signal is '1' for at least two consecutive clocks before SCH3221 asserts ('0') it.

FIGURE 6-3: CLKRUN# SYSTEM IMPLEMENTATION EXAMPLE

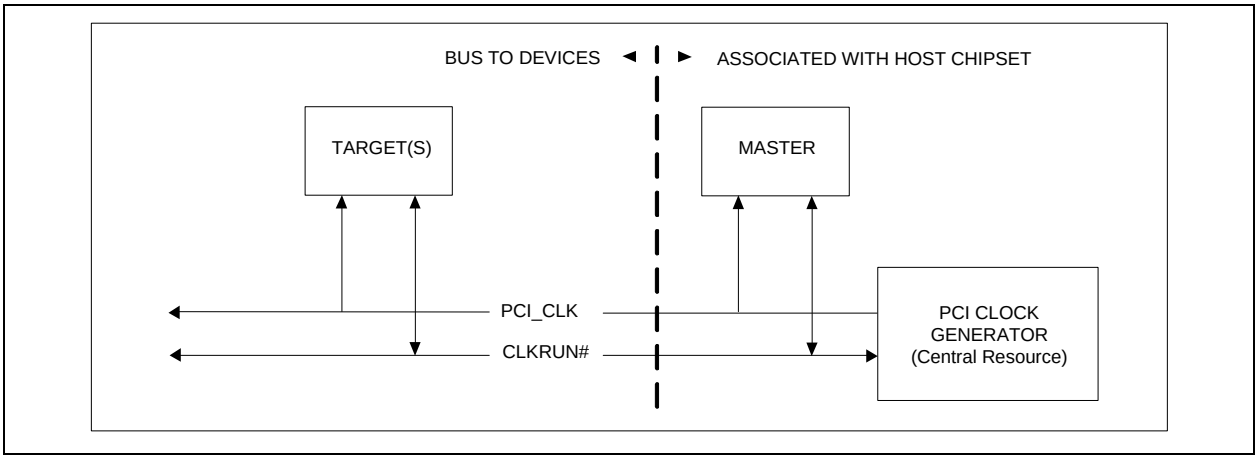
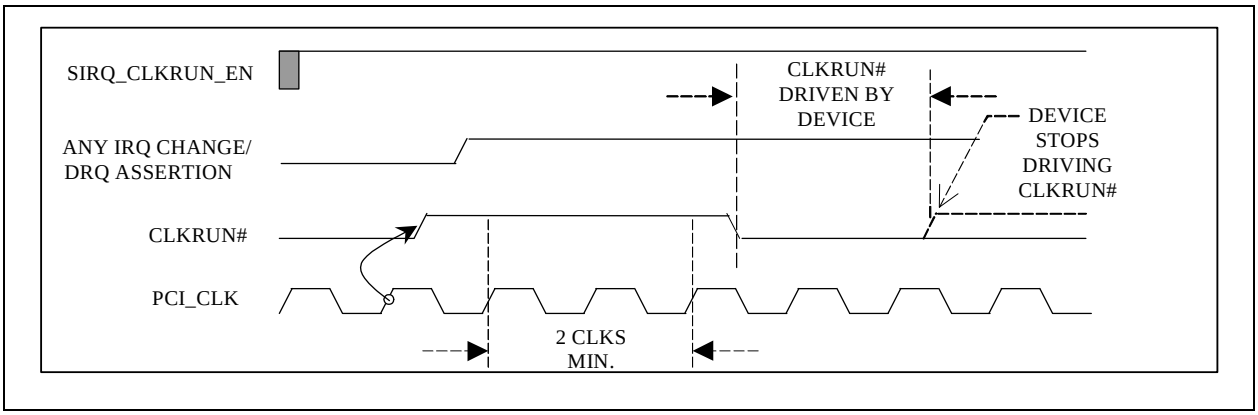


FIGURE 6-4: CLOCK START ILLUSTRATION



Note 6-23 The signal “ANY IRQ CHANGE/DRQ ASSERTION” is the same as “CHANGE/ASSERTION” in Table 6-12, "SCH3221 CLKRUN# Function".

Note 6-24 The SCH3221 continually monitors the state of CLKRUN# to maintain the PCI Clock until an active “ANY IRQ CHANGE/DRQ ASSERTION” condition has been transferred to the host in a SER_IRQ/DMA cycle. For example, if “ANY IRQ CHANGE/DRQ ASSERTION” is asserted before CLKRUN# is de-asserted (not shown in Figure 6-4), the SCH3221 must assert CLKRUN# as needed until the SER_IRQ/DMA cycle has completed.

6.11 General Purpose I/O

The SCH3221 provides a set of flexible Input/Output control functions to the system designer through the 33 independently programmable General Purpose I/O pins (GPIO). The GPIO pins can perform basic I/O and many of them can be individually enabled to generate an SMI and a PME.

6.11.1 GPIO PINS

The following pins include GPIO functionality as defined in the table below.

TABLE 6-13: GPIO PIN FUNCTIONALITY

Name	Power Well	Default on VTR POR	Default on VCC POR	GPIO PME/SMI Function
GP11	VCC (Note 6-25)	GPIO Input	Programmable	PME/SMI
GP23/LED2/IRQIN2	VTR (Note 6-25)	GPIO Input	Programmable	PME/SMI
GP30/nRI3	VCC (Note 6-25, Note 6-26)	GPIO Input	Programmable	PME
GP31/nDCD3	VCC (Note 6-25)	GPIO Input	Programmable	PME
GP32/nRXD3	VCC (Note 6-25)	GPIO Input	Programmable	PME
GP33/nTXD3	VCC (Note 6-25)	GPIO Input	Programmable	PME
GP34/nDSR3	VCC (Note 6-25)	GPIO Input	Programmable	PME
GP35/nRTS3	VCC (Note 6-25)	GPIO Input	Programmable	PME
GP36/nCTS3	VCC (Note 6-25)	GPIO Input	Programmable	PME
GP37/nDTR3	VCC (Note 6-25)	GPIO Input	Programmable	PME
GP40/nRI4	VCC (Note 6-26)	GPIO Input	Programmable	PME
GP41/nDCD4	VCC	GPIO Input	Programmable	-
GP42/nRXD4	VCC	GPIO Input	Programmable	-
GP43/nTXD4	VCC	GPIO Input	Programmable	-
GP44/nDSR4	VCC	GPIO Input	Programmable	-
GP45/nRTS4	VCC	GPIO Input	Programmable	-
GP46/nCTS4	VCC	GPIO Input	Programmable	-
GP47/nDTR4	VCC	GPIO Input	Programmable	-
GP12/IO_SMI#	VCC (Note 6-25)	GPIO Input	Programmable	IO_SMI#/ PME/SMI
GP13/IRQIN1/LED1	VCC (Note 6-25)	GPIO Input	Programmable	PME/SMI
GP16	VCC (Note 6-25)	Floating non-GPIO Output	Programmable	PME/SMI
GP17	VCC (Note 6-25)	Floating non-GPIO Output	Programmable	PME/SMI
GP20/IRRX2/IRQIN3	VCC (Note 6-25)	GPIO Input	Programmable	PME
GP21/IRTX2/WDT	VCC (Note 6-25)	GPIO Input	Programmable	PME
GP22/IRMODE/IRRX3	VCC (Note 6-25)	GPIO Input	Programmable	PME
GP50/nRI2	VCC (Note 6-26)	GPIO Input	Programmable	PME
GP51/nDCD2	VCC	GPIO Input	Programmable	-
GP52/RXD2/IRRX	VCC	GPIO Input	Programmable	-
GP53/TXD2/IRTX	VCC	GPIO Input	Programmable	-
GP54/nDSR2	VCC	GPIO Input	Programmable	-
GP55/nRTS2	VCC	GPIO Input	Programmable	-

TABLE 6-13: GPIO PIN FUNCTIONALITY (CONTINUED)

Name	Power Well	Default on VTR POR	Default on VCC POR	GPIO PME/SMI Function
GP56/nCTS2	VCC	GPIO Input	Programmable	-
GP57/nDTR2	VCC	GPIO Input	Programmable	-

Note 6-25 These pins have input buffers into the wakeup logic that are powered by VTR.

Note 6-26 This pin has an input buffer into the wakeup logic that are powered by VTR to support the nRI function.

6.11.2 DESCRIPTION

Each GPIO port has a 1-bit data register. GPIOs are controlled by GPIO control registers located in the Configuration section. The data register for each GPIO port is represented as a bit in one of the 8-bit GPIO DATA Registers, GP1 to GP5. The bits in these registers reflect the value of the associated GPIO pin as follows. Pin is an input: The bit is the value of the GPIO pin. Pin is an output: The value written to the bit goes to the GPIO pin. Latched on read and write. The GPIO data registers are located in the Runtime Register block; see the Runtime Registers section. The GPIO ports with their alternate functions and configuration state register addresses are listed in Table 6-14.

TABLE 6-14: GENERAL PURPOSE I/O PORT ASSIGNMENTS

Default Function	ALT. FUNC. 1	ALT. FUNC. 2	ALT. FUNC. 3	Data Register (Note 6-27)	Data Register Bit No.	Register Offset (HEX)
Reserved				GP1	0	0C
GPIO					1	
GPIO	IO_SMI#				2	
GPIO	IRQIN1	nLED1			3	
Reserved					4	
Reserved					5	
Reserved	GPIO				6	
Reserved	GPIO				7	
GPIO	IRRX2	IRQIN3		GP2	0	0D
GPIO	IRTX2	WDT			1	
GPIO	IRMODE	IRRX3			2	
GPIO	nLED2	IRQIN2			3	
Reserved					4	
Reserved					5	
Reserved					6	
Reserved					7	
GPIO	nRI3			GP3	0	0E
GPIO	nDCD3				1	
GPIO	nRXD3				2	
GPIO	nTXD3				3	
GPIO	nDSR3				4	
GPIO	nRTS3				5	
GPIO	nCTS3				6	
GPIO	nDTR3				7	

TABLE 6-14: GENERAL PURPOSE I/O PORT ASSIGNMENTS (CONTINUED)

Default Function	ALT. FUNC. 1	ALT. FUNC. 2	ALT. FUNC. 3	Data Register (Note 6-27)	Data Register Bit No.	Register Offset (HEX)
GPIO	nRI4			GP4	0	0F
GPIO	nDCD4				1	
GPIO	nRXD4				2	
GPIO	nTXD4				3	
GPIO	nDSR4				4	
GPIO	nRTS4				5	
GPIO	nCTS4				6	
GPIO	nDTR4				7	
GPIO	nRI5			GP5	0	0F
GPIO	nDCD5				1	
GPIO	nRXD5				2	
GPIO	nTXD5				3	
GPIO	nDSR5				4	
GPIO	nRTS5				5	
GPIO	nCTS5				6	
GPIO	nDTR5				7	

Note 6-27 The GPIO Data Registers are located at the offset shown from the RUNTIME REGISTERS BLOCK address.

6.11.3 GPIO CONTROL

Each GPIO port has an 8-bit control register that controls the behavior of the pin. These registers are defined in the Configuration section of this specification.

Each GPIO port may be configured as either an input or an output. If the pin is configured as an output, it can be programmed as open-drain or push-pull. Inputs and outputs can be configured as non-inverting or inverting. GPIO Direction Registers determine the port direction, GPIO Polarity Registers determine the signal polarity, and GPIO Output Type Register determines the output driver type select. The GPIO Output Type Registers (CR39, CR40, CR41) apply to certain GPIOs (GP11-GP13, GP16-GP17, GP20, GP21, GP23, and GP50-GP57). The GPIO Direction, Polarity and Output Type Registers control the GPIO pin when the pin is configured for the GPIO function and when the pin is configured for the alternate function for all pins.

The basic GPIO configuration options are summarized in Table 6-15.

TABLE 6-15: GPIO CONFIGURATION SUMMARY

Selected Function	Direction Bit	Polarity Bit	Description
	B0	B1	
GPIO	0	0	Pin is a non-inverted output.
	0	1	Pin is an inverted output.
	1	0	Pin is a non-inverted input.
	1	1	Pin is an inverted input.

6.11.4 GPIO OPERATION

The operation of the GPIO ports is illustrated in Figure 6-5.

FIGURE 6-5: GPIO FUNCTION

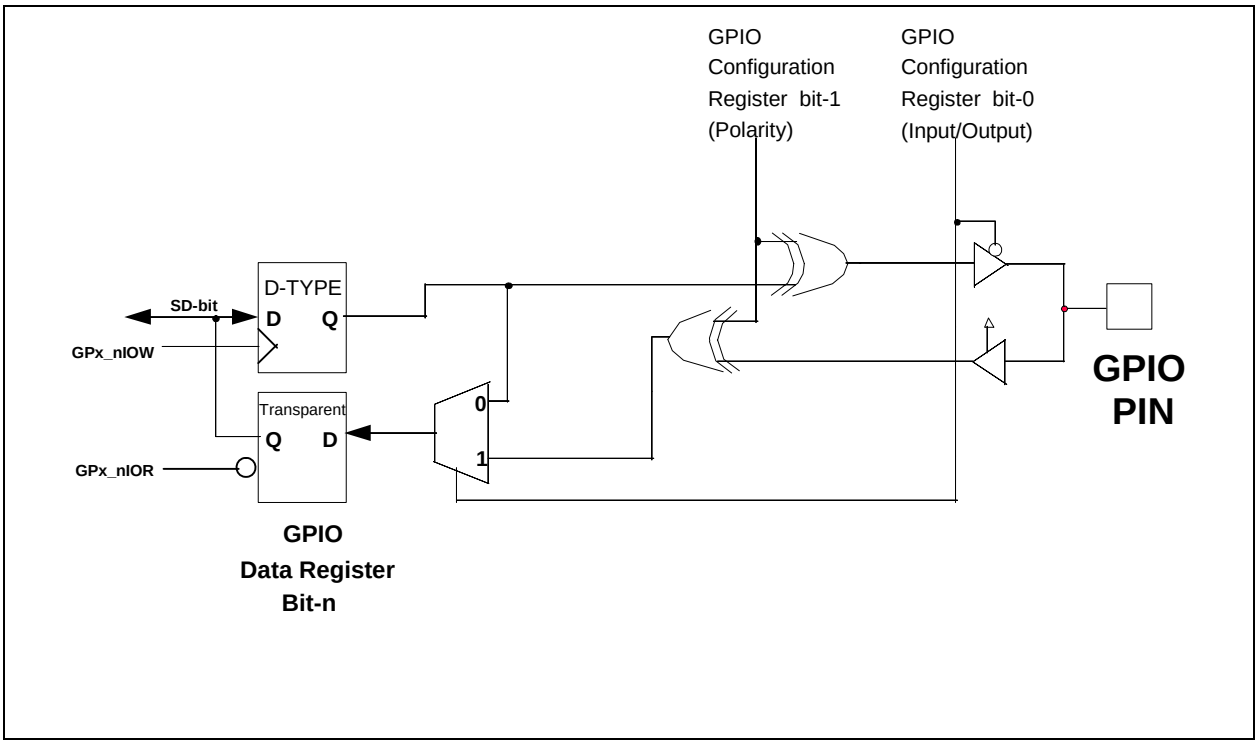


Figure 6-5 is for illustration purposes only and in not intended to suggest specific implementation details.

When a GPIO port is programmed as an input, reading it through the GPIO data register latches either the inverted or non-inverted logic value present at the GPIO pin. Writing to a GPIO port that is programmed as an input has no effect (Table 6-16).

When a GPIO port is programmed as an output, the logic value or the inverted logic value that has been written into the GPIO data register is output to the GPIO pin. Reading from a GPIO port that is programmed as an output returns the last value written to the data register (Table 6-16).

TABLE 6-16: GPIO READ/WRITE BEHAVIOR

Host Operation	GPIO Input Port	GPIO Output Port
READ	LATCHED VALUE OF GPIO PIN	LAST WRITE TO GPIO DATA REGISTER
WRITE	NO EFFECT	BIT PLACED IN GPIO DATA REGISTER

The SCH3221 provides 20 GPIOs that can directly generate a PME. See the table in the next section. The GPIO Polarity Registers in the Configuration section select the edge on these GPIO pins that will set the associated status bit in the PME_STS1 – PME_STS4 registers. The default is the low-to-high edge. If the corresponding enable bit in the PME_EN1 – PME_EN4 registers and the PME_EN bit in the PME_EN register is set, a PME will be generated. These registers are located in the Runtime Registers Block, which is located at the address contained in the configuration registers CR30. The PME status bits for the GPIOs are cleared on a write of ‘1’. In addition, the SCH3221 provides 6 GPIOs that can directly generate an SMI. See the table in the next section.

6.11.5 GPIO, PME AND SMI FUNCTIONALITY

The following GPIOs are dedicated wakeup GPIOs with a status and enable bit in the PME status and enable registers:

- GP11-GP13
- GP16-GP17
- GP20-GP23
- GP30-GP37
- GP40
- GP50

This following is the list of PME status and enable registers for their corresponding GPIOs:

- PME_STS1 and PME_EN1 for GP11-GP13 and GP16-GP17
- PME_STS2 and PME_EN2 for GP20-GP23 and GP50
- PME_STS3 and PME_EN3 for GP30-GP37
- PME_STS4 and PME_EN4 for GP30 and GP40

The following GPIOs can directly generate an SMI and have a status and enable bit in the SMI status and enable registers.

- GP11-GP13
- GP16-GP17
- GP23

The following SMI status and enable registers for these GPIOs:

- SMI_STS1 and SMI_EN1 for GP11-GP13 and GP16-GP17
- SMI_STS2 and SMI_EN2 for GP23

TABLE 6-17: PME AND SMI FUNCTIONALITY FOR EACH GPIO

GPIO	PME	SMI	Output Buffer Power	Notes
GP11	Yes	Yes	VCC	
GP12	Yes	Yes/IO_SMI#	VCC	
GP13	Yes	Yes	VCC	
GP16-GP17	Yes	Yes	VCC	
GP20-GP22	Yes	No	VCC	
GP23	Yes	Yes	VTR	
GP30-GP37	Yes	No	VCC	
GP40	Yes	No	VCC	
GP41-GP47	No	No	VCC	
GP50	Yes	No	VCC	
GP51-GP57	No	No	VCC	

Note 6-28 Since GP12 can be used to generate an SMI and as the IO_SMI# output, do not enable GP12 to generate an SMI (by setting bit 2 of the SMI Enable Register 1) if the IO_SMI# function is selected on the GP12 pin. Use GP12 to generate an SMI event only if the SMI output is enabled on the Serial IRQ stream.

Note 6-29 GP41-GP47 and GP51-GP57 should not be connected to any VTR powered external circuitry. These pins are not used for wakeup.

6.12 System Management Interrupt (SMI)

The SCH3221 implements a “group” IO_SMI# output pin. The System Management Interrupt is a non-maskable interrupt with the highest priority level used for OS transparent power management. The nSMI group interrupt output consists of the enabled interrupts from Super I/O Device Interrupts (Serial Ports 1, 2, 3 and 4) and many of the GPIOs pins. The GP12/IO_SMI# pin, when selected for the IO_SMI# function, can be programmed to be active high or active low via bit[2] in the GPIO Polarity Register 1 (CR32). The IO_SMI# pin function defaults to active low. The output buffer type of the pin can be programmed to be open-drain or push-pull via GPIO Output Type Register 1 (CR39).

The interrupts are enabled onto the group nSMI output via the SMI Enable Registers 1, 2, and 3. The nSMI output is then enabled onto the IO_SMI# output pin via bit[7] in the SMI Enable Register 2. The SMI output can also be enabled onto the serial IRQ stream (IRQ2) via Bit[6] in the SMI Enable Register 2.

6.12.1 SMI REGISTERS

There are six SMI Registers located in the Runtime Register block. They are SMI_EN1, SMI_EN2, SMI_EN3, SMI_STS1, SMI_STS2, and SMI_STS3. The SMI event bits for the GPIOs events are located in the SMI status and Enable registers 1 and 2. The polarity of the edge used to set the status bit and generate an SMI is controlled by the GPIO Polarity Registers located in the Configuration section. For non-inverted polarity (default) the status bit is set on the low-to-high edge. Status bits for the GPIOs are cleared on a write of ‘1’.

The SMI logic for the GPIO events is implemented such that the output of the status bit for each event is combined with the corresponding enable bit in order to generate an SMI.

The SMI event bits for the super I/O devices are located in the SMI status and enable registers 2 and 3. All of these status bits are cleared at the source; these status bits are not cleared by a write of ‘1’. The SMI logic for these events is implemented such that each event is directly combined with the corresponding enable bit in order to generate an SMI.

See Section 7.0, "Runtime Registers" for the definition of the SMI status and enable registers.

6.13 PME Support

The SCH3221 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events in an ACPI system. A power management event is indicated to the chipset via the assertion of the IO_PME# signal. In the SCH3221, the IO_PME# is asserted by active transitions on the ring indicator inputs nRI1, nRI2, nRI3, and nRI4, Watchdog Timer Event (WDT), and programmable edges on GPIO pins. The nIO_PME pin can be programmed to be active high or active low via bit 5 in the GPIO Polarity Register 2 (CR34). The nIO_PME pin function defaults to active low, open-drain output. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 in the GPIO Output Type Register 2 (CR40). This pin is powered by VTR. See the Configuration section for description on these registers.

PME functionality is controlled by the PME status and enable registers in the runtime registers block, which is located at the address programmed in register 0x30 in the Configuration section. The PME Enable bit, PME_EN, globally controls PME Wake-up events. When PME_EN is inactive, the IO_PME# signal can not be asserted. When PME_EN is asserted, any wake source whose individual PME Wake Enable register bit is asserted can cause IO_PME# to become asserted.

The PME Status register indicates that an enabled wake source has occurred and if the PME_EN bit is set, asserted the IO_PME# signal. The PME Status bit is asserted by active transitions of PME wake sources. PME_STS will become asserted independent of the state of the global PME enable, PME_EN.

The following pertains to the PME status bits for each event:

- The output of the status bit for each event is combined with the corresponding enable bit to set the PME status bit.
- The status bit for any pending events must be cleared in order to clear the PME_STS bit. Status bits are cleared on a write of ‘1’.

For the GPIO events, the polarity of the edge used to set the status bit and generate a PME is controlled by the GPIO Polarity Registers in the Configuration section. For non-inverted polarity (default) the status bit is set on the low-to-high edge. Status bits are cleared on a write of ‘1’.

In the SCH3221 the IO_PME# pin can be programmed to be an open drain, active low, driver. The SCH3221 IO_PME# pin is fully isolated from other external devices that might pull the IO_PME# signal low; i.e., the IO_PME# signal is capable of being driven high externally by another active device or pullup even when the SCH3221 VCC is grounded, providing VTR power is active.

6.13.1 PME REGISTERS

There are eight PME Registers located in the Runtime Register block. They are PME_EN1, PME_EN2, PME_EN3, PME_EN4, PME_STS1, PME_STS2, PME_STS3, and PME_STS4. These registers are located in system I/O space at an offset from Runtime Registers Block, the address programmed at register 0x30 in the Configuration section.

The following registers are for GPIO PME events:

- PME Wake Status 1 (PME_STS1), PME Wake Enable 1 (PME_EN1)
- PME Wake Status 2 (PME_STS2), PME Wake Enable 2 (PME_EN2)
- PME Wake Status 3 (PME_STS3), PME Wake Enable 3 (PME_EN3)
- PME Wake Status 4 (PME_STS4), PME Wake Enable 4 (PME_EN4)

See PME register description in Section 7.0, "Runtime Registers".

7.0 RUNTIME REGISTERS

7.1 Runtime Registers Block Summary

The runtime registers are located at the address programmed in the Runtime Register Block Base Address configuration register located in CR30. The part performs 16-bit address qualification on the Runtime Register Base Address (bits[11:0] are decoded and bits[15:12] must be zero). The runtime register block may be located within the range 0x0100-0x0FFF on 16-byte boundaries. Decodes are disabled if the Runtime Register Base Address is located below 0x100. These registers are powered by VTR.

TABLE 7-1: RUNTIME REGISTER BLOCK SUMMARY

Register Offset (HEX)	Type	Hard Reset (Note 7-2)	VCC POR	VTR POR	Register
00	R/W	-	-	0x00	PME_STS
01	R/W	-	-	0x00	PME_EN
02	R/W	-	-	0x00	PME_STS1
03	R/W	-	-	0x00	PME_STS2
04	R/W	-	-	0x00	PME_STS3
05	R/W	-	-	0x00	PME_EN1
06	R/W	-	-	0x00	PME_EN2
07	R/W	-	-	0x00	PME_EN3
08	R/W	-	-	0x00	SMI_STS1
09	R/W	-	-	0x01	SMI_STS2
0A	R/W	-	-	0x00	SMI_EN1
0B	R/W	-	-	0x00	SMI_EN2
0C	R/W	-	-	0x00	GP1
0D	R/W	-	-	0x00	GP2
0E	R/W	-	-	0x00	GP3
0F	R/W	-	-	0x00	GP4
10	R/W	-	-	0x00	GP5
11	R/W	0x00	0x00	0x00	WDT_TIME_OUT
12	R/W	0x00	0x00	0x00	WDT_VAL
13	R/W	0x00	0x00	0x00	WDT_CFG
14	R/W Note 7-1	0x00	0x00	0x00	WDT_CTRL
15	R/W	-	-	0x00	LED1
16	R/W	-	-	0x00	LED2
17	R	-	-	0x00	Reserved
18	R/W	-	-	0x00	SMI_STS3
19	R/W	-	-	0x00	SMI_EN3
1A	R/W	-	-	0x00	PME_STS4
1B	R/W	-	-	0x00	PME_EN4

Note: Reserved bits return 0 on read.

Note 7-1 This register contains some bits that are read or write only.

Note 7-2 Hard Reset = PCI_RESET#

7.2 Runtime Registers Block Description

TABLE 7-2: RUNTIME REGISTERS BLOCK DESCRIPTION

Name/Default	Register Offset	Description
PME_STS Default = 0x00 on VTR POR	00 (R/W)	Bit[0] PME_Status = 0 (default) = 1 Set when SCH3221 would normally assert the IO_PME# signal, independent of the state of the PME_En bit. Bit[7:1] Reserved PME_Status is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to PME_Status will clear it and cause the SCH3221 to stop asserting IO_PME#, in enabled. Writing a “0” to PME_Status has no effect.
PME_EN Default = 0x00 on VTR POR	01 (R/W)	Bit[0] PME_En = 0 IO_PME# signal assertion is disabled (default) = 1 Enables SCH3221 to assert IO_PME# signal Bit[7:1] Reserved PME_En is not affected by Vcc POR, SOFT RESET or HARD RESET
PME_STS1 Default = 0x00 on VTR POR	02 (R/W)	PME Wake Status Register 1 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] Reserved Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] Reserved Bit[5] Reserved Bit[6] GP16 Bit[7] GP17 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect. **Note:** Status bits are set by an event on the pin regardless of the Alternate Function selected.

TABLE 7-2: RUNTIME REGISTERS BLOCK DESCRIPTION (CONTINUED)

Name/Default	Register Offset	Description
PME_STS2 Default = 0x00 on VTR POR	03 (R/W)	PME Wake Status Register 2 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] nRI1 Bit[1] nRI2/GP50 Bit[2] GP20 Bit[3] GP21 Bit[4] GP22 Bit[5] GP23 Bit[6] Reserved Bit[7] WDT Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect. **Note:** Status bits are set by an event on the pin regardless of the Alternate Function selected.
PME_STS3 Default = 0x00 on VTR POR	04 (R/W)	PME Wake Status Register 3 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] GP30/nRI3 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] GP35 Bit[6] GP36 Bit[7] GP37 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect. **Note:** Status bits are set by an event on the pin regardless of the Alternate Function selected.

TABLE 7-2: RUNTIME REGISTERS BLOCK DESCRIPTION (CONTINUED)

Name/Default	Register Offset	Description
PME_EN1 Default = 0x00 on VTR POR	05 (R/W)	PME Wake Enable Register 1 This register is used to enable individual SCH3221 PME wake sources onto the IO_PME# wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the IO_PME# signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the IO_PME# signal. Bit[0] Reserved Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] Reserved Bit[5] Reserved Bit[6] GP16 Bit[7] GP17 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.
PME_EN2 Default = 0x00 on VTR POR	06 (R/W)	PME Wake Enable Register 2 This register is used to enable individual SCH3221 PME wake sources onto the IO_PME# wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the IO_PME# signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the IO_PME# signal. Bit[0] nRI1 Bit[1] nRI2/GP50 Bit[2] GP20 Bit[3] GP21 Bit[4] GP22 Bit[5] GP23 Bit[6] Reserved Bit[7] WDT

TABLE 7-2: RUNTIME REGISTERS BLOCK DESCRIPTION (CONTINUED)

Name/Default	Register Offset	Description
PME_EN3 Default = 0x00 on VTR POR	07 (R/W)	PME Wake Enable Register 3 This register is used to enable individual SCH3221 PME wake sources onto the IO_PME# wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the IO_PME# signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the IO_PME# signal. Bit[0] GP30/nRI3 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] GP35 Bit[6] GP36 Bit[7] GP37 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.
SMI_STS1 Default = 0x00 on VTR POR	08 (R/W)	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of ‘1’. Bit[0] Reserved Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] Reserved Bit[5] Reserved Bit[6] GP16 Bit[7] GP17
SMI_STS2 Default = 0x01 on VTR POR Bit 0 is set to ‘1’ on VCC POR, VTR POR and HARD RESET	09 (R/W)	SMI Status Register 2 This register is used to read the status of the SMI inputs. The bits [1] and [2] must be cleared at their source. Bit[4] is cleared on a write of ‘1’. Bit[0] defaults to 1 and cannot be cleared. Bit[0] Reserved, default state =1 Bit[1] U2INT Bit[2] U1INT Bit[3] Reserved Bit[4] GP23 Bit[7:5] Reserved

TABLE 7-2: RUNTIME REGISTERS BLOCK DESCRIPTION (CONTINUED)

Name/Default	Register Offset	Description
SMI_EN1 Default = 0x00 on VTR POR	0A (R/W)	SMI Enable Register 1 This register is used to enable the different interrupt sources onto the internal group nSMI signal. 1=Enable 0=Disable Bit[0] Reserved Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] Reserved Bit[5] Reserved Bit[6] GP16 Bit[7] GP17
SMI_EN2 Default = 0x00 on VTR POR	0B (R/W)	SMI Enable Register 2 This register is used to enable the different interrupt sources onto the internal group nSMI signal, and the internal group nSMI signal onto the IO_SMI# GPI/O pin or the serial IRQ stream on IRQ2. 1=Enable 0=Disable Bit[0] Reserved. Default = 0, do not change. Bit[1] EN_U2INT Bit[2] EN_U1INT Bit[3] Reserved Bit[4] GP23 Bit[5] Reserved Bit[6] EN_SMI_S (Enable group nSMI signal onto serial IRQ2) Bit[7] EN_SMI (Enable group nSMI signal onto IO_SMI# pin)
GP1 Default = 0x00 on VTR POR	0C R/W	General Purpose I/O Data Register 1 Bit[0]Reserved Bit[1]GP11 Bit[2]GP12 Bit[3]GP13 Bit[4]Reserved Bit[5]Reserved Bit[6]GP16 Bit[7]GP17
GP2 Default = 0x00 on VTR POR	0D R/W	General Purpose I/O Data Register 2 Bit[0]GP20 Bit[1]GP21 Bit[2]GP22 Bit[3]GP23 Bit[7:4]Reserved
GP3 Default = 0x00 on VTR POR	0E R/W	General Purpose I/O Data Register 3 Bit[0]GP30 Bit[1]GP31 Bit[2]GP32 Bit[3]GP33 Bit[4]GP34 Bit[5]GP35 Bit[6]GP36 Bit[7]GP37

TABLE 7-2: RUNTIME REGISTERS BLOCK DESCRIPTION (CONTINUED)

Name/Default	Register Offset	Description
GP4 Default = 0x00 on VTR POR	0F R/W	General Purpose I/O Data Register 4 Bit[0]GP40 Bit[1]GP41 Bit[2]GP42 Bit[3]GP43 Bit[4]GP44 Bit[5]GP45 Bit[6]GP46 Bit[7]GP47
GP5 Default = 0x00 on VTR POR	10 R/W	General Purpose I/O Data Register 5 Bit[0]GP50 Bit[1]GP51 Bit[2]GP52 Bit[3]GP53 Bit[4]GP54 Bit[5]GP55 Bit[6]GP56 Bit[7]GP57
WDT_TIME_OUT Default = 0x00 on VCC POR, VTR POR, and Hard Reset	11 (R/W)	Watchdog Timeout Bits[6:0] Reserved Bit[7] WDT Time-out Value Units Select = 0 Minutes (default) = 1 Seconds
WDT_VAL Default = 0x00 on VCC POR, VTR POR, and Hard Reset	12 (R/W)	Watchdog Timer Time-out Value Binary coded, units = minutes (default) or seconds, selectable via Bit[7] of WDT_TIME_OUT register (0x52). 0x00 Time out disabled 0x01 Time-out = 1 minute (second) ..... 0xFF Time-out = 255 minutes (seconds)
WDT_CFG Default = 0x00 on VCC POR, VTR POR, and Hard Reset	13 (R/W)	Watchdog timer Configuration Bit[3:0] Reserved Bits[7:4] WDT Interrupt Mapping 1111 = IRQ15 ..... 0011 = IRQ3 0010 = Invalid 0001 = IRQ1 0000 = Disable

TABLE 7-2: RUNTIME REGISTERS BLOCK DESCRIPTION (CONTINUED)

Name/Default	Register Offset	Description
WDT_CTRL Default = 0x00 on VCC POR, VTR POR, and Hard Reset	14 (R/W) Bit[2] is Write-Only	Watchdog timer Control Bit[0] Watchdog Status Bit, R/W (Note) =1 WD timeout occurred =0 WD timer counting Bit[1] Reserved Bit[2] Force Timeout, W =1 Forces WD timeout event; this bit is self-clearing Bit[3] Reserved Bit[7:4] Reserved. Set to 0 **Note:** If WDT is disabled (i.e., WDT_VAL register is 00h) bit[0] is forced to '0'
LED1 Default = 0x00 on VTR POR	15 (R/W)	Bit[1:0] LED1 Control 00=off 01=Blink at 1Hz rate with a 50% duty cycle (0.5 sec on, 0.5 sec off) 10=Blink at ½ HZ rate with a 25% duty cycle (0.5 sec on, 1.5 sec off) 11=on Bits[7:2] Reserved
LED2 Default = 0x00 on VTR POR	16 (R/W)	Bit[1:0] LED2 Control 00=off 01=Blink at 1Hz rate with a 50% duty cycle (0.5 sec on, 0.5 sec off) 10=Blink at ½ Hz rate with a 25% duty cycle (0.5 sec on, 1.5 sec off) 11=on Bits[7:2] Reserved
Reserved	17	Reads return 0.
SMI_STS3 Default = 0x00 on VTR POR	18 (R/W)	SMI Status Register 3 This register is used to read the status of the SMI inputs. Bit[0] is cleared on a write of '1'. Bit[0] WDT Bit[1] U3INT Bit[2] U4INT Bit[7:3] Reserved
SMI_EN3 Default = 0x00 on VTR POR	19 (R/W)	SMI Enable Register 3 This register is used to enable the different interrupt sources onto the internal group nSMI signal. 1=Enable 0=Disable Bit[0] EN_WDT Bit[1] EN_U3INT Bit[2] EN_U4INT Bit[7:3] Reserved

TABLE 7-2: RUNTIME REGISTERS BLOCK DESCRIPTION (CONTINUED)

Name/Default	Register Offset	Description
PME_STS4 Default = 0x00 on VTR POR	1A (R/W)	PME Wake Status Register 4 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] nRI3/GP30 Bit[1] nRI4/GP40 Bit[2] Reserved Bit[3] Reserved Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved Writing a “1” to Bit[1:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect. **Note:** Status bits are set by an event on the pin regardless of the Alternate Function selected.
PME_EN4 Default = 0x00 on VTR POR	1B (R/W)	PME Wake Enable Register 4 This register is used to enable individual SCH3221 PME wake sources onto the IO_PME# wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the IO_PME# signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the IO_PME# signal. Bit[0] nRI3/GP30 Bit[1] nRI4/GP40 Bit[2] Reserved Bit[3] Reserved Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved

Note: Reserved bits return 0 on read except where noted.

8.0 CONFIGURATION

The configuration of the SCH3221 is programmed through hardware selectable Configuration Access Ports that appear when the chip is placed into the configuration state. The SCH3221 logical device blocks, if enabled, will operate normally in the configuration state.

8.1 Configuration Access Ports

The Configuration Access Ports are the CONFIG PORT, the INDEX PORT, and the DATA PORT (Table 8-1, "Configuration Access Ports"). The base address of these registers is controlled by the nRTS1/SYSOPT pin and by the Configuration Port Base Address registers CR12 and CR13. To determine the configuration base address at power-up, the state of the nRTS1/SYSOPT pin is latched by the trailing edge of a hardware reset (deasserting edge of PCI_RESET#). If the latched state is a 0, the base address of the Configuration Access Ports is located at address 0x02E; if the latched state is a 1, the base address is located at address 0x04E. The base address is relocatable via CR12 and CR13.

TABLE 8-1: CONFIGURATION ACCESS PORTS

Port Name	SYSOPT = 0	SYSOPT = 1	Type
CONFIG PORT	0x02E	0x04E	WRITE
INDEX PORT	0x02E	0x04E	READ/WRITE (Note 8-1, Note 8-2)
DATA PORT	INDEX PORT + 1		READ/WRITE (Note 8-1)

Note 8-1 The INDEX and DATA ports are active only when the SCH3221 is in the configuration state.

Note 8-2 The INDEX PORT is only readable in the configuration state.

8.2 Configuration State

The configuration registers are used to select programmable chip options. The SCH3221 operates in two possible states: the run state and the configuration state. After power up by default the chip is in the run state. To program the configuration registers, the configuration state must be explicitly enabled. Programming the configuration registers typically follows this sequence:

1. Enter the Configuration State,
2. Program the Configuration Register(s),
3. Exit the Configuration State.

8.2.1 ENTERING THE CONFIGURATION STATE

To enter the configuration state write the Configuration Access Key to the CONFIG PORT. The Configuration Access Key is one byte of 55H data. The SCH3221 will automatically activate the Configuration Access Ports following this procedure.

8.2.2 CONFIGURATION REGISTER PROGRAMMING

The SCH3221 contains configuration registers CR00-CR54. After the SCH3221 enters the configuration state, configuration registers can be programmed by first writing the register index number (00 - 54H) to the Configuration Select Register (CSR) through the INDEX PORT and then writing or reading the configuration register contents through the DATA PORT. Configuration register access remains enabled until the configuration state is explicitly exited.

8.2.3 EXITING THE CONFIGURATION STATE

To exit the configuration state, write one byte of AAH data to the CONFIG PORT. The SCH3221 will automatically deactivate the Configuration Access Ports following this procedure, at which point configuration register access cannot occur until the configuration state is explicitly re-enabled.

8.2.3.1 Programming Example

The following is a configuration register programming example written in Intel 8086 assembly language.

```
;----------------------------.
; ENTER CONFIGURATION STATE  |
;----------------------------'
MOV   DX,02EH     ;SYSOPT = 0
MOV   AX,055H
OUT   DX,AL
;----------------------------.
; CONFIGURE REGISTERS CRx    |
;----------------------------'
MOV   DX,02EH
MOV   AL,24H
OUT   DX,AL       ;Point to CR24
MOV   DX,02FH
MOV   AL,0FEH     ; UART1 Base = COM1
OUT   DX,AL       ;Update CR24
;
MOV   DX,02EH
MOV   AL,25H
OUT   DX,AL       ;Point to CR25
MOV   DX,02FH
MOV   AL,0BEH     ; UART2 Base = COM2
OUT   DX,AL       ;Update CR25
;
; Repeat for other CRx registers
;
;----------------------------.
; EXIT CONFIGURATION STATE    |
;----------------------------'
MOV   DX,02EH
MOV   AX,AAH
OUT   DX,AL
```

8.2.3.2 Configuration Select Register (CSR)

The Configuration Select Register can only be accessed when the SCH3221 is in the configuration state. The CSR is located at the INDEX PORT address and must be initialized with configuration register index before the register can be accessed using the DATA PORT.

8.3 Configuration Registers Summary

The configuration registers are set to their default values at power up and are RESET as indicated in Table 8-2. The register descriptions follow.

CAUTION: This device contains circuits which must not be used because their pins are not brought out of the package, and are pulled to known states internally. Any features, and especially SIO blocks that are not listed in this document, must not be activated or accessed. Doing so may cause unpredictable behavior and/or excessive currents, and therefore may damage the device and/or the system.

TABLE 8-2: CONFIGURATION REGISTERS SUMMARY

Register Index	Type	Hard Reset (Note 8-3)	VCC POR	VTR POR	Register
CR00	R/W	Bit[3] = 0	0x20	-	Valid Config Cycle
CR01	R/W	bit[7]=1 Bit[2]=0	0x98	-	CR Lock
CR02	R/W	0x00	0x00	-	UART Power
CR03	R/W	-	0x70	-	Reserved
CR04	R/W	-	0x00	-	UART Miscellaneous
CR05	R/W	-	0x00	-	Reserved
CR06	R/W	-	0xFF	-	Reserved
CR07	R/W	bit[7:2]=0	0x00	-	Auto Power Mgt
CR08	R	-	0x00	-	Reserved
CR09	R/W	-	0x00	-	Test 4
CR0A	R/W	bit[7:6]=0	0x00	-	IR MUX
CR0B	R/W	-	0x00	-	Reserved
CR0C	R/W	0x02	0x02	-	UART Mode
CR0D	R	-	0x5B	-	Device ID
CR0E	R	-	Revision	-	Revision ID
CR0F	R/W	-	0x00	-	Test 1
CR10	R/W	-	0x00	-	Test 2
CR11	R/W	-	0x00	-	Test 3
CR12	R/W	SYSOPT=0:0x2E SYSOPT=1:0x4E		-	Configuration Base Address 0
CR13	R/W	SYSOPT=0:0x00 SYSOPT=1:0x00		-	Configuration Base Address 1
CR14	R	-	-	-	Reserved
CR15	R	-	-	-	UART1 FCR Shadow
CR16	R	-	-	-	UART2 FCR Shadow
CR17	R/W	0x03	0x03	-	Reserved
CR18	R/W	bit[7:6]=0	0x00	-	UART 3,4 Miscellaneous
CR19	R	-	-	-	UART3 FCR Shadow
CR1A	R	-	-	-	UART4 FCR Shadow
CR1B	R/W	-	0x00	-	UART3 Base Address
CR1C	R/W	-	0x00	-	UART4 Base Address
CR1D	R/W	-	0x00	-	UART 3,4 IRQ Select
CR1E	R/W	-	-	0x00	Clock Register
CR1F	R/W	-	0x00	-	Reserved

TABLE 8-2: CONFIGURATION REGISTERS SUMMARY (CONTINUED)

Register Index	Type	Hard Reset (Note 8-3)	VCC POR	VTR POR	Register
CR20	R/W	-	0x3C	-	Reserved
CR21	R/W	-	0x00	-	Reserved
CR22	R/W	0x00	0x00	-	Reserved
CR23	R/W	-	0x00	-	Reserved
CR24	R/W	-	0x00	-	UART1 Base Address
CR25	R/W	-	0x00	-	UART2 Base Address
CR26	R/W	-	0xFF	-	Reserved
CR27	R/W	-	0x00	-	Reserved
CR28	R/W	-	0x00	-	UART IRQ Select
CR29	R/W	-	0x80	-	IRQIN1/HPMODE/SIRQ_CLKRUN_En
CR2A	R/W	-	0x00	-	IRQIN2/IRQIN3
CR2B	R/W	-	0x00	-	SCE (FIR) Base Address
CR2C	R/W	-	0x0F	-	SCE (FIR) DMA Select
CR2D	R/W	-	0x03	-	IR Half Duplex Timeout
CR2E	R/W	-	0x00	-	Software Select A
CR2F	R/W	-	0x00	-	Software Select B
CR30	R/W	-	0x00	-	Runtime Register Block Address
CR31	R/W	-	-	0x00	GPIO Direction Register 1
CR32	R/W	-	-	0x00	GPIO Polarity Register 1
CR33	R/W	-	-	0x00	GPIO Direction Register 2
CR34	R/W	-	-	0x00	GPIO Polarity Register 2
CR35	R/W	-	-	0x00	GPIO Direction Register 3
CR36	R/W	-	-	0x00	GPIO Polarity Register 3
CR37	R/W	-	-	0x00	GPIO Direction Register 4
CR38	R/W	-	-	0x00	GPIO Polarity Register 4
CR39	R/W	-	-	0x00	GPIO Output Type Register 1
CR3A	R/W	-	0x00	-	Test 5
CR3B	R	-	0x00	-	Reserved
CR3C	R	-	0x00	-	Reserved
CR3D	R	-	0x00	-	Reserved
CR3E	R	-	0x00	-	Reserved
CR3F	R	-	0x00	-	Reserved
CR40	R/W	-	-	0x80	GPIO/MISC Output Type Register 2
CR41	R/W	-	-	0x00	GPIO Output Type Register 5
CR42	R/W	-	-	0x00	GPIO Direction Register 5
CR43	R/W	-	-	0x00	GPIO Polarity Register 5
CR44	R/W	-	-	0x00	GPIO Alternate Function Select Register 1
CR45	R/W	bit[7:4]= 0101	bit[7:4]= 0101	0x50	GPIO Alternate Function Select Register 2

TABLE 8-2: CONFIGURATION REGISTERS SUMMARY (CONTINUED)

Register Index	Type	Hard Reset (Note 8-3)	VCC POR	VTR POR	Register
CR46	R/W	-	-	0x00	GPIO Alternate Function Select Register 3
CR47	R/W	-	0x00	-	Reserved
CR48	R/W	-	-	0x00	GPIO Alternate Function Select Register 5
CR49	R/W	-	-	0x00	GPIO Alternate Function Select Register 6
CR4A	R/W	-	-	0x00	GPIO Alternate Function Select Register 7
CR4B	R/W	-	-	0x00	GPIO Alternate Function Select Register 8
CR4C	R/W	-	-	0x00	GPIO Alternate Function Select Register 9
CR4D	R/W	-	-	0x00	GPIO Alternate Function Select Register 10
CR4E	R/W	0x00	0x00	-	Reserved
CR4F	R/W	0x01	0x01	-	Reserved
CR50	R/W	0x00	0x00	-	Reserved
CR51	R/W	0x01	0x01	-	Reserved
CR52	R/W	0x00	0x00	-	Reserved
CR53	R/W	0x8C	0x8C	-	Reserved
CR54	R/W	0XX00000b	0XX00000b	-	Reserved

Note: Reserved registers are read-only, reads return 0.

Note 8-3 Hard Reset = PCI_RESET#

8.4 Configuration Registers Description

8.4.1 CR00

CR00 can only be accessed in the configuration state and after the CSR has been initialized to 00H.

TABLE 8-3: CR00

VALID CONFIGURATION CYCLE		
TYPE: R/W		**DEFAULT:** 0x20 on VCC POR Bit[3] = 0 on a Hard Reset
Bit No.	**Bit Name**	**Description**
0-2	Reserved	Read Only. A read returns 0
3	Reserved	Reserved. Do not alter this bit from its default.
4,5,6	Reserved	Read only. A read returns bit 5 as a 1 and bits 4 and 6 as a 0.
7	Valid	A high level on this software controlled bit can be used to indicate that a valid configuration cycle has occurred. The control software must take care to set this bit at the appropriate times. Set to zero after power up. This bit has no effect on any other hardware in the chip.

8.4.2 CR01

CR01 can only be accessed in the configuration state and after the CSR has been initialized to 01H.

TABLE 8-4: CR01

CR LOCK		
TYPE: R/W		**DEFAULT:** 0x98 on VCC POR; Bit[7] = 1 and Bit[2]=0 on HARD RESET
Bit No.	**Bit Name**	**Description**
0,1	Reserved	Read Only. A read returns “0”.
2	Reserved	Reserved. Do not alter this bit from its default.
3	Reserved	Reserved. Do not alter this bit from its default.
4	Reserved	Read Only. A read returns “1”.
5,6	Reserved	Read Only. A read returns “0”.
7	Lock CRx	A high level on this bit enables the reading and writing of CR00 –CR39 (Default). A low level on this bit disables the reading and writing of CR00 – CR39. **Note:** Once the Lock CRx bit is set to “0”, this bit can only be set to “1” by a hard reset or power-up reset.

8.4.3 CR02

CR02 can only be accessed in the configuration state and after the CSR has been initialized to 02H.

TABLE 8-5: CR02

UART Power		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR and Hard Reset
Bit No.	**Bit Name**	**Description**
0	Reserved	Read Only. A read returns “0”.
1	UART3 Power (Note 8-4, Note 8-5)	A high level on this bit, allows normal operation of the Primary Serial Port. A low level on this bit places the Primary Serial Port into Power Down Mode (Default).
2	UART4 Power (Note 8-4, Note 8-5)	A high level on this bit, allows normal operation of the Primary Serial Port. A low level on this bit places the Primary Serial Port into Power Down Mode (Default).
3	UART1 Power (Note 8-4)	A high level on this bit, allows normal operation of the Primary Serial Port. A low level on this bit places the Primary Serial Port into Power Down Mode (Default).
4-6	Reserved	Read Only. A read returns “0”.
7	UART2 Power (Note 8-4, Note 8-5)	A high level on this bit, allows normal operation of the Secondary Serial Port, including the SCE/FIR block. A low level on this bit places the Secondary Serial Port including the SCE/FIR block into Power Down Mode (Default).

Note 8-4 Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device’s base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

Note 8-5 The UART pins must be configured for their alternate function prior to enabling the UART power bits. In addition, the IRCC should be configured for the appropriate mode of operation before the UART2 Power bit is set. This is to ensure the state of the transmit and receive pins are in their inactive state for the external device attached and for the internal block that has been enabled, respectively. The registers used to configure the IRCC block are IR Output Mux bits located in the IR MUX located at CR0A and the UART Mode register located at CR0C. These functions may also be configured directly in the SCE registers located in the IR block. A description of these register may be found in the Infrared Communication Controller (IRCC) specification.

8.4.4 CR03

CR03 is reserved. The default value of this register after power up is 70H. Do not change this register from its default value.

8.4.5 CR04

CR04 can only be accessed in the configuration state and after the CSR has been initialized to 04H.

TABLE 8-6: CR04

UART MISCELLANEOUS		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
1,0	Reserved	Reserved. Do not alter this field from its default.
2,3	Reserved	Reserved. Do not alter this field from its default.
4	MIDI 1 (Note 8-6)	Serial Clock Select Port 1: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.
5	MIDI 2 ((Note 8-6)	Serial Clock Select Port 2: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.
6	Reserved	Reserved. Do not alter this bit from its default.
7	Reserved	Reserved - Read as 0.

Note 8-6 MIDI Support: The Musical Instrumental Digital Interface (MIDI) operates at 31.25Kbaud (+/-1%).

8.4.6 CR05

CR05 is reserved. The default value of this register after power up is 00H. Do not change this register from its default value.

8.4.7 CR06

CR06 is reserved. The default value of this register after power up is FFH. Do not change this register from its default value.

8.4.8 CR07

CR07 can only be accessed in the configuration state and after the CSR has been initialized to 07H.

TABLE 8-7: CR07

AUTO POWER MANAGEMENT		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR; Bits[7:2] = 000000b on HARD RESET
Bit No.	**Bit Name**	**Description**
0,1	Reserved	Reserved. Do not alter this field from its default.
2	UART 3 Enable	This bit controls the AUTOPOWER DOWN feature of the UART3. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by VCC POR or a hardware reset.
3	UART 4 Enable	This bit controls the AUTOPOWER DOWN feature of the UART4. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by VCC POR or a hardware reset.
4	Reserved	Reserved. Do not alter this bit from its default.
5	UART 2 Enable	This bit controls the AUTOPOWER DOWN feature of the UART2. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by VCC POR or a hardware reset.
6	UART 1 Enable	This bit controls the AUTOPOWER DOWN feature of the UART1. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by VCC POR or a hardware reset.
7	Reserved	Reserved. Do not alter this bit from its default.

8.4.9 CR08

Register CR08 is reserved. The default value of this register after power up is 00H.

8.4.10 CR09

CR09 can only be accessed in the configuration state and after the CSR has been initialized to 09H. CR09 is a test control register and all bits must be treated as Reserved.

Note: All test modes are reserved for Microchip use. Activating test mode registers may produce undesired results.

TABLE 8-8: CR09

TEST 4		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0	Test 24	RESERVED FOR MICROCHIP USE
1	Test 25	
2	Test 26	
3	Test 27	
4	Test 28	
5	Test 29	
6	Test 30	
7	Test 31	

8.4.11 CR0A

CR0A can only be accessed in the configuration state and after the CSR has been initialized to 0AH. Bits [7:6] are the IR OUTPUT MUX bits and are reset to the default state by a POR and a hardware reset.

TABLE 8-9: CR0A

IR MUX				
TYPE: R/W				**DEFAULT:** 0x00 on VCC POR; Bits[7:6] = 00 on HARD RESET
Bit No.	**Bit Name**	**Description**		**Bit No.**
0-5	Reserved	Reserved. Do not alter this field from its default.		
6,7	IR Output Mux	These bits are used to select IR Output Mux Mode.		
		BIT7	**BIT6**	**MUX MODE**
		0	0	Active device to COM port (Default). That is, depending on the mode of Serial Port 2, use UART2 pins for COM signals or use RXD2 and TXD2 for IR. When Serial Port 2 is inactive (UART2 Power bit = 0), then TXD2 signal is tristate. The IRTX2 signal is low.
		0	1	Active device to IR port. That is, use IRRX2, IRTX2. When Serial Port 2 is inactive (UART2 Power bit = 0), then IRTX2 signal is low. The TXD2 signal is low.
		1	0	Reserved.
		1	1	Outputs Inactive: TXD2/IRTX and IRTX2 are High-Z, regardless of mode of UART2 and state of UART2 powerdown bit.

8.4.12 CR0B

CR0B is reserved. The default value of this register after power up is 00H.

8.4.13 CR0C

CR0C can only be accessed in the configuration state and after the CSR has been initialized to 0CH. CR0C controls the operating mode of the UART. This register is reset to the default state by a POR or a hardware reset.

TABLE 8-10: CR0C

UART MODE		
TYPE: R/W		**DEFAULT:** 0x02 on VCC POR and HARD RESET
Bit No.	**Bit Name**	**Description**
0	UART 2 RCV Polarity	0 = RX input active high (default). 1 = RX input active low.
1	UART 2 XMIT Polarity	0 = TX output active high. 1 = TX output active low (default).
2	UART 2 Duplex	This bit is used to define the FULL/HALF DUPLEX operation of UART 2. 1 = Half duplex 0 = Full duplex (default)
3, 4, 5	UART 2 MODE	UART 2 Mode (Note 8-7) 5 4 3 0 0 0 Standard COM Functionality (default) 0 0 1 IrDA (HPSIR) 0 1 0 Amplitude Shift Keyed IR 0 1 1 Reserved (Note 8-8) 1 x x Reserved (Note 8-8)
6	UART 1 Speed	This bit enables the high speed mode of UART 1. 1 = High speed enabled 0 = Standard (default)
7	UART 2 Speed	This bit enables the high speed mode of UART 2. 1 = High speed enabled 0 = Standard (default)

Note 8-7 The UART 2 Mode may be selected by writing bits[5:3] shown or by programming the block control bits located in Register Block One - SCE Configuration Register A of the SCE (FIR) block. See the IrCC Specification dated 5/10/96 for a detailed description of this register and the modes supported.

Note 8-8 Writing these reserved bit combinations will place the IR block into an alternate mode, which is beyond the scope of this specification. Users that require these advanced options should refer to the IrCC Specification dated 5/10/96.

8.4.14 CR0D

CR0D can only be accessed in the configuration state and after the CSR has been initialized to 0DH. This register is read only. CR0D contains the SCH3221 Device ID. The default value of this register after power up is 5BH on VCC POR.

8.4.15 CR0E

CR0E can only be accessed in the configuration state and after the CSR has been initialized to 0EH. This register is read only. CR0E contains the current SCH3221 Chip Revision Level starting at 00H.

8.4.16 CR0F

CR0F can only be accessed in the configuration state and after the CSR has been initialized to 0FH. CR0F is a test control register and all bits must be treated as Reserved.

Note:	All test modes are reserved for Microchip use. Activating test mode registers may produce undesired results.

TABLE 8-11: CR0F

TEST 1		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0	Test 0	RESERVED FOR MICROCHIP USE
1	Test 1	
2	Test 2	
3	Test 3	
4	Test 4	
5	Test 5	
6	Test 6	
7	Test 7	

8.4.17 CR10

CR10 can only be accessed in the configuration state and after the CSR has been initialized to 10H. CR10 is a test control register and all bits must be treated as Reserved.

Note:	All test modes are reserved for Microchip use. Activating test mode registers may produce undesired results.

TABLE 8-12: CR10

TEST 2		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0	Test 8	RESERVED FOR MICROCHIP USE
1	Test 9	
2	Test 10	
3	Test 11	
4	Test 12	
5	Test 13	
6	Test 14	
7	Test 15	

8.4.18 CR11

CR11 can only be accessed in the configuration state and after the CSR has been initialized to 11H. CR11 is a test control register and all bits must be treated as Reserved.

Note:	All test modes are reserved for Microchip use. Activating test mode registers may produce undesired results.

TABLE 8-13: CR11

TEST 3		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0	Test 16	RESERVED FOR MICROCHIP USE
1	Test 17	
2	Test 18	
3	Test 19	
4	Test 20	
5	Test 21	
6	Test 22	
7	Test 23	

8.4.19 CR12 - CR13

CR12 and CR13 are the SCH3221 Configuration Ports base address registers (and Table 8-15, "CR13"). These registers are used to relocate the Configuration Ports base address beyond the power-up defaults determined by the SYSOPT pin programming.

CR12 contains the Configuration Ports base address bits A[7:0]. CR13 contains the Configuration Ports base address bits A[10:8]. The address bits A[15:11] must be ‘00000’ to access the configuration port.

The Configuration Ports base address is relocatable on even-byte boundaries; i.e., A0 = ‘0’.

At power-up the Configuration Ports base address is determined by the SYSOPT pin programming. To relocate the Configuration Ports base address after power-up, first write the lower address bits of the new base address to CR12 and then write the upper address bits to CR13.

Note:	Writing CR13 changes the Configuration Ports base address.

TABLE 8-14: CR12

CONFIGURATION PORTS BASE ADDRESS BYTE 0 (Note 8-9)		
TYPE: R/W		**DEFAULT:** 0x2E (SYSOPT=0) 0x4E (SYSOPT=1) on VCC POR and HARD RESET
Bit No.	**Bit Name**	**Description**
0	Reserved	Read Only. A read returns 0.
1	A1	Configuration Ports Base Address Byte 0 for decoder.
2	A2	
3	A3	
4	A4	
5	A5	
6	A6	
7	A7	

Note 8-9 The Configuration Ports Base Address is relocatable on even-byte boundaries; i.e., A0 = “0”.

TABLE 8-15: CR13

CONFIGURATION PORTS BASE ADDRESS BYTE 1 (Note 8-10)		
TYPE: R/W		**DEFAULT:** 0x00 (SYSOPT=0) 0x00 (SYSOPT=1) on VCC POR and HARD RESET
Bit No.	**Bit Name**	**Description**
0	A8	Configuration Ports Base Address Byte 1 for decoder.
1	A9	
2	A10	
3-7	Reserved	Read Only. A read returns 0.

Note 8-10 Writing CR13 changes the Configuration Ports base address.

8.4.20 CR14

CR14 is reserved. The default value of this register after power up is undefined.

8.4.21 CR15

CR15 can only be accessed in the configuration state and after the CSR has been initialized to 15H. CR15 shadows the bits in the write-only UART1 run-time FCR register.

TABLE 8-16: CR15

UART1 FCR SHADOW REGISTER				
TYPE: R (Note 8-11)		**DEFAULT:** N/A		
Bit No.	**Bit Name**	**Description**		
0	FIFO Enable	Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs		
1	RCVR FIFO Reset	Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. This bit is self clearing.		
2	XMIT FIFO Reset	Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. This bit is self-clearing.		
3	DMA Mode Select	Writing to this bit has no effect on the operation of the UART.		
4,5	Reserved	Read Only. A read returns 0.		
6,7	RCVR Trigger	These bits are used to set the trigger level for the RCVR FIFO interrupt.		
		BIT7	**BIT6**	**RCVR FIFO Trigger Level (BYTES)**
		0	0	1
		0	1	4
		1	0	8
		1	1	14

Note 8-11 This is a read only register. Software may set these register bits by writing the UART1 runtime FCR register located at an offset of +2 from the UART1 Base I/O Address. See Table 8-60, "I/O Base Address Configuration Register Description".

8.4.22 CR16

CR16 can only be accessed in the configuration state and after the CSR has been initialized to 16H. CR16 shadows the bits in the write-only UART2 run-time FCR register. See Section 8.4.21, "CR15" for register description.

Note:	This is a read only register. Software may set these register bits by writing the UART2 runtime FCR register located at an offset of +2 from the UART2 Base I/O Address. See Table 8-60, "I/O Base Address Configuration Register Description".

8.4.23 CR17

CR17 is reserved. The default value of this register after power up is 03H.

8.4.24 CR18

CR18 can only be accessed in the configuration state and after the CSR has been initialized to 18H.

TABLE 8-17: CR18

UART 3,4 MISCELLANEOUS		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR, bits[6:7] are reset on Hard Reset
Bit No.	**Bit Name**	**Description**
0-3	Reserved	Reserved - Read as 0.
4	MIDI 3 (Note 8-12)	Serial Clock Select Port 3: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.
5	MIDI 4 (Note 8-12)	Serial Clock Select Port 4: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.
6	UART 3 Speed	This bit enables the high speed mode of UART 3. 1 = High speed enabled 0 = Standard (default)
7	UART 4 Speed	This bit enables the high speed mode of UART 4. 1 = High speed enabled 0 = Standard (default)

Note 8-12 MIDI Support: The Musical Instrumental Digital Interface (MIDI) operates at 31.25Kbaud (+/-1%).

8.4.25 CR19

CR19 can only be accessed in the configuration state and after the CSR has been initialized to 19H. CR19 shadows the bits in the write-only UART3 run-time FCR register.

TABLE 8-18: CR19

UART3 FCR SHADOW REGISTER				
TYPE: R (**Note 8-13**)		**DEFAULT:** N/A		
Bit No.	**Bit Name**	**Description**		
0	FIFO Enable	Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs		
1	RCVR FIFO Reset	Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. This bit is self clearing.		
2	XMIT FIFO Reset	Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. This bit is self-clearing.		
3	DMA Mode Select	Writing to this bit has no effect on the operation of the UART.		
4,5	Reserved	Read Only. A read returns 0.		
6,7	RCVR Trigger	These bits are used to set the trigger level for the RCVR FIFO interrupt.		
		BIT7	**BIT6**	**RCVR FIFO Trigger Level (BYTES)**
		0	0	1
		0	1	4
		1	0	8
		1	1	14

Note 8-13 This is a read only register. Software may set these register bits by writing the UART3 runtime FCR register located at an offset of +2 from the UART3 Base I/O Address. See Table 8-60, "I/O Base Address Configuration Register Description".

8.4.26 CR1A

CR1A can only be accessed in the configuration state and after the CSR has been initialized to 1AH. CR1A shadows the bits in the write-only UART4 run-time FCR register.

TABLE 8-19: CR1A

UART4 FCR SHADOW REGISTER				
TYPE: R (**Note 8-14**)		**DEFAULT:** N/A		
Bit No.	**Bit Name**	**Description**		
0	FIFO Enable	Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs		
1	RCVR FIFO Reset	Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. This bit is self clearing.		
2	XMIT FIFO Reset	Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. This bit is self-clearing.		
3	DMA Mode Select	Writing to this bit has no effect on the operation of the UART.		
4,5	Reserved	Read Only. A read returns 0.		
6,7	RCVR Trigger	These bits are used to set the trigger level for the RCVR FIFO interrupt.		
		BIT7	**BIT6**	**RCVR FIFO Trigger Level (BYTES)**
		0	0	1
		0	1	4
		1	0	8
		1	1	14

Note 8-14 This is a read only register. Software may set these register bits by writing the UART4 runtime FCR register located at an offset of +2 from the UART4 Base I/O Address. See Table 8-60, "I/O Base Address Configuration Register Description".

8.4.27 CR1B

CR1B can only be accessed in the configuration state and after the CSR has been initialized to 1BH. CR1B is used to select the base address of Serial Port 3 (UART3). The serial port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 3, set ADR9 and ADR8 to zero. Set CR1B.0 to 0 when writing the UART3 Base Address.

Serial Port 3 Address Decoding: address bits A[15:10] must be '000000' to access UART3 registers. A[2:0] are decoded as XXXb.

TABLE 8-20: CR1B

UART3 BASE ADDRESS REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0	Reserved	Read Only. A read returns 0.
1	ADR3	Serial Port 3 Base Address bits for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

8.4.28 CR1C

CR1C can only be accessed in the configuration state and after the CSR has been initialized to 1CH. CR1C is used to select the base address of Serial Port 4 (UART4). The serial port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 4, set ADR9 and ADR8 to zero. Set CR1C.0 to 0 when writing the UART4 Base Address.

Serial Port 4 Address Decoding: address bits A[15:10] must be '000000' to access UART4 registers. A[2:0] are decoded as XXXb.

TABLE 8-21: CR1C

UART4 BASE ADDRESS REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0	Reserved	Read Only. A read returns 0.
1	ADR3	Serial Port 4 Base Address bits for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

8.4.29 CR1D

CR1D can only be accessed in the configuration state and after the CSR has been initialized to 1DH. CR1D is used to select the IRQ for Serial Port 3 (bits 7 - 4) and for Serial Port 4 (bits 3 - 0). A value of 1-15 in the field selects the corresponding IRQ number. A value of zero selects no IRQ output (disabled). Shared IRQs are not supported in the SCH3221.

TABLE 8-22: CR1D

UART 3, 4 INTERRUPT SELECTION		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0-3	UART4 IRQ Select	These bits are used to select IRQ for Serial Port 4. (0 = Disabled)
4-7	UART3 IRQ Select	These bits are used to select IRQ for Serial Port 3. (0 = Disabled)

TABLE 8-23: UART INTERRUPT OPERATION

UARTx		IRQ
UARTx OUT2 bit	**UARTx IRQ Output State**	**UARTx IRQ State**
0	Z	Z
1	asserted	1
1	de-asserted	0

Note:

- It is the responsibility of the software to ensure that two IRQ's are not set to the same IRQ number. Potential damage to chip may result.
- Z = Don't Care.

8.4.30 CR1E

CR1E can only be accessed in the Configuration State and after the CSR has been initialized to 1EH.

TABLE 8-24: CR1E

CLOCK REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	CLOCKI32	Bit[0] (CLK32_PRSN) 0=32kHz clock is connected to the CLKI32 pin (default) 1=32kHz clock is not connected to the CLKI32 pin (pin is grounded)
1	Reserved	Reserved – Do not change its default setting of 0.
2-7	Reserved	Reserved – Read as 0.

8.4.31 CR1F

CR1F is reserved. The default value of this register after power up is 00H.

8.4.32 CR20

CR20 is reserved. The default value of this register after power up is 3CH.

8.4.33 CR21

CR21 is reserved. The default value of this register after power up is 00H.

8.4.34 CR22

CR22 is reserved. The default value of this register after power up is 00H.

8.4.35 CR23

CR23 is reserved. The default value of this register after power up is 00H.

8.4.36 CR24

CR24 can only be accessed in the configuration state and after the CSR has been initialized to 24H. CR24 is used to select the base address of Serial Port 1 (UART1). The serial port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 1, set ADR9 and ADR8 to zero. Set CR24.0 to 0 when writing the UART1 Base Address.

Serial Port 1 Address Decoding: address bits A[15:10] must be '000000' to access UART1 registers. A[2:0] are decoded as XXXb.

TABLE 8-25: CR24

UART1 BASE ADDRESS REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0	Reserved	Read Only. A read returns 0.
1	ADR3	Serial Port 1 Base Address bits for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

8.4.37 CR25

CR25 can only be accessed in the configuration state and after the CSR has been initialized to 25H. CR25 is used to select the base address of Serial Port 2 (UART2). Serial Port 2 can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 2, set ADR9 and ADR8 to zero. Set CR25.0 to 0 when writing the UART2 Base Address.

Serial Port 2 Address Decoding: address bits A[15:10] must be '000000' to access UART2 registers. A[2:0] are decoded as XXXb.

TABLE 8-26: CR25

UART2 BASE ADDRESS REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0	Reserved	Read Only. A read returns 0.
1	ADR3	Serial Port 2 Base Address bits for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

8.4.38 CR26

CR26 is reserved. The default value of this register after power up is FFH.

8.4.39 CR27

CR27 is reserved. The default value of this register after power up is 00H.

8.4.40 CR28

CR28 can only be accessed in the configuration state and after the CSR has been initialized to 28H. CR28 is used to select the IRQ for Serial Port 1 (bits 7 - 4) and for Serial Port 2 (bits 3 - 0). A value of 1-15 in the field selects the corresponding IRQ number. A value of zero selects no IRQ output (disabled). Shared IRQs are not supported in the SCH3221.

TABLE 8-27: CR28

UART INTERRUPT SELECTION		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
3:0	UART2 IRQ Select	These bits are used to select IRQ for Serial Port 2. (0 = Disabled)
7:4	UART1 IRQ Select	These bits are used to select IRQ for Serial Port 1. (0 = Disabled)

TABLE 8-28: UART INTERRUPT OPERATION

UARTx		IRQ
UARTx OUT2 Bit	**UARTx IRQ Output State**	**UARTx IRQ State**
0	Z	Z
1	asserted	1
1	de-asserted	0

Note:

- It is the responsibility of the software to ensure that two IRQ's are not set to the same IRQ number. Potential damage to chip may result.
- Z = Don't Care.

8.4.41 CR29

CR29 can only be accessed in the configuration state and after the CSR has been initialized to 29H. CR29 controls the HPMODE bit and is used to select the IRQ mapping (bits 0 - 3) for the IRQIN1 pin. A value of 1-15 in the field selects the corresponding IRQ number. A value of zero selects no IRQ output (disabled).

TABLE 8-29: CR29

IRQIN1/HPMODE/SIRQ_CLKRUN_En			
TYPE: R/W		**DEFAULT:** 0x80 on VCC POR	
Bit No.	**Bit Name**	**Description**	
0-3	IRQIN1	Selects the IRQ for IRQIN1. (See Application Note in "Section 6.9.2, "Routable IRQ Inputs".)	
4	HPMODE	See FIGURE 6-2: Infrared Interface Block Diagram on page 37	
		0	Select IRMODE (default)
		1	Select IRRX3
5-6	RESERVED	Not Writable, Reads Return "0"	
7	SIRQ_CLKRUN_EN	Serial IRQ and CLKRUN enable bit. 0 = Disable 1 = Enable (default)	

8.4.42 CR2A

CR2A can only be accessed in the configuration state and after the CSR has been initialized to 2AH. CR2A is used to select the IRQ mapping for the IRQIN2 and IRQIN3 pins. A value of 1-15 in the field selects the corresponding IRQ number. A value of zero selects no IRQ output (disabled).

TABLE 8-30: CR2A

IRQIN2		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0-3	IRQIN2	Selects the IRQ for IRQIN2.
4-7	IRQIN3	Selects the IRQ for IRQIN3.

8.4.43 CR2B

CR2B can only be accessed in the configuration state and after the CSR has been initialized to 2BH. CR2B is used to set the SCE (FIR) base address ADR[10:3]. The SCE base address can be set to 224 locations on 8-byte boundaries from 100H - 7F8H. To disable the SCE, set ADR10, ADR9 and ADR8 to zero.

SCE Address Decoding: address bits A[15:11] must be '00000' to access SCE registers. A[2:0] are decoded as XXXb.

TABLE 8-31: CR2B

SCE (FIR) BASE ADDRESS REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0	ADR3	FIR Base Address bits for decoder.
1	ADR4	
2	ADR5	
3	ADR6	
4	ADR7	
5	ADR8	
6	ADR9	
7	ADR10	

8.4.44 CR2C

CR2C can only be accessed in the configuration state and after the CSR has been initialized to 2CH. Bits D[3:0] of this register are used to select the DMA for the SCE (FIR). Bits D[7:4] are Reserved. Reserved bits cannot be written and return 0 when read. Any unselected DMA Request output (DRQ) is in tristate.

TABLE 8-32: CR2C

SCE (FIR) DMA SELECT REGISTER						
TYPE: R/W					**DEFAULT:** 0x0F on VCC POR	
Bit No.	**Bit Name**	**Description**				
3:0	DMA Select	**BIT3**	**BIT2**	**BIT1**	**BIT0**	**DMA SELECTED**
		0	0	0	0	DMA0
		0	0	0	1	DMA1
		0	0	1	0	DMA2
		0	0	1	1	DMA3
		0	1	0	0	RESERVED
		. .	. .	. .	. .	. .
		1	1	1	0	RESERVED
		1	1	1	1	NONE
7:4	Reserved	Read Only. A read returns 0.				

8.4.45 CR2D

CR2D can only be accessed in the configuration state and after the CSR has been initialized to 2DH. CR2D is used to set the IR Half Duplex Turnaround Delay Time for the IR port. This value is 0 to 25.5msec in 100µsec increments.

The IRCC v2.0 block includes an 8 bit IR Half Duplex Time-out register in SCE Register Block 5, Address 1 that interacts with configuration register CR2D. These two registers behave like the other IRCC Legacy controls where either source uniformly updates the value of both registers when either register is explicitly written using IOW or following a device-level POR. IRCC software resets do not affect these registers.

The IR Half Duplex Time-out is programmable from 0 to 25.5mS in 100µS increments, as follows:

IR HALF DUPLEX TIME-OUT = (CR2D) x 100µS

TABLE 8-33: CR2D

IR HALF DUPLEX TIMEOUT		
TYPE: R/W		**DEFAULT:** 0x03 on VCC POR
Bit No.	**Bit Name**	**Description**
0-7	IR Half Duplex Time Out	These bits are used to set the IR Half Duplex Turnaround Delay Time for the IR port. This value is 0 to 25.5msec in 100µsec increments.

8.4.46 CR2E

CR2E can only be accessed in the configuration state and after the CSR has been initialized to 2EH. CR2E is directly connected to SCE Register Block Three, Address 0x05 in the IRCC v2.0 block.

TABLE 8-34: CR2E

SOFTWARE SELECT A		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0-7	Software Select A	These bits are directly connected to SCE Register Block Three, Address 0x05 in the IRCC v2.0 block.

8.4.47 CR2F

CR2F can only be accessed in the configuration state and after the CSR has been initialized to 2FH. CR2F is directly connected to SCE Register Block Three, Address 0x06 in the IRCC v2.0 block.

TABLE 8-35: CR2F

SOFTWARE SELECT B		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0-7	Software Select B	These bits are directly connected to SCE Register Block Three, Address 0x06 in the IRCC v2.0 block.

8.4.48 CR30

CR30 can only be accessed in the configuration state and after the CSR has been initialized to 30H. CR30 is used to set the Runtime Register Block base address ADR[11:5]. The Runtime Register Block base address can be set to 120 locations on 32-byte boundaries from 100H – FE0H. To disable Runtime Registers Block set the Base Address to a value below 100h (i.e., set ADR11 – ADR8 to zero).

Runtime Register Address Decoding: To access registers located in the Runtime Register block the I/O address bits A[15:12] must be '0000' and the address bits A[11:5] must match the value programmed in the Base Address Register below. I/O address bits A[4:0] are used as the register offset value into the register block. (For example: If A[4:0] = '00000' then the PME_STS register will be accessed).

TABLE 8-36: CR30

RUNTIME REGISTERS BLOCK BASE ADDRESS		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0	Reserved	The bits in this register are used to program the location of the Runtime Register Block Base Address.
1	ADR5	
2	ADR6	
3	ADR7	
4	ADR8	
5	ADR9	
6	ADR10	
7	ADR11	

8.4.49 CR31

CR31 can only be accessed in the configuration state and after the CSR has been initialized to 31H. CR31 is GPIO Direction Register 1 and is used to select the direction of GP11-GP13 and GP16-GP17 pins.

TABLE 8-37: CR31

GPIO DIRECTION REGISTER 1		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	Reserved	The bits in this register are used to select the direction of the GP11-GP13 and GP16-GP17 pins. 0=Input 1=Output
1	GP11	
2	GP12	
3	GP13	
4	Reserved	
5	Reserved	
6	GP16	
7	GP17	

8.4.50 CR32

CR32 can only be accessed in the configuration state and after the CSR has been initialized to 32H. CR32 is GPIO Polarity Register 1 and is used to select the polarity of GP11-GP13 and GP16-GP17 pins.

TABLE 8-38: CR32

GPIO POLARITY REGISTER 1		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	Reserved	The bits in this register are used to select the polarity of the GP11-GP13 and GP16-GP17 pins. 0=Non-Inverted 1=Inverted
1	GP11	
2	GP12	
3	GP13	
4	Reserved	
5	Reserved	
6	GP16	
7	GP17	

8.4.51 CR33

CR33 can only be accessed in the configuration state and after the CSR has been initialized to 33H. CR33 is GPIO Direction Register 2. It is used to select the direction of GP20-GP23 pins.

TABLE 8-39: CR33

GPIO DIRECTION REGISTER 2		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	GP20	These bits are used to select the direction of the GP20-GP23. 0=Input 1=Output
1	GP21	
2	GP22	
3	GP23	
4	Reserved	Read Only. A read returns 0.
5	Reserved	Read Only. A read returns 0.
6	Reserved	Read Only. A read returns 0.
7	Reserved	Read Only. A read returns 0.

8.4.52 CR34

CR35 can only be accessed in the configuration state and after the CSR has been initialized to 34H. CR35 is GPIO Polarity Register 2. It is used to select the polarity of GP20-GP23 and IO_PME pins.

TABLE 8-40: CR34

GPIO POLARITY REGISTER 2		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	GP20	These bits are used to select the polarity of the GP20-GP23 pins. 0=Non-Inverted 1=Inverted
1	GP21	
2	GP22	
3	GP23	
4	Reserved	Read Only. A read returns 0.
5	IO_PME# Polarity select	This bit is used to select the polarity of the IO_PME# pin. 0=Non-Inverted 1=Inverted **Note:** configuring this pin function with non-inverted polarity will give an active low output signal. The output type can be either open drain or push-pull. (See CR39).
6	Reserved	Read Only. A read returns 0.
7	Reserved	Read Only. A read returns 0.

8.4.53 CR35

CR35 can only be accessed in the configuration state and after the CSR has been initialized to 35H. CR35 is GPIO Direction Register 3 and is used to select the direction of GP30-GP37 pins.

TABLE 8-41: CR35

GPIO DIRECTION REGISTER 3		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	GP30	The bits in this register are used to select the direction of the GP30-GP37 pins. 0=Input 1=Output
1	GP31	
2	GP32	
3	GP33	
4	GP34	
5	GP35	
6	GP36	
7	GP37	

8.4.54 CR36

CR36 can only be accessed in the configuration state and after the CSR has been initialized to 36H. CR36 is GPIO Polarity Register 3 and is used to select the polarity of GP30-GP37 pins.

TABLE 8-42: CR36

GPIO POLARITY REGISTER 3		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	GP30	The bits in this register are used to select the polarity of the GP30-GP37 pins. 0=Non-Inverted 1=Inverted
1	GP31	
2	GP32	
3	GP33	
4	GP34	
5	GP35	
6	GP36	
7	GP37	

8.4.55 CR37

CR37 can only be accessed in the configuration state and after the CSR has been initialized to 37H. CR37 is GPIO Direction Register 4 and is used to select the direction of GP40-GP47 pins.

TABLE 8-43: CR37

GPIO DIRECTION REGISTER 4		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	GP40	The bits in this register are used to select the direction of the GP40-GP47 pins. 0=Input 1=Output
1	GP41	
2	GP42	
3	GP43	
4	GP44	
5	GP45	
6	GP46	
7	GP47	

8.4.56 CR38

CR38 can only be accessed in the configuration state and after the CSR has been initialized to 38H. CR38 is GPIO Polarity Register 4 and is used to select the polarity of GP40-GP47 pins.

TABLE 8-44: CR38

GPIO POLARITY REGISTER 4		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	GP40	The bits in this register are used to select the polarity of the GP40-GP47 pins. 0=Non-Inverted 1=Inverted
1	GP41	
2	GP42	
3	GP43	
4	GP44	
5	GP45	
6	GP46	
7	GP47	

8.4.57 CR39

CR39 can only be accessed in the configuration state and after the CSR has been initialized to 39H. CR39 is GPIO Output Register and is used to select the output buffer of GP11-GP13 and GP16-GP17 pins.

TABLE 8-45: CR39

GPIO OUTPUT TYPE REGISTER 1		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	Reserved	The bits in this register are used to select the output buffer type of the GP11-GP13 and GP16-GP17 pins. 0=Push-pull 1=Open Drain
1	GP11	
2	GP12	
3	GP13	
4	Reserved	
5	Reserved	
6	GP16	
7	GP17	

8.4.58 CR3A

CR3A can only be accessed in the configuration state and after the CSR has been initialized to 3AH. CR3A is a test control register and all bits must be treated as Reserved.

Note:	All test modes are reserved for Microchip use. Activating test mode registers may produce undesired results.

TABLE 8-46: CR3A

TEST 5		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
Bit No.	**Bit Name**	**Description**
0	Test 32	RESERVED FOR MICROCHIP USE
1	Test 33	
2	Test 34	
3	Test 35	
4	Test 36	
5	Test 37	
6	Test 38	
7	Test 39	

8.4.59 CR3B – CR3F

CR3A – CR3F registers are reserved. Reserved registers cannot be written and return 0 when read. The default value of these registers after power up is 00H on VCC POR.

8.4.60 CR40

CR40 can only be accessed in the configuration state and after the CSR has been initialized to 40H. CR40 is GPIO Output Register and is used to select the output buffer for the GP20, GP21, GP23, and IO_PME# pins.

TABLE 8-47: CR40

GPIO/MISC OUTPUT TYPE REGISTER 2		
TYPE: R/W		**DEFAULT:** 0x80 on VTR POR
Bit No.	**Bit Name**	**Description**
0	GP20	The bits in this register are used to select the output buffer type of the GP20, GP21, GP23, and IO_PME# pins. 0=Push-pull 1=Open Drain
1	GP21	
2	Reserved	
3	GP23	
4	Reserved	
5	Reserved	
6	Reserved	
7	IO_PME#	

8.4.61 CR41

CR41can only be accessed in the configuration state and after the CSR has been initialized to 41H. CR41is GPIO Output Register and is used to select the output buffer of GP50 to GP57 pins.

TABLE 8-48: CR41

GPIO OUTPUT TYPE REGISTER 5		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	GP50	The bits in this register are used to select the output buffer type of GP50 to GP57 pins. 0=Push-pull 1=Open Drain
1	GP51	
2	GP52	
3	GP53	
4	GP54	
5	GP55	
6	GP56	
7	GP57	

8.4.62 CR42

CR42 can only be accessed in the configuration state and after the CSR has been initialized to 42H. CR42 is GPIO Direction Register 5 and is used to select the direction of GP50-GP57 pins.

TABLE 8-49: CR42

GPIO DIRECTION REGISTER 5		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	GP50	The bits in this register are used to select the direction of the GP50-GP57 pins. 0=Input 1=Output
1	GP51	
2	GP52	
3	GP53	
4	GP54	
5	GP55	
6	GP56	
7	GP57	

8.4.63 CR43

CR43 can only be accessed in the configuration state and after the CSR has been initialized to 43H. CR43 is GPIO Polarity Register 5 and is used to select the polarity of GP50-GP57 pins.

TABLE 8-50: CR43

GPIO POLARITY REGISTER 5		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0	GP50	The bits in this register are used to select the polarity of the GP50-GP57 pins. 0=Non-Inverted 1=Inverted
1	GP51	
2	GP52	
3	GP53	
4	GP54	
5	GP55	
6	GP56	
7	GP57	

8.4.64 CR44

CR44 can only be accessed in the configuration state and after the CSR has been initialized to 44H. The bits in this register are used to select an alternate function of GP11-GP13 pins.

TABLE 8-51: CR44

GPIO ALTERNATE FUNCTION SELECT REGISTER 1		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0,1	Reserved	Reads return 0.
2,3	GP11	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 Reserved 1 0 Reserved 1 1 Reserved
4,5	GP12	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 IO_SMI# (Note) 1 0 Reserved 1 1 Reserved See Note 8-15 below.

TABLE 8-51: CR44 (CONTINUED)

GPIO ALTERNATE FUNCTION SELECT REGISTER 1		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
6,7	GP13	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 IRQIN1 (Note) 1 0 LED1 1 1 Reserved See Note 8-16 below.

Note: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

Note 8-15 Selecting the IO_SMI# function with GP12 configured with non-inverted polarity will give an active low output signal. The output type can be programmed for open drain via CR39.

Note 8-16 See Application Note in Section 6.9.2, "Routable IRQ Inputs".

8.4.65 CR45

CR45 can only be accessed in the configuration state and after the CSR has been initialized to 45H. The bits in this register are used to select an alternate function of GP16-GP17 pins.

TABLE 8-52: CR45

GPIO ALTERNATE FUNCTION SELECT REGISTER 2		
TYPE: R/W		**DEFAULT:** 0x50 on VTR POR, BITS[7:4] VTR POR, VCC POR, and Hard Reset
Bit No.	**Bit Name**	**Description**
0,1	Reserved	Reads return 0.
2,3	Reserved	Reads return 0.
4,5	GP16	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO 0 1 Reserved (default) - Note 1 0 Reserved 1 1 Reserved See Note 8-17 below.
6,7	GP17	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO 0 1 Reserved (default) – Note 1 0 Reserved 1 1 Reserved See Note 8-18 below.

Note: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

Note 8-17 Bits[4:5] are reset on VTR POR, VCC POR, and Hard Reset. They must be reconfigured from their Reserved default to 00 before the GP16 pin functionality can be used.

Note 8-18 Bits[7:6] are reset on VTR POR, VCC POR, and Hard Reset. They must be reconfigured from their Reserved default to 00 before the GP17 pin functionality can be used.

8.4.66 CR46

CR46 can only be accessed in the configuration state and after the CSR has been initialized to 46H. The bits in this register are used to select an alternate function of GP20-GP23 pins.

TABLE 8-53: CR46

GPIO ALTERNATE FUNCTION SELECT REGISTER 3		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0,1	GP20	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 IRRX2 1 0 IRQIN3 1 1 Reserved
2,3	GP21	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 IRTX2 1 0 WDT 1 1 Reserved
4,5	GP22	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 HPMODE – Note 1 0 Reserved 1 1 Reserved See Note 8-19 below.
6,7	GP23	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 LED2 1 0 IRQIN2 (Note) 1 1 Reserved See Note 8-20 below.

Note: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

Note 8-19 HPMODE is programmable in the IRQIN1/HPMODE/SIRQ_CLKRUN_En Configuration Register at offset CR29. The default HPMODE is the IRMODE function.

Note 8-20 See Application Note in Section 6.9.2, "Routable IRQ Inputs".

8.4.67 CR47

CR47 is reserved. The default value of this register after power up is 00H.

8.4.68 CR48

CR48 can only be accessed in the configuration state and after the CSR has been initialized to 48H. The bits in this register are used to select an alternate function of GP30-GP33 pins.

TABLE 8-54: CR48

GPIO ALTERNATE FUNCTION SELECT REGISTER 5		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0,1	GP30	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nRI3 1 0 Reserved 1 1 Reserved
2,3	GP31	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nDCD3 1 0 Reserved 1 1 Reserved
4,5	GP32	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 nRXD3 1 0 Reserved 1 1 Reserved
6,7	GP33	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 nTXD3 1 0 Reserved 1 1 Reserved

Note: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

8.4.69 CR49

CR49 can only be accessed in the configuration state and after the CSR has been initialized to 49H. The bits in this register are used to select an alternate function of GP34-GP37 pins.

TABLE 8-55: CR49

GPIO ALTERNATE FUNCTION SELECT REGISTER 6		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0,1	GP34	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nDSR3 1 0 Reserved 1 1 Reserved
2,3	GP35	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nRTS3 1 0 Reserved 1 1 Reserved
4,5	GP36	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 nCTS3 1 0 Reserved 1 1 Reserved
6,7	GP37	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 nDTR3 1 0 Reserved 1 1 Reserved

Note: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

8.4.70 CR4A

CR4A can only be accessed in the configuration state and after the CSR has been initialized to 4AH. The bits in this register are used to select an alternate function of GP40-GP43 pins.

TABLE 8-56: CR4A

GPIO ALTERNATE FUNCTION SELECT REGISTER 7		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0,1	GP40	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nRI4 1 0 Reserved 1 1 Reserved
2,3	GP41	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nDCD4 1 0 Reserved 1 1 Reserved
4,5	GP42	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 nRXD4 1 0 Reserved 1 1 Reserved
6,7	GP43	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 nTXD4 1 0 Reserved 1 1 Reserved

Note: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

8.4.71 CR4B

CR4B can only be accessed in the configuration state and after the CSR has been initialized to 4BH. The bits in this register are used to select an alternate function of GP44-GP47 pins.

TABLE 8-57: CR4B

GPIO ALTERNATE FUNCTION SELECT REGISTER 8		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0,1	GP44	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nDSR4 1 0 Reserved 1 1 Reserved
2,3	GP45	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nRTS4 1 0 Reserved 1 1 Reserved
4,5	GP46	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 nCTS4 1 0 Reserved 1 1 Reserved
6,7	GP47	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 nDTR4 1 0 Reserved 1 1 Reserved

Note: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

8.4.72 CR4C

CR4C can only be accessed in the configuration state and after the CSR has been initialized to 4CH. The bits in this register are used to select an alternate function of GP50-GP53 pins.

TABLE 8-58: CR4C

GPIO ALTERNATE FUNCTION SELECT REGISTER 9		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0,1	GP50	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nRI2 1 0 Reserved 1 1 Reserved
2,3	GP51	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nDCD2 1 0 Reserved 1 1 Reserved
4,5	GP52	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 RXD2/IRRX 1 0 Reserved 1 1 Reserved
6,7	GP53	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 TXD2/IRTX 1 0 Reserved 1 1 Reserved

Note: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

8.4.73 CR4D

CR4D can only be accessed in the configuration state and after the CSR has been initialized to 4DH. The bits in this register are used to select an alternate function of GP54-GP57 pins.

TABLE 8-59: CR4D

GPIO ALTERNATE FUNCTION SELECT REGISTER 10		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
Bit No.	**Bit Name**	**Description**
0,1	GP54	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nDSR2 1 0 Reserved 1 1 Reserved
2,3	GP55	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nRTS2 1 0 Reserved 1 1 Reserved
4,5	GP56	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 nCTS2 1 0 Reserved 1 1 Reserved
6,7	GP57	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 nDTR2 1 0 Reserved 1 1 Reserved

Note: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

8.4.74 CR4E

CR4E is reserved. The default value of this register after power up is 00H.

8.4.75 CR4F

CR4F is reserved. The default value of this register after power up is 01H.

8.4.76 CR50

CR50 is reserved. The default value of this register after power up is 00H.

8.4.77 CR51

CR51 is reserved. The default value of this register after power up is 01H.

8.4.78 CR52

CR52 is reserved. The default value of this register after power up is 00H.

8.4.79 CR53

CR53 is reserved. The default value of this register after power up is 8CH.

8.4.80 CR54

CR54 is reserved. The default value of this register after power up is undefined.

8.5 Logical Device Base I/O Address and Range

TABLE 8-60: I/O BASE ADDRESS CONFIGURATION REGISTER DESCRIPTION

Logical Device	Register Index	Base I/O Range (Note 8-21)	Fixed Base Off Sets
Serial Port 1	0x24	[0x0100:0x03F8] on 8 byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
Serial Port 2	0x25	[0x0100:0x03F8] on 8-byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
	0x2B (FIR/CIR)	[0x100:0x07F8] on 8-byte boundaries	+0 : DR/SCEA/CIRC/IDH/(IRDACR/BOFH) +1 : INTID/SCEB/CIRCR/IDL/BOFL +2 : IER/FIFOT/CIRBR/CID/BWCL +3 : LSR/LSA/VERN/(BWCH/TDSH) +4 : LCA/(IRQL/DMAC)/TDSL +5 : LCB/RDSH +6 : BS/RDSL +7 : MCR
Runtime Register Block	0x30	[0x0100:0x0FE0] on 32-byte boundaries	+00 : PME_STS . . . +1B : PME_EN4 (See Table 7-1 in Section 7.0, "Runtime Registers" for Full List)

TABLE 8-60: I/O BASE ADDRESS CONFIGURATION REGISTER DESCRIPTION (CONTINUED)

Logical Device	Register Index	Base I/O Range (Note 8-21)	Fixed Base Off Sets
Config. Port	0x12, 0x13	[0x0100:0x07FE] on 2-byte boundaries	See Configuration Registers in Section 8.3, "Configuration Registers Summary," on page 63. They are accessed through the index and DATA ports located at the Configuration Port address and the Configuration Port address +1 respectively.
Serial Port 3	0x1B	[0x0100:0x03F8] on 8 byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
Serial Port 4	0x1C	[0x0100:0x03F8] on 8 byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR

Note 8-21 The Configuration Port is at either 0x02E or 0x04E (for SYSOPT=0 or SYSOPT=1) at power up and can be relocated via CR12 and CR13.

8.6 Note A. Logical Device IRQ and DMA Operation

1. IRQ and DMA Enable and Disable: Any time the IRQ or DMA channel for a logical block is disabled by a register bit in that logical block, the IRQ and/or DMA channel is disabled. This is in addition to the IRQ and DMA channel disabled by the Configuration Registers (active bit or address not valid).
   a) Serial Ports:
   Modem Control Register (MCR) Bit D2 (OUT2) - When OUT2 is a logic "0", the serial port interrupts disabled. Disabling DMA Enable bit, disables DMA for UART2. Refer to the IrCC specification.

9.0 OPERATIONAL DESCRIPTION

9.1 Maximum Ratings

Operating Temperature Range (Industrial) ..... $-40^{o}C$ to $+85^{o}C$
Operating Temperature Range (Commercial) ..... $0^{o}C$ to $+70^{o}C$
Storage Temperature Range..... -55^{o} to $+150^{o}C$
Lead Temperature Range .....Refer to JEDEC Spec. J-STD-020
Positive Voltage on any pin, with respect to Ground ..... V_{CC}+0.3V
Negative Voltage on any pin, with respect to Ground..... -0.3V
Maximum V_{CC}..... +5.5V

Note:

- Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.
- When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

9.2 DC Electrical Characteristics

(T_A Industrial = $-40^{0}C$ – $85^{0}C$, V_{CC} = +3.3 V ± 10%)

(T_A Commercial = $0^{0}C$ – $70^{0}C$, V_{CC} = +3.3 V ± 10%)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		100		mV	
IPD Type Input Buffer						
Low Input Level	V_{ILIPD}			0.8	V	TTL Levels
High Input Level	V_{IHIPD}	2.0			V	
Internal Pulldown			30		µA	

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
Input Leakage, I and IS Buffers						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{CC}
O6 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -3mA
IO8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
Leakage Current	I_{LEAK}			±10	µA	V_{IN} = 0 to V_{CC} (Note 9-1)
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
Leakage Current	I_{LEAK}			+10	µA	V_{IN} = 0 to V_{CC}
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
IO12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Leakage Current	I_{LEAK}			±10	µA	V_{IN} = 0 to V_{CC} (Note 9-1)
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
Leakage Current	I_{LEAK}			+10	µA	V_{IN} = 0 to V_{CC}

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
OD14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
Leakage Current	I_{LEAK}			+10	µA	V_{IN} = 0 to V_{CC}
OP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Leakage Current	I_{LEAK}			+10	µA	V_{IN} = 0 to V_{CC} (Note 9-1)
IOP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Leakage Current	I_{LEAK}			±10	µA	V_{IN} = 0 to V_{CC} (Note 9-1)
Backdrive Protect/ChiProtect (All pins excluding LAD[3:0], LDRQ#, LPCPD#, LFRAME#)	I_{IL}			± 10	µA	V_{CC} = 0V V_{IN} = 5.5V Max
5V Tolerant Pins (All pins excluding LAD[3:0], LDRQ#, LPCPD#, LFRAME#) Inputs and Outputs in High Impedance State	I_{IL}			± 10	µA	V_{CC} = 3.3V V_{IN} = 5.5V Max
LPC Bus Pins (LAD[3:0], LDRQ#, LPCPD#, LFRAME#)	I_{IL}			± 10	µA	V_{CC} = 0V and V_{CC} = 3.3V V_{IN} = 3.6V Max
V_{CC} Supply Current Active	I_{CC}			17	mA	All outputs open, all inputs transitioning from/ to 0V to/from 3.3V
Trickle Supply Voltage	V_{TR}	V_{CC} min -.5V (Note 9-3)		V_{CC} max	V	V_{CC} must not be greater than .5V above V_{TR}
V_{TR} Supply Current Active	I_{TR}			0.2 (Note 9-2)	mA	All outputs open, all inputs transitioning from/ to 0V to/from 3.3V

Note 9-1 All output leakages are measured with all pins in high impedance.

Note 9-2 Max I_{TR} with V_{CC} = 3.3V (nominal) is 0.2mA. Max I_{TR} with V_{CC} = 0V (nominal) is 60µA.

Note 9-3 The minimum value given for V_{TR} applies when V_{CC} is active. When V_{CC} is 0V, the minimum V_{TR} is 0V.

CAPACITANCE $T_A = 25^0C$; fc = 1MHz; V_{CC} = 3.3V ±10%

Parameter	Symbol	Limits			Units	Test Condition
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

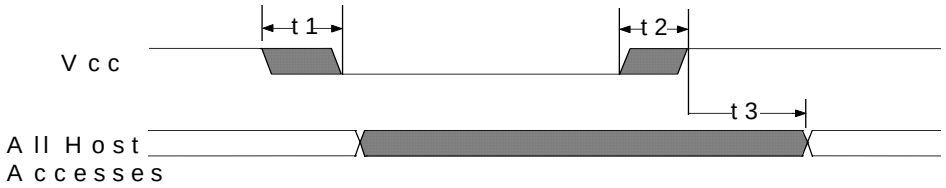
10.0 TIMING DIAGRAMS

For the Timing Diagrams shown, the following capacitive loads are used on outputs.

Name	Capacitance Total (pF)
SER_IRQ	50
nLAD[3:0]	50
LDRQ#	50
TXD1	50
TXD2	50
CLKRUN#	50

10.1 Power-up Timing

FIGURE 10-1: POWER-UP TIMING

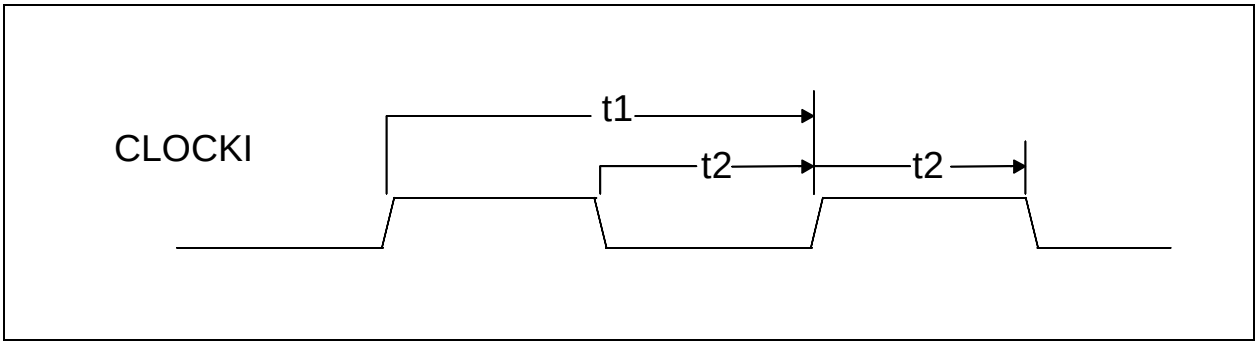


Name	Description	MIN	TYP	MAX	Units
t1	Vcc Slew from 2.7V to 0V	300			µs
t2	Vcc Slew from 0V to 2.7V	100			µs
t3	All Host Accesses After Powerup (Internal write-	125		500	µs

Note 10-1 Internal write-protection period after Vcc passes 2.7 volts on power-up.

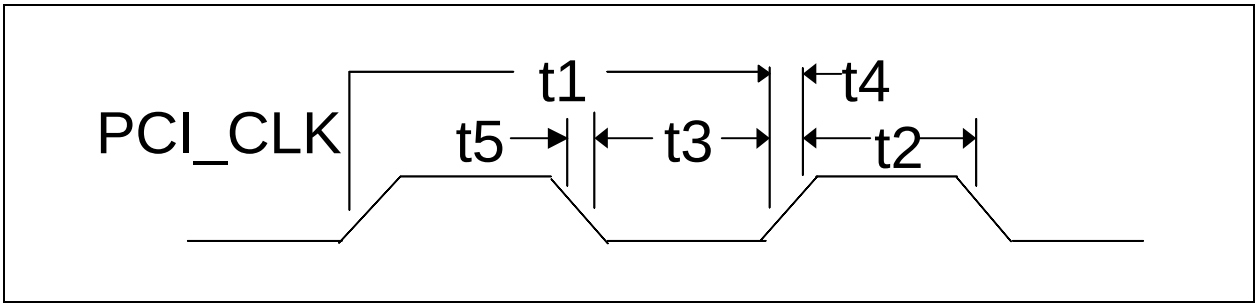
10.2 Input Clock Timing.

FIGURE 10-2: 14MHZ CLOCK TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Clock Cycle Time for 14.318MHZ		69.84		ns
t2	Clock High Time/Low Time for 14.318MHz	20	35		ns
	Clock Rise Time/Fall Time (not shown)			5	ns

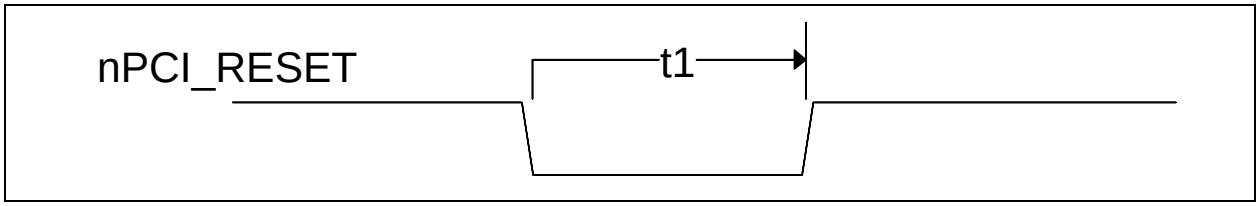
FIGURE 10-3: PCI CLOCK TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Period	30		33.3	nsec
t2	High Time	12			nsec
t3	Low Time	12			nsec
t4	Rise Time			3	nsec
t5	Fall Time			3	nsec

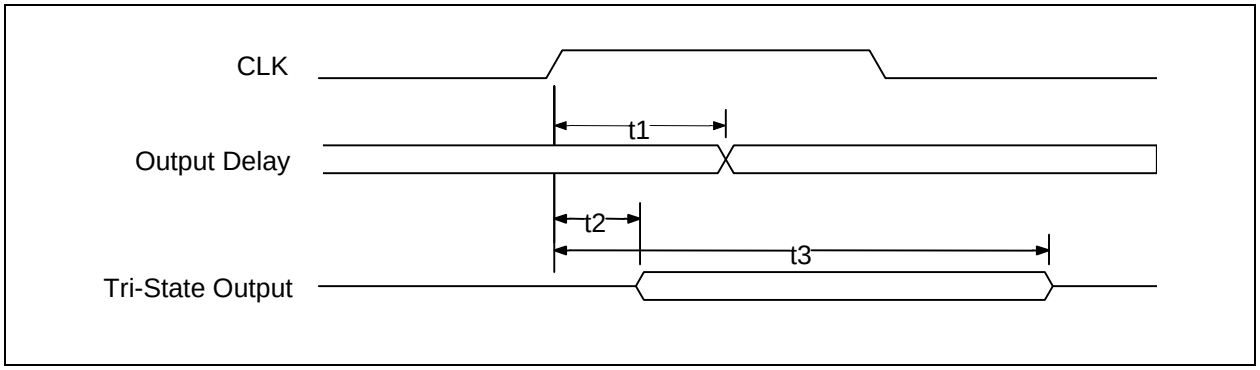
10.3 LPC Timing

FIGURE 10-4: RESET TIMING



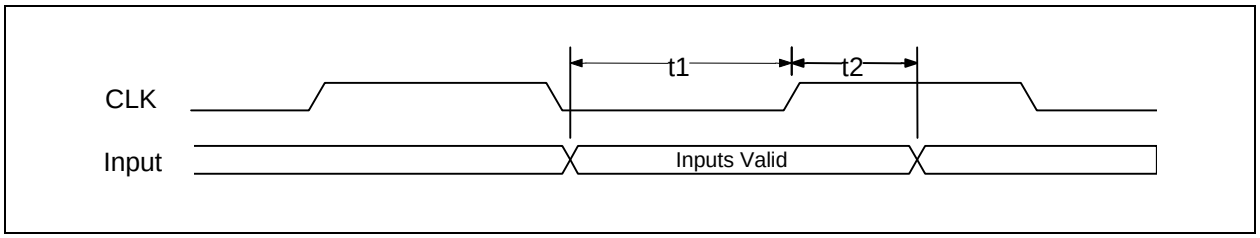
Name	Description	MIN	TYP	MAX	Units
t1	PCI_RESET# width	1			ms

FIGURE 10-5: OUTPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS



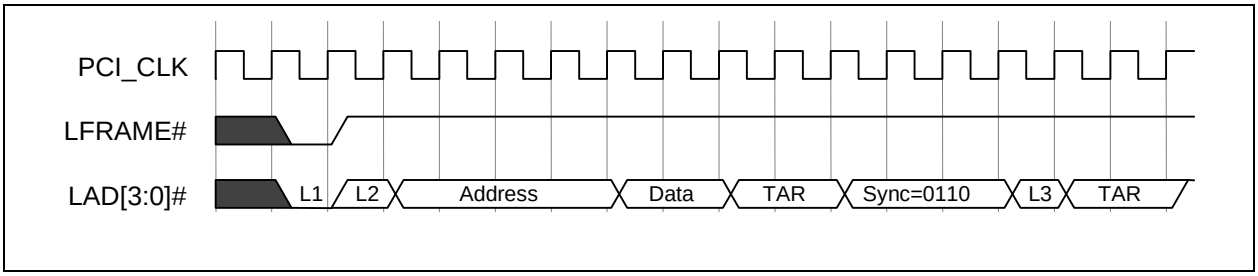
Name	Description	MIN	TYP	MAX	Units
t1	CLK to Signal Valid Delay – Bused Signals	2		11	ns
t2	Float to Active Delay	2		11	ns
t3	Active to Float Delay			28	ns

FIGURE 10-6: INPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS



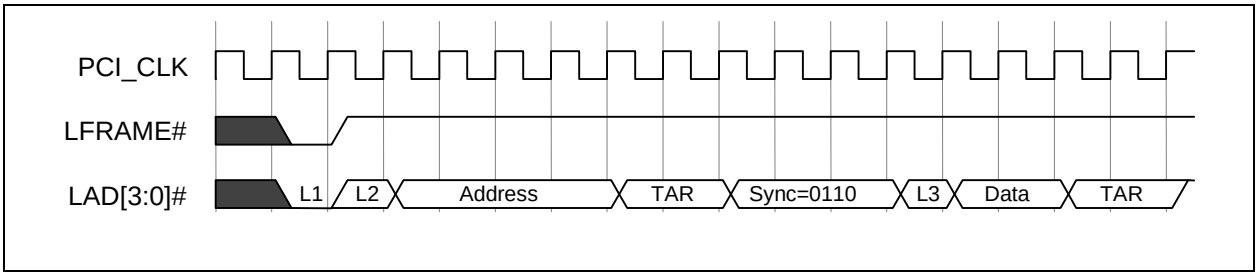
Name	Description	MIN	TYP	MAX	Units
t1	Input Set Up Time to CLK – Bused Signals	7			ns
t2	Input Hold Time from CLK	0			ns

FIGURE 10-7: I/O WRITE



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

FIGURE 10-8: I/O READ



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

FIGURE 10-9: DMA REQUEST ASSERTION THROUGH LDRQ#

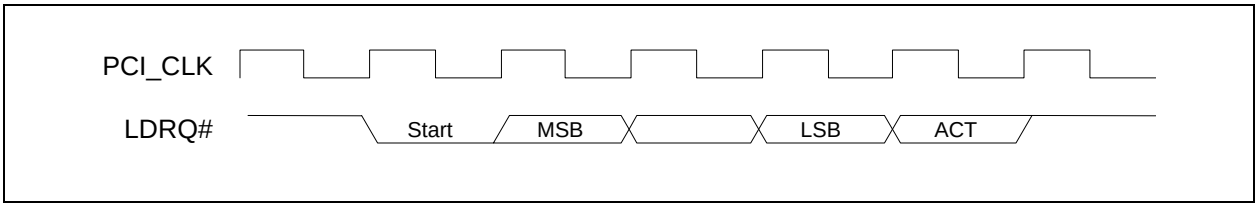
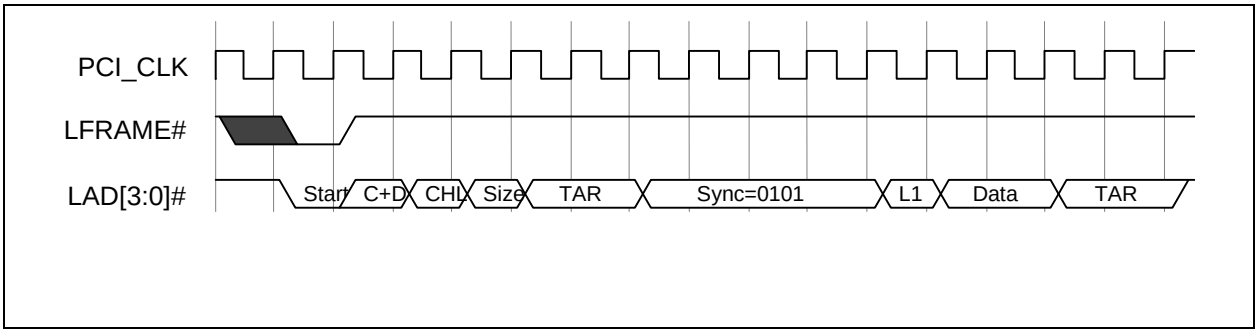
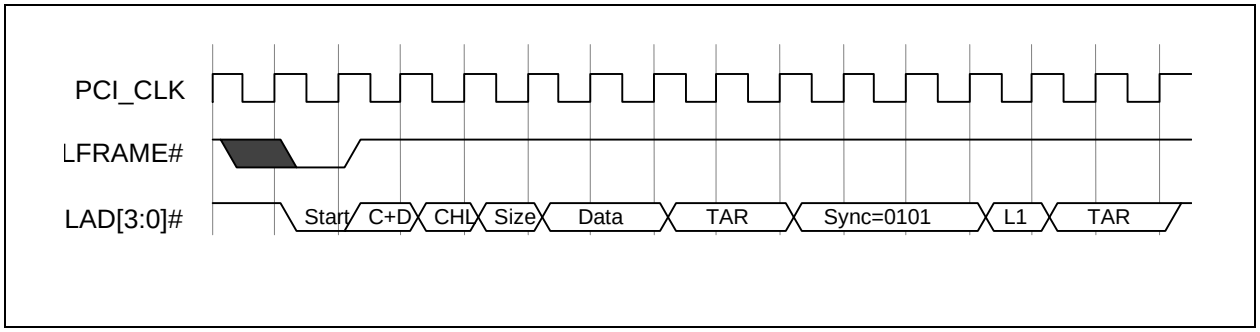


FIGURE 10-10: DMA WRITE (FIRST BYTE)



Note: L1=Sync of 0000

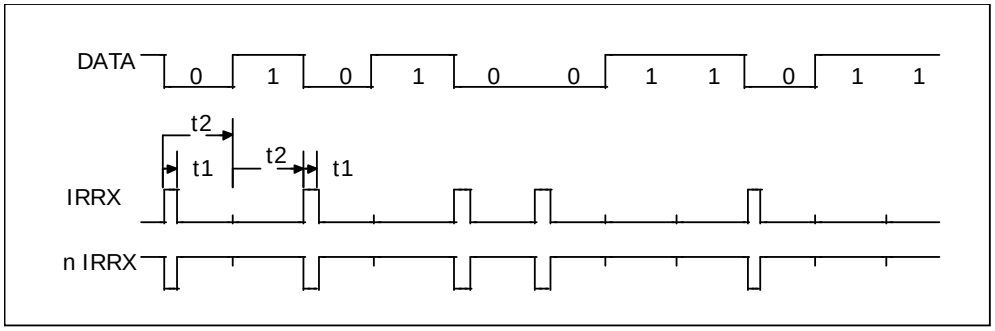
FIGURE 10-11: DMA READ (FIRST BYTE)



Note: L1=Sync of 0000

10.4 IR Timing

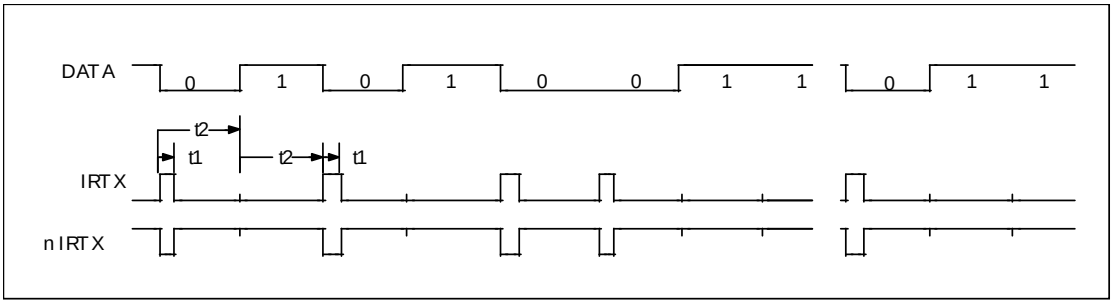
FIGURE 10-12: IRDA RECEIVE TIMING



	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:
1. Receive Pulse Detection Criteria: A received pulse is considered detected if the received pulse is a minimum of 1.41µs.
2. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)

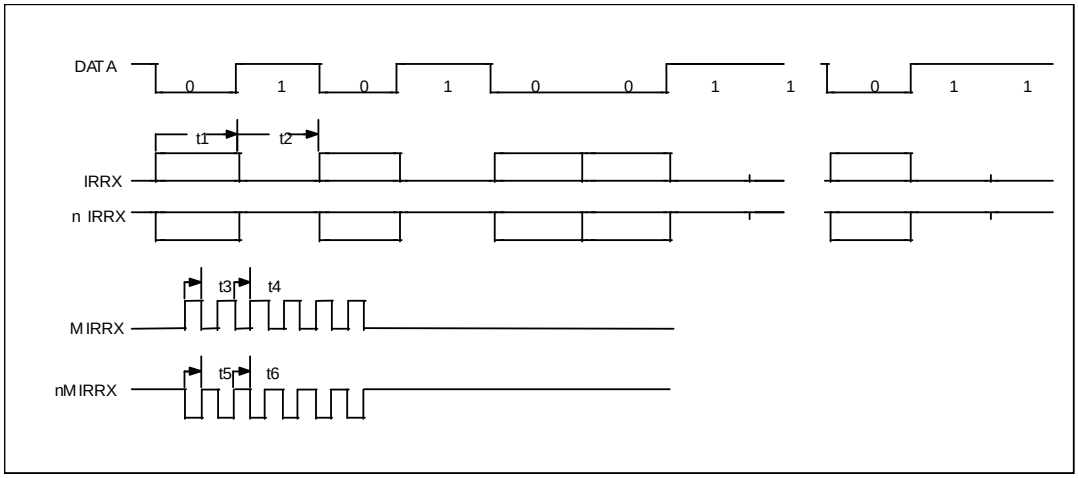
FIGURE 10-13: IRDA TRANSMIT TIMING



	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.41	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.41	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.41	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.41	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.41	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.41	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.41	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:
1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP 95LX and 48SX.
2. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0

FIGURE 10-14: AMPLITUDE SHIFT KEYED IR RECEIVE TIMING



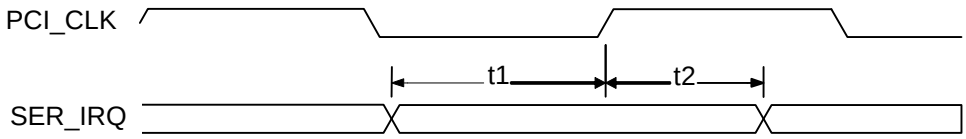
	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

1. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)
   MIRRX, nMIRRX are the modulated outputs

10.5 Serial IRQ Timing

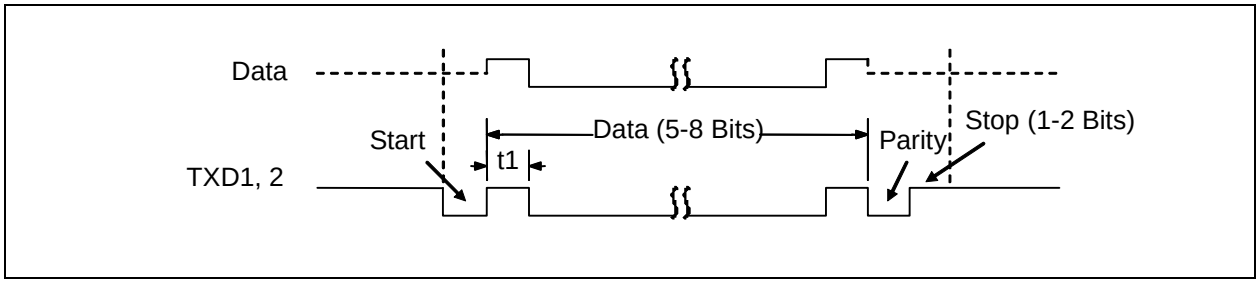
FIGURE 10-15: SETUP AND HOLD TIME



Name	Description	MIN	TYP	MAX	Units
t1	SER_IRQ Setup Time to PCI_CLK Rising	7			nsec
t2	SER_IRQ Hold Time to PCI_CLK Rising	0			nsec

10.6 UART Timing

FIGURE 10-16: SERIAL PORT DATA



Name	Description	MIN	TYP	MAX	Units
t1	Serial Port Data Bit Time		t_{BR} (Note 10-2)		nsec

Note 10-2 t_{BR} is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in the “Baud Rate” table in the “Serial Port” section.

11.0 XNOR-CHAIN TEST MODE

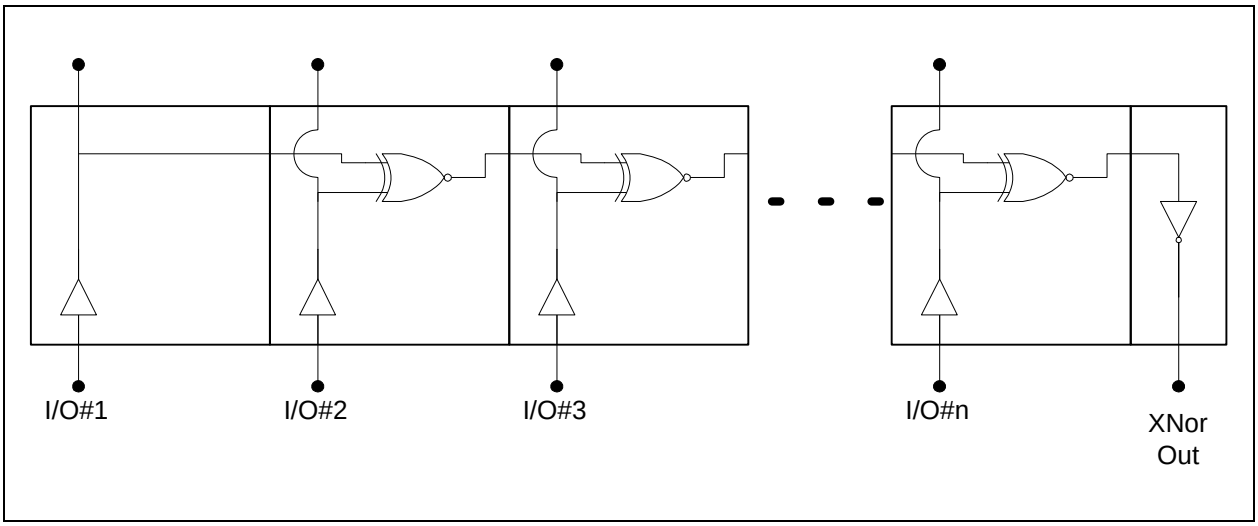
The SCH3221 provides board test capability through the implementation of XNOR chain. See following sub-sections.

XNOR-Chain test structure allows users to confirm that all pins are in contact with the motherboard during assembly and test operations. See Figure 11-1 below. When the chip is in the XNOR chain test mode, setting the state of any of the input pins to the opposite of its current state will cause the output of the chain to toggle.

The XNOR-Chain test structure must be activated to perform these tests. When the XNOR-Chain is activated, the SCH3221 pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR-Chain.

The tests that are performed when the XNOR-Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR-Chain output pin.

FIGURE 11-1: XNOR-CHAIN TEST STRUCTURE



11.1 Pin List of XNOR Chain

Pins on the chip are inputs to the first XNOR chain, with the exception of the following:

1. Power pins VCC and VTR
2. Ground pins VSS
3. PCI_RESET#
4. nIO_PME: This is the chain output.

Note that the pin named TEST is in fact one of the XNOR chain inputs, and for this purpose it is not special.

11.2 Setup of XNOR Chain

WARNING: Ensure power supply is off during setup.

1. Connect VSS pins to ground.
2. Connect VCC pins and VTR pin to VCC (a 3.3V source). Keep these voltages off for now.
3. Connect test equipment to monitor output on nIO_PME pin.
4. Hold PCI_RESET# to ground.
5. All other pins should be held to ground.

11.3 Testing Procedure

1. Turn power on, on all VTR and VCC pins.

2. Put the chip in XNOR chain test mode:

- Tie pins LAD0 and LFRAME# low.
- Then toggle PCI_RESET# from a low to a high state.
- Once the chip is put into XNOR chain test mode, LAD0 and LFRAME# become part of the chain.

3. The chip is now in XNOR chain test mode. The output, on nIO_PME, will reflect the XNOR function of all the input pins, toggling as individual pins are toggled, in any desired order.

4. To exit XNOR chain test mode:

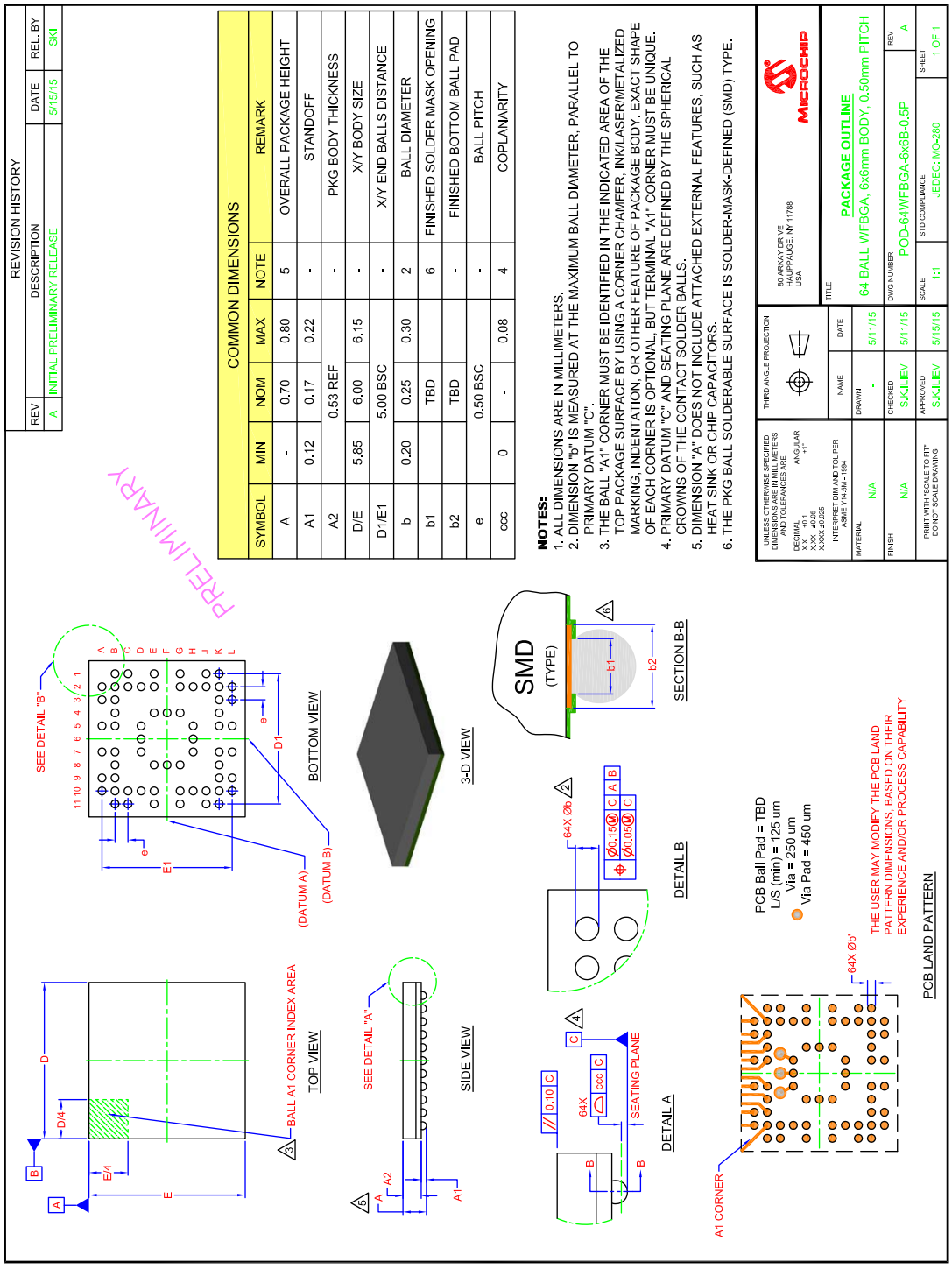
- Tie LAD0 or LFRAME# high.
- Then toggle PCI_RESET# from a low to a high state.

Note:	A VCC POR will also cause the XNOR chain test mode to be exited, regardless of the Mode. To verify the test mode has been exited, observe the output at nIO_PME. Toggling any of the input pins in the chain should not cause its state to change.

12.0 PACKAGE OUTLINE

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

FIGURE 12-1: 64-PIN WFBGA PACKAGE OUTLINE



APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002120A (02-29-16)	Document Release	

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PART NO.	[X]	-	XX	-	[XX]
Device	Temperature Range		Package		Tape and Reel Option

Device:	SCH3221	
Temperature Range:	Blank =	0°C to +70°C (Commercial)
	I =	-40°C to +85°C (Industrial)
Package:	7U =	64-pin WFBGA
Tape and Reel Option:	Blank =	Standard packaging (tray)
	TR =	Tape and Reel (Note 1)

Examples:

c) SCH3221-7U
Commercial temperature, 64-pin WFBGA, Tray

d) SCH3221I-7U-TR
Industrial temperature, 64-pin WFBGA, Tape & Reel

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