

# Contact Monitoring and Dual Low-Side Protected Driver

The 33287 interfaces between switch contacts and a microcontroller. Eight switch-to-battery (or switch-to-ground) sense monitor switch status. Additionally, two internal low-side switches are available to control inductive or capacitive loads.

The 33287 has eight sense inputs (rated at 40 V) with thresholds ratiometric to  $V_{BAT}$ . One sense input has a dedicated output for direct interfacing to the MCU and the remaining seven inputs are multiplexed interfaced to the MCU.

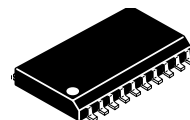
The two low-side switch outputs are current limited to 535 mA and internally clamped to 50 V. Outputs also have independent overtemperature shutdown and diagnostic reporting.

## Features

- Eight High-Voltage Sense Inputs
- Direct Interfacing to Microcontroller
- Two Current Limited Low-Side Drivers
- Drivers Internally Overvoltage Clamped and Thermally Protected
- 55  $\mu$ A Standby Current
- Pb-Free Packaging Designated by Suffix Code EG

**33287**

**AUTOMOTIVE CONTACT MONITORING AND  
DUAL LOW-SIDE PROTECTED DRIVER**



**DW SUFFIX  
EG SUFFIX (PB-FREE)  
98ASB42343B  
20-PIN SOICW**

## ORDERING INFORMATION

Device	Temperature Range ( $T_A$ )	Package
MC33287DW/R2	-40 to 125°C	20 SOICW
MCZ33287EG/R2		

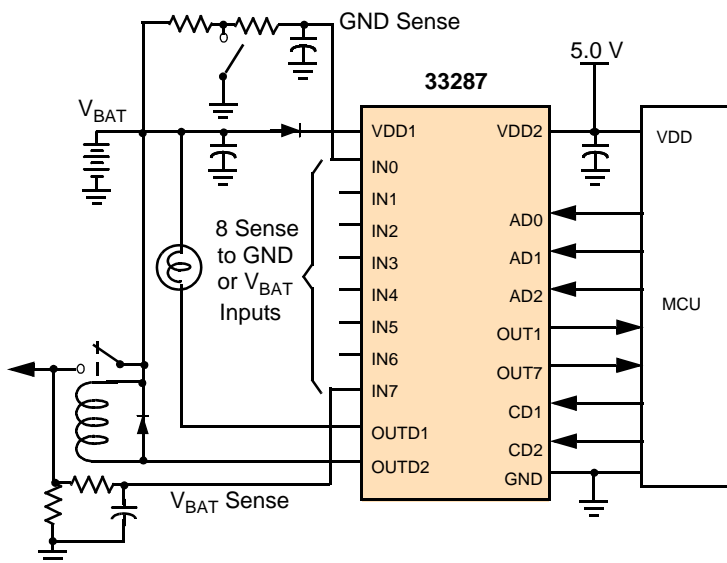


Figure 1. Simplified Application Design

### INTERNAL BLOCK DIAGRAM

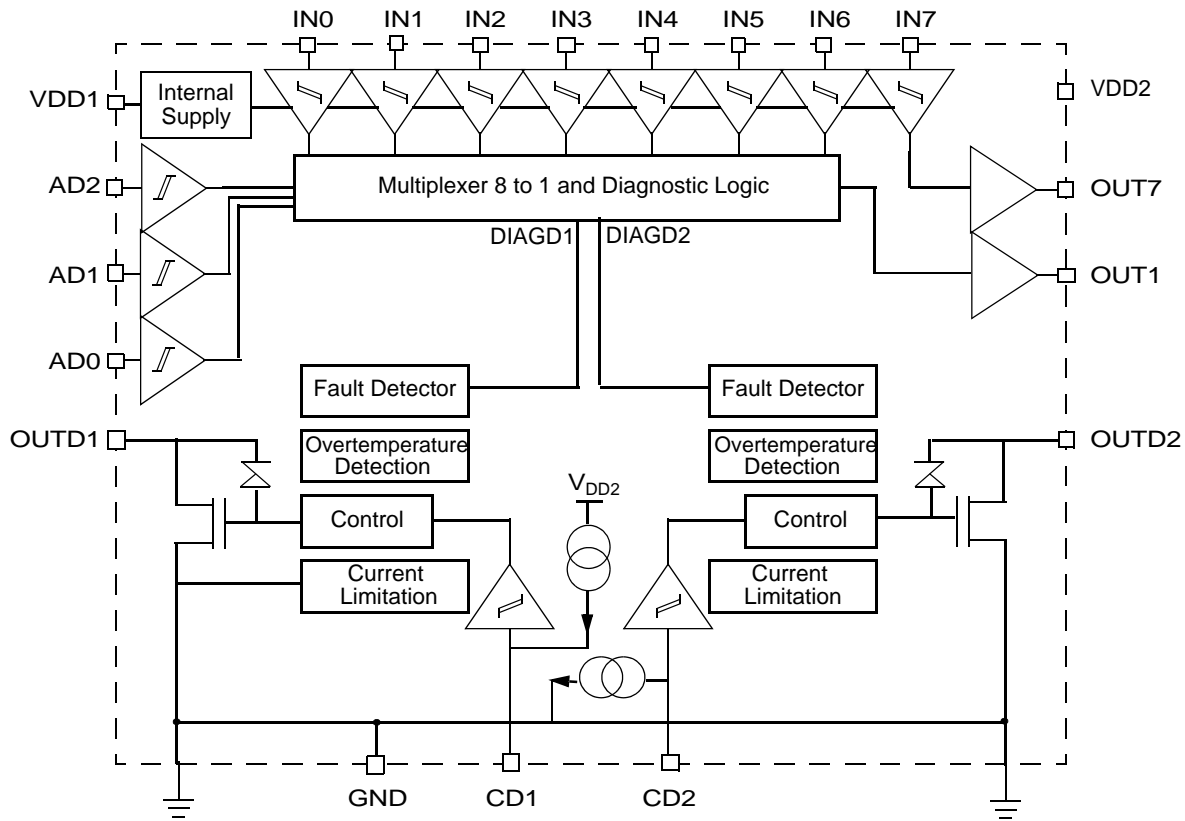


Figure 2. 33287 Simplified Internal Block Diagram

# PIN CONNECTIONS

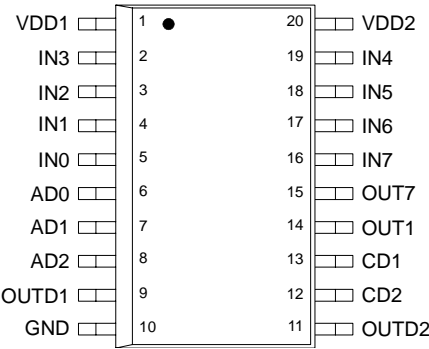


Figure 3. 33287 Pin Connections

Table 1. 33287 Pin Definitions

Pin Number	Pin Name	Formal Name	Definition
1, 20	V <sub>DD1</sub> , V <sub>DD2</sub>	Voltage Power	These are high-voltage power supply 5.0 V pins (V <sub>BAT</sub> ).
5, 4, 3, 2, 19, 18, 17, 16	IN0 – IN7	Input 0 – 7	These are high-voltage input pins.
6, 7, 8	AD0 – AD2	Address	These pins are the addresses for mode and input selection.
9, 11	OUTD1, OUTD2	Output Drain	These two are output driver pins (drain).
10	GND	Ground	This pin is the ground for the logic and analog circuitry of the device.
12, 13	CD1, CD2	Command Driver	These are the two driver command pins.
14	OUT1	Output 1	This is the output (multiplexed Output 1 = 0 to 6.0 V for IN0 to IN6 and DIAGD1 or DIAGD2) and DIAGD2 pins.
15	OUT7	Output 7	This is the direct output from IN7 pin.

## ELECTRICAL CHARACTERISTICS

### MAXIMUM RATINGS

**Table 2. MAXIMUM RATINGS**

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Power Supply Voltage Normal Operation (Steady-State) Load Dump Conditions	$V_{DD1}$	24 40	V
Logic Supply Voltage (Continuous)	$V_{DD2}$	7.0	V
Input Pin Voltage <sup>(1)</sup>	$V_{IN}$	40	V
ESD Voltage <sup>(2)</sup> Human Body Model Machine Model	$V_{ESD1}$ $V_{ESD2}$	$\pm 2000$ $\pm 200$	V
Operating Ambient Temperature	$T_A$	-40 to 125°C	°C
Storage Temperature	$T_{STG}$	-65 to 150	°C
Power Dissipation ( $T_A = 85^\circ\text{C}$ )	$P_D$	0.7	W
Peak Package Reflow Temperature During Reflow <sup>(3), (4)</sup>	$T_{PPRT}$	Note 4.	°C
Thermal Resistance Junction-to-Ambient	$R\theta_{J-A}$	100	°C/W

**Notes**

- 1 With Serial Resistor  $\geq 25 \text{ k}\Omega$
- 2 ESD1 testing is performed in accordance with the Human Body Model ( $C_{ZAP}=100 \text{ pF}$ ,  $R_{ZAP}=1500 \Omega$ ), ESD2 testing is performed in accordance with the Machine Model ( $C_{ZAP}=200 \text{ pF}$ ,  $R_{ZAP}=0 \Omega$ ).
- 3 Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- 4 Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

### STATIC ELECTRICAL CHARACTERISTICS

**Table 3. STATIC ELECTRICAL CHARACTERISTICS**

Characteristics noted under conditions  $7.0\text{ V} \leq V_{DD1} \leq 18\text{ V}$ ,  $4.75\text{ V} \leq V_{DD2} \leq 5.25\text{ V}$ ,  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ , unless otherwise noted. Extended limit is  $5.0\text{ V} \leq V_{DD1} \leq 7.0\text{ V}$  and other parameters are full specification in this mode. Inputs IN1–IN7 and low-side drivers are still functional with down-graded characteristics.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>SUPPLY VOLTAGE (<math>V_{DD1}</math> AND <math>V_{DD2}</math> PINS)</b>					
Operational Supply Voltage	VDD1				V
Full Specification		7.0	12	18	
Extend Limit		5.0	—	7.0	
Operational Supply Voltage (Full Specification)	VDD2	4.75	—	—	V
Supply Current Standby Mode <sup>(5)</sup>					$\mu\text{A}$
$V_{DD1} \leq 14\text{ V}$	IVDD1-0	—	55	110	
$V_{CD1} = V_{DD2}$ , $V_{CD2} = 0\text{ V}$	IVDD2-0	—	—	10	
Supply Current in Drivers on Configuration (Full Specification) <sup>(5)</sup>					$\mu\text{A}$
$V_{CD1} = 0\text{ V}$	IVDD1-1	—	250	1500	
$V_{CD2} = V_{DD2}$	IVDD2-1	—	650	1500	
<b>OUTPUT DRIVERS CHARACTERISTICS (OUTD1 AND OUTD2 PINS)</b>					
Output Resistance (Full Specification and $T_J \leq 130^{\circ}\text{C}$ )	R <sub>DS(ON)</sub>	—	1.40	3.20	$\Omega$
Output Resistance (Extent Limit and $T_J \leq 130^{\circ}\text{C}$ )	R <sub>DS(ON)</sub>	—	—	5.0	$\Omega$
Leakage Current (Internal Current Source)	I <sub>LEAK</sub>	1.0	—	13	$\mu\text{s}$
<b>PROTECTION AND LEVEL DETECTION (OUTD1 AND OUTD2 PINS)</b>					
Positive Output Clamp	V <sub>CLAMP</sub>	40	50	60	V
Output Current Limitation ( $130^{\circ}\text{C} \geq T_J$ )	I <sub>LIM</sub>	300	535	750	mA
Output Fault Detector Level	V <sub>FAULT</sub>	2.0	2.75	3.5	V
Overtemperature Detection (at $25^{\circ}\text{C}$ by Function Simulation)	T <sub>DETEC</sub>	145	160	175	$^{\circ}\text{C}$
<b>INPUTS (CD1 AND CD2 PINS)</b>					
Input Voltage Low	V <sub>IL</sub>	—	—	$4.0 \times V_{DD2}$	V
Input Voltage High	V <sub>IH</sub>	$8.0 \times V_{DD2}$	—	—	V
Hysteresis	V <sub>HST</sub>	500	800	—	mV
Input Current on Pin CD1 (Internal Pull-Up and CD1 Connected to Ground)	I <sub>CD1</sub>	-100	-30	-10	$\mu\text{A}$
Leakage Current on Pin CD1 (Internal Pull-Up Connected to $V_{DD2}$ )	I <sub>LEAK</sub>	-5.0	—	5.0	$\mu\text{A}$
Input Current on Pin CD2 (Internal Pull Down CD2 Connected to $V_{DD2}$ )	I <sub>CD2</sub>	10	30	100	$\mu\text{A}$
Leakage Current on Pin CD2 (Internal Pull-Up CD1 Connected to Ground)	I <sub>LEAK</sub>	-5.0	—	5.0	$\mu\text{A}$

Notes

- 5 All INn and ADn inputs are connected to ground.

**Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)**

Characteristics noted under conditions  $7.0\text{ V} \leq V_{DD1} \leq 18\text{ V}$ ,  $4.75\text{ V} \leq V_{DD2} \leq 5.25\text{ V}$ ,  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ , unless otherwise noted. Extended limit is  $5.0\text{ V} \leq V_{DD1} \leq 7.0\text{ V}$  and other parameters are full specification in this mode. Inputs IN1–IN7 and low-side drivers are still functional with down-graded characteristics.

Characteristic	Symbol	Min	Typ	Max	Unit
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**INPUTS (IN0 TO IN7 PINS)**

Input Voltage Low (Full Specification)	$V_{IL}$	—	—	$4.0 \times V_{DD1}$	V
Input Voltage Low (Extended Limit)	$V_{IL}$	—	—	$3.0 \times V_{DD1}$	V
Input Voltage High (Full Specification and Extended Limit)	$V_{IH}$	$7.0 \times V_{DD1}$	—	—	V
Hysteresis ( $5.0\text{ V} < V_{DD1} < 16\text{ V}$ )	$V_{HYS}$	5.0	1.0	—	V
Input Current ( $V_{IN} < 16\text{ V}$ )	$I_{LEAK}$	5.0	—	5.0	$\mu\text{A}$
Input Voltage Clamp ( $I = 100\text{ }\mu\text{A}$ )	$V_{INCLAMP}$	17	20	23	V

**INPUTS (AD0, AD1, AND AD2 PINS)**

Input Voltage Low	$V_{IL}$	—	—	$4.0 \times V_{DD2}$	V
Input Voltage High	$V_{IH}$	$8.0 \times V_{DD2}$	—	—	V
Hysteresis	$V_{HYS}$	500	750	—	mV
Input Current	$I_{LEAK}$	-5.0	—	5.0	$\mu\text{A}$

**OUTPUTS (OUT1 AND OUT7 PINS)**

Output Voltage Low ( $I_{LOAD} = 2.0\text{ mA}$ )	$V_{OL}$	—	—	$2.0 \times V_{DD2}$	V
Output Voltage High ( $I_{LOAD} = -2.0\text{ mA}$ )	$V_{OH}$	$8.0 \times V_{DD2}$	—	—	V

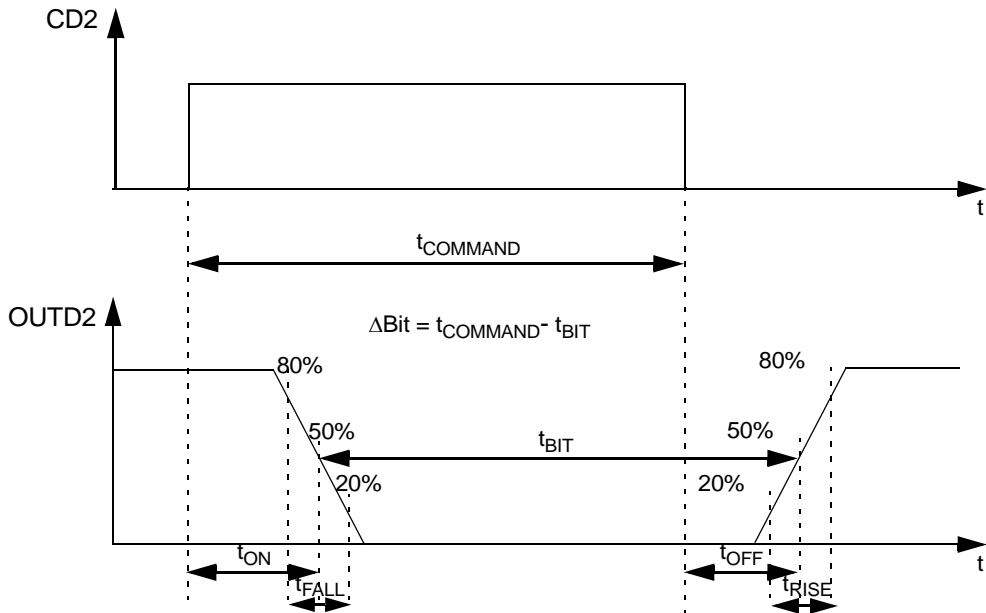
### *DYNAMIC ELECTRICAL CHARACTERISTICS*

**Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS**

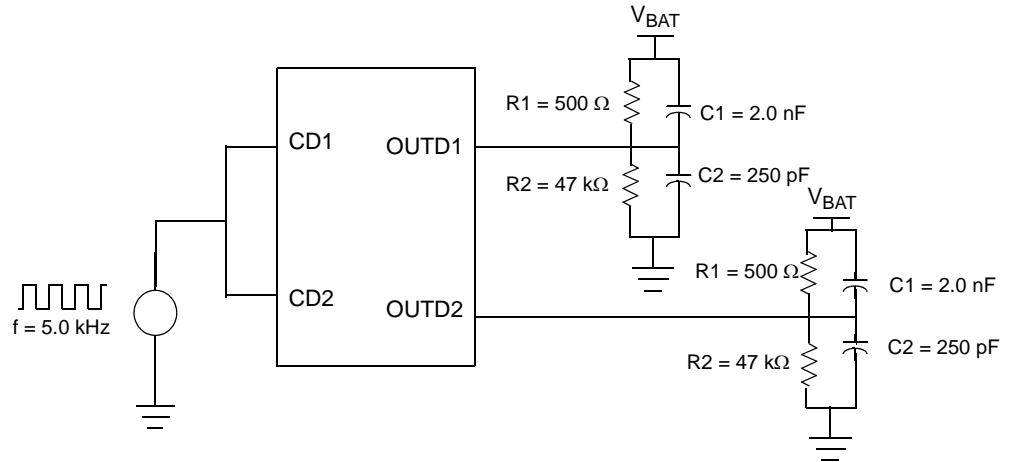
Characteristics noted under conditions  $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $9.0\text{ V} \leq V_{PWR} \leq 16\text{ V}$ ,  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ , unless otherwise noted. Typical values noted reflect the approximate parameter mean at  $T_A = 25^{\circ}\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OUTPUT DRIVERS CHARACTERISTICS (OUTD1 AND OUTD2 PINS)</b>					
Turn ON Delay Time	$t_{ON}$	—	1.3	10	$\mu\text{s}$
Turn OFF Delay Time	$t_{OFF}$	—	2.1	10	$\mu\text{s}$
Output Rising Edge	$t_{RISE}$	—	2.8	10	$\mu\text{s}$
Output Falling Edge	$t_{FALL}$	—	1.0	10	$\mu\text{s}$
Difference Between Command Duration and Bit Duration	$\Delta_{BIT}$	-5.0	—	5.0	$\mu\text{s}$

**TIMING DIAGRAMS**



**Figure 4. Timing Characteristics**



**Figure 5. Timing Test Configuration**



## FUNCTIONAL DEVICE OPERATION

### LOGIC COMMANDS AND REGISTERS

**Table 5. Drivers Function Table**

CD1 <sup>(6)</sup>	OUTD1	DIAGD1 <sup>(8)</sup>	Status
High Level for Logic Signals	High Level for Drivers Outputs	High Level for Logic Signals	Driver 1 Normally OFF
Low Level for Logic Signals	Low Level for Drivers Outputs	High Level for Logic Signals	Driver 1 Normally ON
High Level for Logic Signals	Low Level for Drivers Outputs	Low Level for Logic Signals	Driver 1 Shorted to GND or Open Load
Low Level for Logic Signals	High Level for Drivers Outputs	Low Level for Logic Signals	Driver 1 Overloaded
CD2 <sup>(7)</sup>	OUTD2	DIAGD2	Status
Low Level for Logic Signals	High Level for Drivers Outputs	High Level for Logic Signals	Driver 2 Normally OFF
High Level for Logic Signals	Low Level for Drivers Outputs	High Level for Logic Signals	Driver 2 Normally ON
Low Level for Logic Signals	Low Level for Drivers Outputs	Low Level for Logic Signals	Driver 2 Shorted to GND or Open Load
High Level for Logic Signals	High Level for Drivers Outputs	Low Level for Logic Signals	Driver 2 Overloaded

Notes

- 6 CD1 is active on low level (driver 1 is on when CD1 is low).
- 7 CD2 is active on high level (driver 2 is on when CD2 is high).
- 8 DIAGD1 output is neither latched nor filtered.

**Table 6. Eight-to-One Data Multiplexer Function**

Inputs			OUT1
AD2	AD1	AD0	
High Impedance	High Impedance	High Impedance	Unknown
Low Level	Low Level	Low Level	IN0 <sup>(9)</sup>
Low Level	Low Level	High Level	IN1
Low Level	High Level	Low Level	IN2
Low Level	High Level	High Level	IN3
High Level	Low Level	Low Level	IN4
High Level	Low Level	High Level	IN5
High Level	High Level	Low Level	IN6
High Level	High Level	High Level	DIAGD1 or DIAGD2 <sup>(10)</sup>

Notes

- 9 IN0 to IN6 are the normalized values.
- 10 DIAGD1 or DIAGD2 are the values of the selected internal fault detector. See [Table 7](#).

**Table 7. Fault Detector Selection**

Inputs			OUT1
AD2	AD1	AD0	
Unknown	Unknown	Unknown	Unknown
Unknown	Low Level	High Level	Unknown
High Level	High Level	High Level	DIAGD1
Unknown	Unknown	Unknown	Unknown
Unknown	High Level	Low Level	Unknown
High Level	High Level	High Level	DIAGD2

### TYPICAL APPLICATIONS

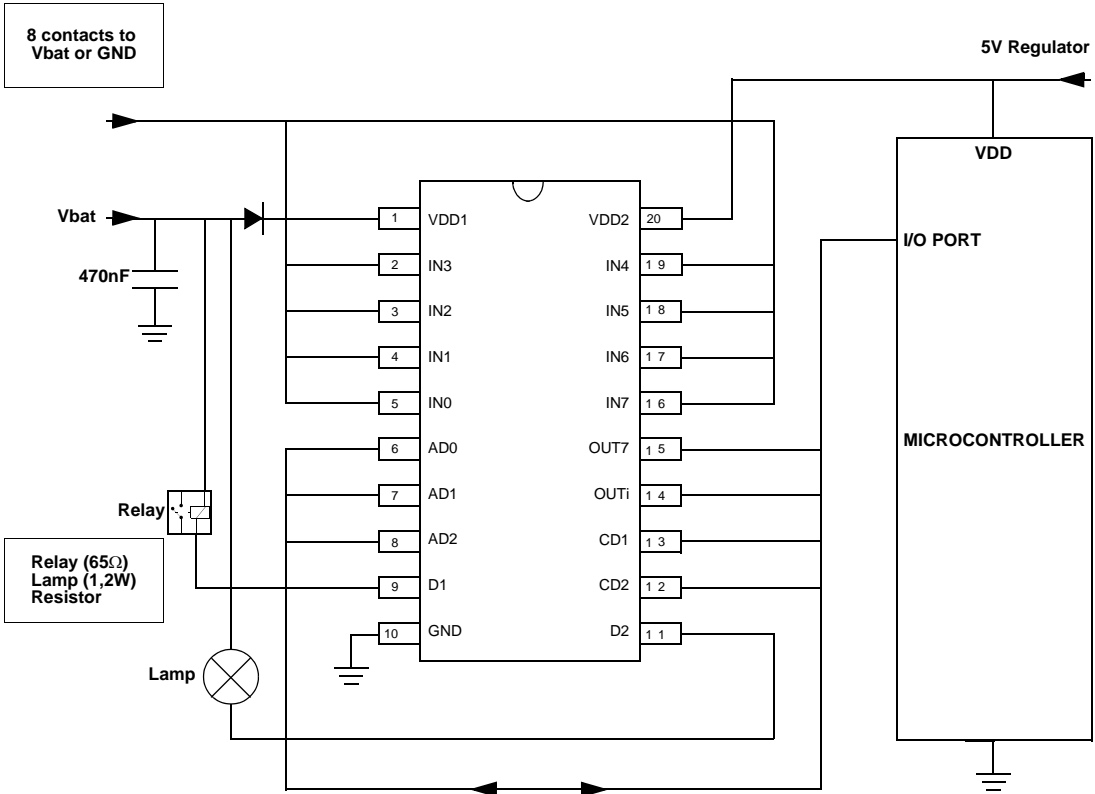


Figure 6. Typical Application Configuration

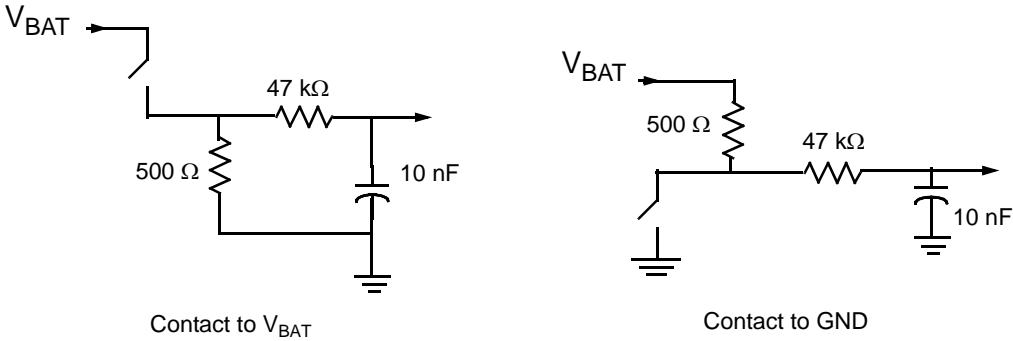
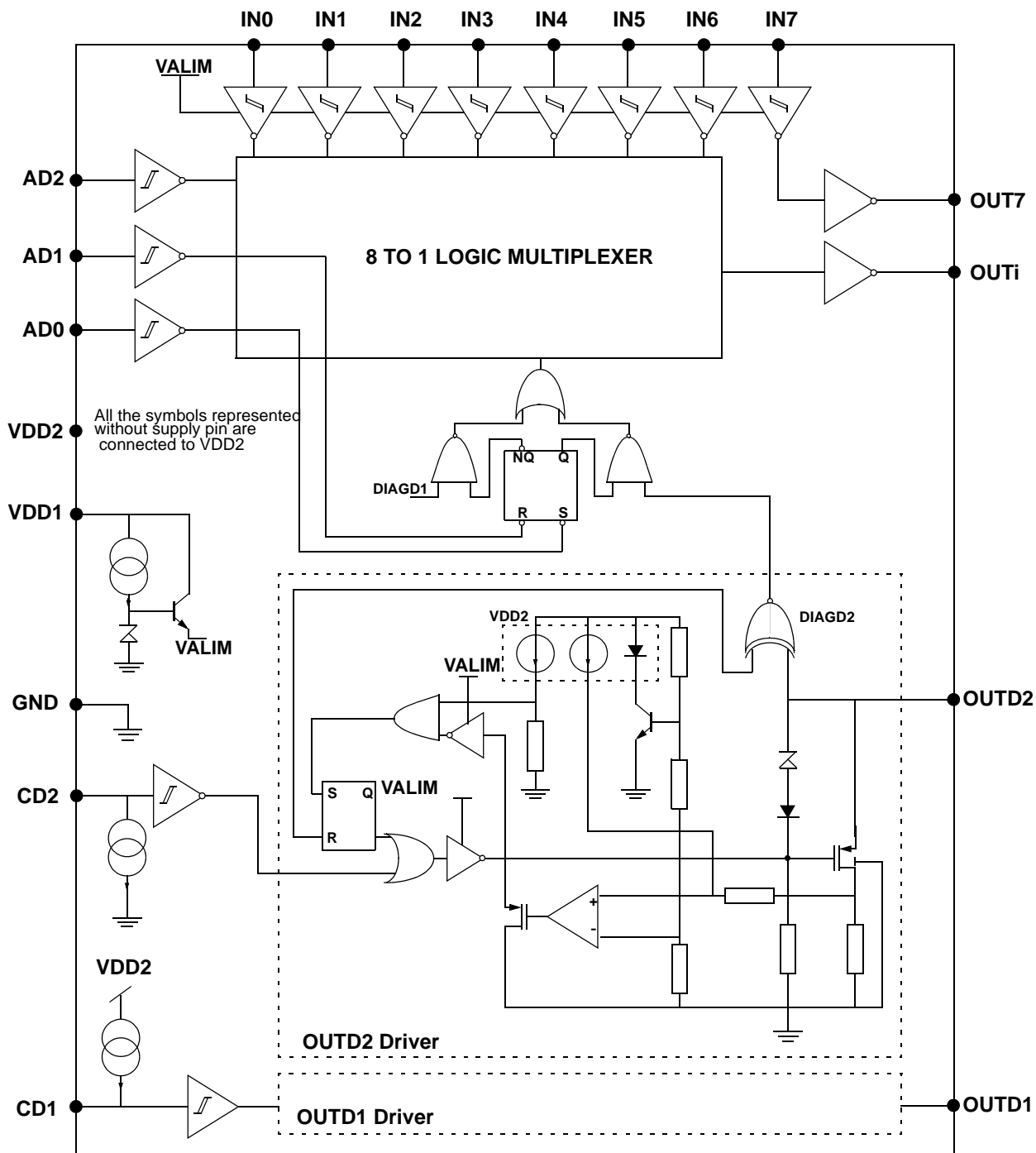


Figure 7. Contact Configuration



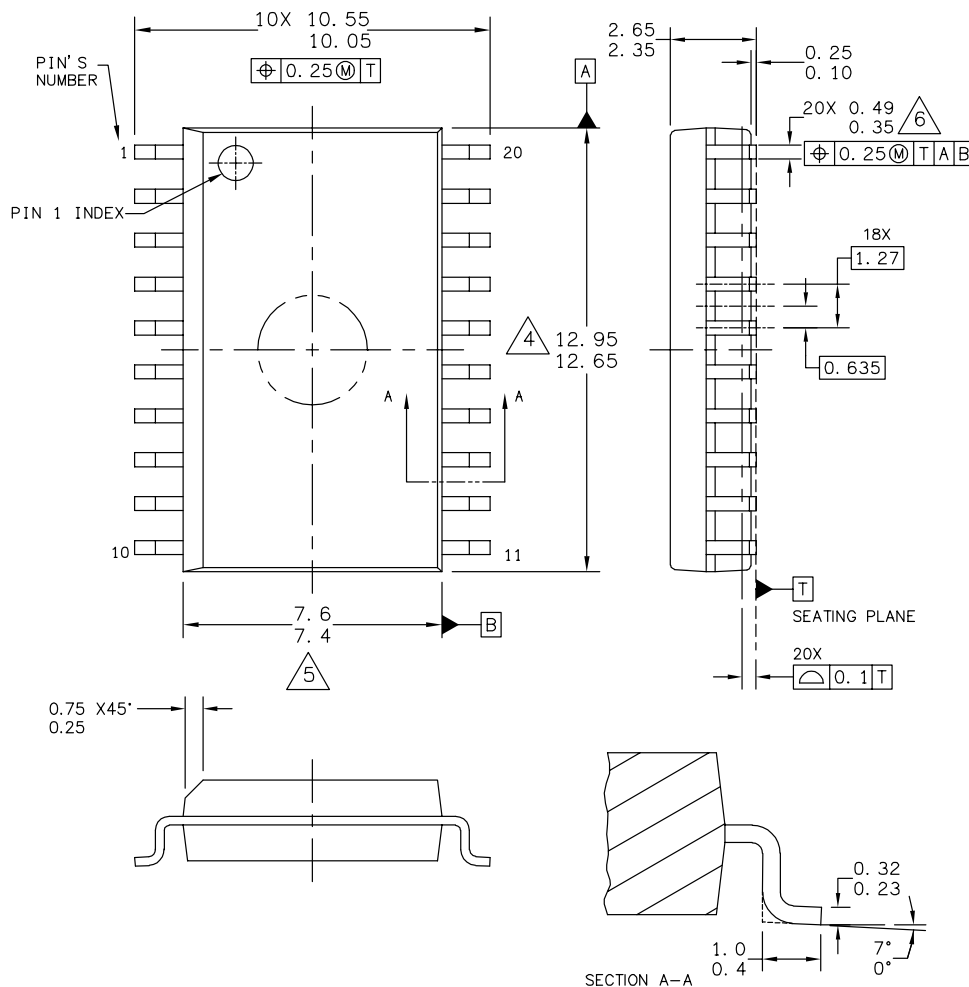
NOTE: The only difference between the low side driver 1 and 2 is the polarity of the command. Also, there is an integral pull-up at pin CD1, and an internal pull-down at pin CD2.

Figure 8. Electrical Schematic

# PACKAGE

## PACKAGE DIMENSIONS

For the most current package revision, visit [www.freescale.com](http://www.freescale.com) and perform a keyword search using the "98A" listed below.



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TITLE: 20LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42343B			REV: J	
	CASE NUMBER: 751D-07			23 MAR 2005	
	STANDARD: JEDEC MS-013AC				

**DW SUFFIX**  
**EG SUFFIX (PB-FREE)**  
 20-PIN  
 PLASTIC PACKAGE  
 98ASB42343B  
 REV. J

## REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	11/2006	<ul style="list-style-type: none"> <li>Converted to Freescale format with the current form and style</li> <li>Implemented Revision History page</li> <li>Updated Package Drawing 98ASB42343B to Rev. J</li> <li>Added EG Pb-FREE suffix</li> <li>Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from <a href="#">Maximum Ratings on page 4</a>. Added note with instructions to obtain this information from <a href="http://www.freescale.com">www.freescale.com</a>.</li> </ul>
5.0	2/2007	<ul style="list-style-type: none"> <li>Corrected <a href="#">Internal Block Diagram on page 2</a></li> <li>Restated Definition for OUT1 in <a href="#">33287 Pin Definitions on page 3</a></li> <li>Corrected value for <a href="#">Storage Temperature on page 4</a></li> <li>Corrected unit for <a href="#">Output Resistance (Extent Limit and <math>T_J \leq 130^{\circ}\text{C}</math>) on page 5</a></li> <li>Corrected <a href="#">Electrical Schematic on page 12</a></li> <li>Restated note 4 in <a href="#">Maximum Ratings on page 4</a>.</li> </ul>

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