

INTERNAL BLOCK DIAGRAM

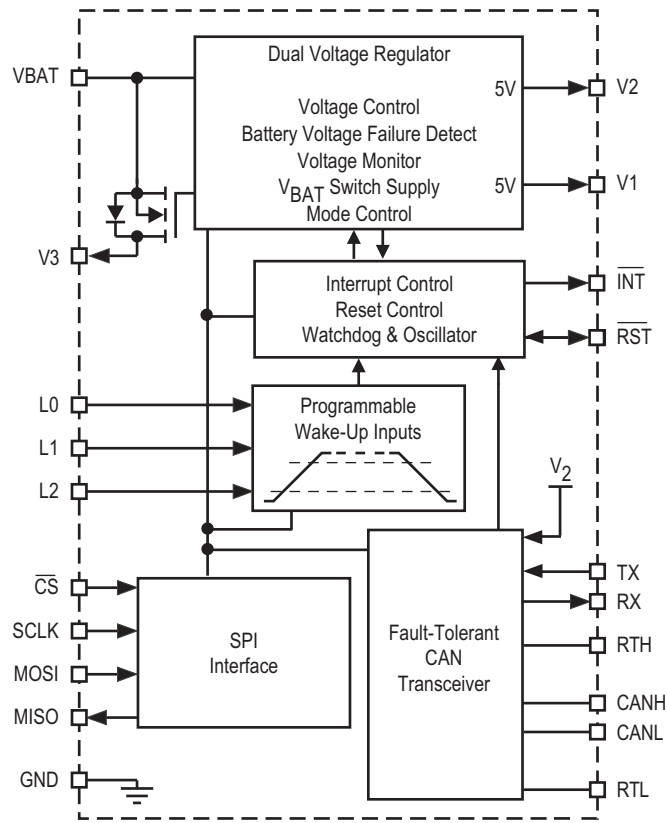
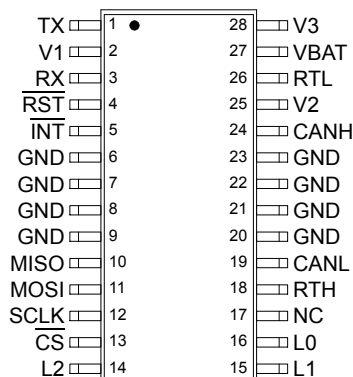


Figure 2. 33389 Simplified Internal Block Diagram

**Table 2. 33389 Pin Definitions: SOICW 28-Lead**

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 17](#).

Pin Number	Pin Name	Formal Name	Definition
1	TX	Transmitter Data	Transmitter input of the LS CAN interface
2	V1	Voltage Regulator One	This 5.0 V pin is a 3% low drop voltage regulator dedicated to the microcontroller supply.
3	RX	Receiver Data	Receiver output of the LS CAN interface
4	$\overline{\text{RST}}$	Reset	This is an Input/Output pin.
5	$\overline{\text{INT}}$	Interrupt	This output is asserted LOW when an enabled interrupt condition occurs.
6 -9 20 - 23	GND	Ground	These device ground pins are internally connected to the package lead frame to provide a 33389-to-PCB thermal path.
10	MISO	Master In/Slave Out	This pin is the tri-state output from the shift register.
11	MOSI	Master Out/Slave In	This pin is for the input of serial instruction data.
12	SCLK	System Clock	This pin clocks the internal shift registers.
13	$\overline{\text{CS}}$	Chip Select	This pin communicates with the system MCU and enables SPI communication.
14, 15, 16	L0: L2	Wake-up Input (L0: L2)	Input interfaces to external circuitry. Levels at these pins can be read by SPI and input can be used as programmable wake-up input in Sleep or Stop mode.
17	NC	No Connect	This pin does not connect.
18	RTH	Thermal Resistance High	Pin for the connection of the bus termination to CANH
19	CANL	CAN Low	CAN low input/output
24	CANH	CAN High	CAN high input/output
25	V2	Voltage Regulator Two	This 5.0 V pin is a low drop voltage regulator dedicated to the peripherals supply.
26	RTL	Thermal Resistance Low	Pin for the connection of the bus termination to CANL
27	VBAT	Voltage Battery	This pin is voltage supply from the battery.
28	V3	Voltage Regulator Three	This pin is a 10 Ω switch to V_{BAT} , used to supply external contacts or relays.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{BAT} , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^{\circ}\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (CONTINUED)					
V1 Output Current Limitation V1 _{NOM} - 100 mV	I1 _{MAX}	130	170	200	mA
V1 Overtemperature Shut OFF Threshold Junction Temperature	TV1H	160	—	190	$^{\circ}\text{C}$
V1 Pre-Warning Temperature Threshold Junction Temperature	TV1L	130	—	160	$^{\circ}\text{C}$
V1 Temperature Threshold Difference	TV1H-TV1L	20	—	40	$^{\circ}\text{C}$
V1 Reset Threshold on V1 5.5 V < V _{BAT} < 27 V	VR1	4.1	4.3	4.8	V
	(C Version)	V2 - 0.4	V1 - 0.28	V1 - 0.1	
	(D Version)				
V1 Reset Active V1 Range	V1R	1.0	VR1	—	V
V1 Reverse Current from V1 to V _{BAT} and GND V1 = 4.9 V, 0 < V _{BAT} < 4.9 V	IREV	—	—	1.0	mA
V2 Output Voltage 0 mA < I _{OUT} < 200 mA 5.5 V < V _{BAT} < 40 V	V2 _{NOM}	4.75	5.0	5.25	V
V2 Drop Voltage I _{OUT} = 200 mA ⁽⁷⁾	V2DROP	—	0.2	0.5	V
V2 Drop Voltage I _{OUT} = 20 mA ⁽⁷⁾	V2DROP	—	0.05	0.15	V
V2 Output Current Limitation V2 _{NOM} -100 mV	I1 _{MAX}	220	280	350	mA
V2 Threshold on V2 to Report V2 OFF V2 Nominal	VR2	4.1	4.55	4.75	V
VR2 Delay Time	VR2	20	—	70	μs
V2 Overtemperature Pre-Warning Threshold V2 Junction Temperature	TV2L	130	—	160	$^{\circ}\text{C}$
V2 Overtemperature Switch-OFF Threshold V2 Junction Temperature	TV2H	155	—	185	$^{\circ}\text{C}$
V2 Line Regulation 9.0 V < V _{BAT} < 16.5	V2 _{LR1}	-15	—	+15	mV
V2 Load Regulation 4.0 mA < I _{LOAD} < 200 mA	V2 _{LR2}	-75	—	+75	mV
V2 Line Ripple Rejection 100 Hz, 1.0 V _{PP} on V _{BAT} ⁽⁸⁾	V2 _{LRR}	30	55	—	dB

Notes

7. Measured when V1 has dropped 100mV below its nominal value
8. Guaranteed by design; however, it is not production tested

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{BAT} , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^{\circ}\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (CONTINUED)					
V2 Percentage Difference V2-V1 $V_{BAT} > 9.0$, $I_{V1} = 20$ mA, $I_{V2} = 40$ mA	$V2_{V2-V1}$	-3.0	—	3.0	%
V3 High Level Voltage Drop $I_{V3} = -50$ mA, 9.0 V $< V_{BAT} < 40$ V	$V3_{DROP}$	—	0.4	1.0	V
V3 High Level Voltage Drop $I_{V3} = -50$ mA, 6.0 V $< V_{BAT} < 9.0$ V	$V3_{DROP}$	—	—	1.5	V
V3 Leakage Output Limitation 5.5 V $< V_{BAT} < 27$ V	$I3_{LIM}$	100	150	250	mA
V3 Leakage Current $V3 = 0$ (V3 OFF)	$I3_{LEAK}$	—	—	15	μ A
V3 Overtemperature Detection Junction Temperature	T_{V3}	155	—	185	$^{\circ}\text{C}$
V3 Voltage with -30 mA (negative current for Relay Switch OFF) No Functional Error Allowed for $t \leq 100$ ms	V_{V3}	0.3	—	0.5	V
CAN Transceiver V2 for Forced Bus Stand-by Mode (Fail Safe)	VRC2	3.0	3.9	4.7	V
CANH/L Differential Receiver, Threshold Voltage	V_{CANTH}	-3.2	—	-2.5	V
CANH/L Differential Receiver, Dominant to Recessive Threshold (Bus Failures 1, 2, and 5)	$V_{CANDRTH}$	-3.2	—	-2.5	V
CANH Recessive Output Voltage TX = High, R(RTH) < 4.0 k	V_{CANH}	—	—	0.2	V
CANL Recessive Output Voltage TX = High, R(RTH) < 4.0 k	V_{CANL}	V2-0.2	—	—	V
CANH Output Voltage, Dominant TX = 0 V, BusNormal Mode, $I_{CANH} = -40$ mA	V_{CANH}	V2-1.4	—	—	V
CANL Output Voltage, Dominant TX = 0 V, Bus Normal Mode, $I_{CANL} = -40$ mA	V_{CANL}	—	—	1.4	V
CANH Output Current Limit ($V_{CANH} = 0.0$ V, TX = 0)	I_{CANH}	50	75	100	mA
CANL Output Current Limit ($V_{CANL} = 14$ V, TX = 0)	I_{CANL}	50	95	130	mA
Detection Threshold for Short Circuit to Battery Voltage Bus Normal Mode	$V_{CANH}-V_{CANL}$	7.3	7.9	8.9	V
Detection Threshold for Short Circuit to Battery Voltage Bus Stand-by Mode	V_{CANH}	$V_{BAT}/2+3$	—	$V_{BAT}/2+5$	V
CANH Output Current, Failure 3 Bus Stand-by Mode $V_{CANH} = 12$ V	I_{CANHF3}	—	5.0	10	μ A
CANL Output Current, Failure 4 Bus Stand-by Mode, $V_{CANL} = 0.0$ V, $V_{BAT} = 12$ V	I_{CANLF4}	—	0.0	2.0	μ A

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{BAT} , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^{\circ}\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (CONTINUED)					
CANL Wake-Up Voltage Threshold Bus Stand-by Mode	V_{WAKEL}	2.5	3.3	3.9	V
CANH Wake-Up Voltage Threshold Bus Stand-by Mode	V_{WAKEH}	1.2	2.0	2.7	V
Wake-Up Threshold Difference	$V_{WAKEL} - V_{WAKEH}$	0.2	—	—	V
CANH Single Ended Receiver Threshold Failures 4, 6, and 7	V_{CANH}	1.5	1.85	2.15	V
CANL Single Ended Receiver Threshold Failures 3 and 8	V_{CANL}	2.8	3.05	3.4	V
CANL Pull-Up Current Bus Normal Mode	I_{CANLPU}	45	75	90	μA
CANH Pull Down Current Bus Normal Mode	I_{CANLPD}	45	75	90	μA
Receiver Differential Input Impedance CANH/CANL	R_{DIFF}	100	—	180	$\text{k}\Omega$
Differential Receiver Common Mode Voltage Range	V_{COM}	-8.0	—	8.0	V
RTL to V2 Switch on Resistance $I_{OUT} < -10 \text{ mA}$, Bus Normal Operating Mode	R_{RTL}	10	25	70	Ω
RTL to Battery Switch Series Resistance Bus Stand-by Mode	R_{RTL}	8.0	12.5	20	$\text{k}\Omega$
RTH to Ground Switch on Resistance $I_{OUT} < 10 \text{ mA}$, All Modes	R_{RTH}	—	25	70	Ω
CONTROL INTERFACE					
High Level Input Voltage	V_{IH}	0.7 V1	—	V1 + 0.3 V	V
$\overline{\text{CS}}$ Threshold for SPI Wake-Up SBC in Sleep Mode, V1 < 1.5 V	V_{CSTH}	—	2.2	—	V
$\overline{\text{CS}}$ Filter Time for SPI Wake-Up SBC in Sleep Mode, V1 < 1.0 V	t_{CSFT}	—	—	3.0	μs
Low Level Input Voltage	V_{IL}	-0.3	—	0.3 V1	V
High Level Input Current on $\overline{\text{CS}}$ $V_I = 4.0 \text{ V}$	I_{CSH}	-100	—	-20	μA
Low Level Input Current on $\overline{\text{CS}}$ $V_I = 1.0 \text{ V}$	I_{CSL}	-100	—	-20	μA
TX High Level Input Current $V_I = 4.0 \text{ V}$	I_{TXH}	-200	-80	-25	μA
TX Low Level Input Current $V_I = 1.0 \text{ V}$	I_{TXL}	-800	-320	-100	μA
SI, SCLK Input Current $0 < V_{IN} < V1$	I_{SISLK}	-10	—	+10	μA

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_{\text{A}} \leq 125^\circ\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
MICROCONTROLLER INTERFACE (CONTINUED)					
Software Watchdog Timing 5 ⁽¹⁰⁾	t_{SW5}	44.8	51	58	ms
Software Watchdog Timing 6 ⁽¹⁰⁾	t_{SW6}	65	74	83	ms
Software Watchdog Timing 7 ⁽¹⁰⁾	t_{SW7}	88	100	112	ms
Software Watchdog Timing 8 ⁽¹⁰⁾	t_{SW8}	167	190	213	ms
Sleep Mode Oscillator Tolerance ⁽¹⁰⁾	SMOT	-30	—	+30	%
Cyclic Sense/FWU Timing 1 Sleep Mode ⁽¹⁰⁾	t_{CY1}	22.4	32	46.6	ms
Cyclic Sense/FWU Timing 2 Sleep Mode ⁽¹⁰⁾	t_{CY2}	44.8	64	83.2	ms
Cyclic Sense/FWU Timing 3 Sleep Mode ⁽¹⁰⁾	t_{CY3}	89.6	128	166.4	ms
Cyclic Sense/FWU Timing 4 Sleep Mode ⁽¹⁰⁾	t_{CY4}	179	256	333	ms
Cyclic Sense/FWU Timing 5 Sleep Mode ⁽¹⁰⁾	t_{CY5}	358	512	665	ms
Cyclic Sense/FWU Timing 6 Sleep Mode ⁽¹⁰⁾	t_{CY6}	717	1024	1331	ms
Cyclic Sense/FWU Timing 7 Sleep Mode ⁽¹⁰⁾	t_{CY7}	1434	2048	2662	ms
Cyclic Sense/FWU Timing 8 Sleep Mode ⁽¹⁰⁾	t_{CY8}	5734	8192	10650	ms
Ground Shift Threshold 1 ⁽¹¹⁾ CAN Transceiver Active in Two Wire Operation	GS1	-1.0	-0.7	-0.3	V
Ground Shift Threshold 2 ⁽¹¹⁾ CAN Transceiver Active in Two Wire Operation	GS2	-1.5	-1.2	-0.8	V
Ground Shift Threshold 3 ⁽¹¹⁾ CAN Transceiver Active in Two Wire Operation	GS3	-2.0	-1.7	-1.3	V
Ground Shift Threshold 4 ⁽¹¹⁾ CAN Transceiver Active in Two Wire Operation	GS4	-2.6	-2.2	-1.7	V
BUS TRANSMITTER					
AC Minimum Dominant Time for Wake-Up on CANL or CANH Bus Stand-by Mode, $V_{\text{BAT}} = 12\text{ V}$	t_{WAKE}	4.0	—	40	μs
AC Failure 3 Detection Time Bus Normal Mode	t_{AC3D}	10	—	60	μs
AC Failure 3 Recovery Time Bus Normal Mode	t_{AC3R}	10	—	60	μs
AC Failure 6 Detection Time Bus Normal Mode	t_{AC6D}	50	—	400	μs
AC Failure 6 Recovery Time Bus Normal Mode	t_{AC6R}	150	—	1000	μs
AC Failure 4, 7, and 8 Detection Time Bus Normal Mode	t_{AC478D}	0.75	—	4.0	ms

Notes

- Cyclic sense and forced wake-up timing accuracy are based on the Sleep mode oscillator tolerance.
- No overlap between two adjacent thresholds.

TIMING DIAGRAMS

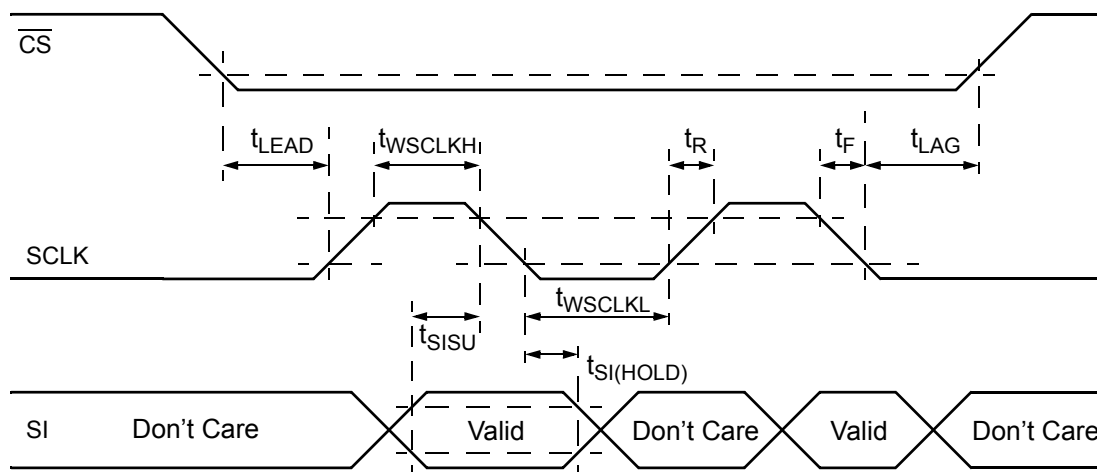


Figure 4. Input Timing Switch Characteristics

FUNCTIONAL DESCRIPTION

INTRODUCTION

The System Basis Chip (SBC) is an integrated circuit dedicated to car body applications. It includes three main blocks:

1. A dual voltage regulator
2. Reset, watchdog, wake-up inputs, cyclic wake-up

3. CAN low speed fault tolerant physical interface

Supplies

Two low drop regulators and one switch to V_{BAT} are provided to supply the **ECU** microcontroller or peripherals, with independent control and monitoring through SPI.

FUNCTIONAL PIN DESCRIPTION

TRANSMIT AND RECEIVE DATA (TX AND RX)

The RX and TX pins (receive data and transmit data pins, respectively) are connected to a microcontroller's CAN protocol handler. TX is an input and controls the CANH and CANL line state (dominant when TX is LOW, recessive when TX is HIGH). RX is an output and reports the bus state.

VOLTAGE REGULATOR ONE AND TWO (V1 AND V2)

The V1 pin is a 3% low drop voltage regulator dedicated to the microcontroller supply (nominal 5V supply).

The V2 pin is a low drop voltage regulator dedicated to the peripherals supply (nominal 5V supply).

RESET (\overline{RST})

The \overline{RST} (reset) pin is an input/output pin. The typical reset duration from SBC to microcontroller is 1ms. If longer times are required, an external capacitor can be used. SBC provides two \overline{RST} output pull-up currents. A typical 30 μ A pull up when V_{reset} is below 2.5V and a 300 μ A pull up when reset voltage is higher than 2.5V. \overline{RST} is also an input for the SBC. It means the MC33389 is forced to Normal Request mode after \overline{RST} is released by the microcontroller

INTERRUPT (\overline{INT})

The Interrupt pin \overline{INT} is an output that is set LOW when an interrupt occurs. \overline{INT} is enabled using the Interrupt Register (INTR). When an interrupt occurs, \overline{INT} stays LOW until the interrupt source is cleared.

\overline{INT} output also reports a wake-up event.

GROUND (GND)

This pin is the ground of the integrated circuit.

MASTER IN/ SLAVE OUT (MISO)

MISO is the Master In Slave Out pin of the serial peripheral interface. Data is sent from the SBC to the microcontroller through the MISO pin.

MASTER OUT/ SLAVE IN (MOSI)

MOSI is the Master Out Slave In pin of the serial peripheral interface. Control data from a microcontroller is received through this pin.

SYSTEM CLOCK (SCLK)

This pin clocks the internal shift registers for SPI communication.

CHIP SELECT (\overline{CS})

\overline{CS} is the Chip Select pin of the serial peripheral interface (SPI). When this pin is LOW, the SPI port of the device is selected.

LEVEL 0-2 INPUTS (L0: L2)

The L0: L2 pins can be connected to contact switches or the output of other ICs for external inputs. The input states can be read by the SPI. These inputs can be used as wake-up events for the SBC.

NO CONNECT (NC)

No pin connection.

TERMINATION RESISTANCE (HIGH AND LOW?) (RTH AND RTL)

External CAN bus high and low termination resistance pins are connected to these pins.

CAN HIGH AND CAN LOW OUTPUTS (CANH AND CANL)

The CAN High and CAN Low pins are the interfaces to the CAN bus lines. They are controlled by TX input level, and the state of CANH and CANL is reported through RX output.

VOLTAGE BATTERY (VBAT)

This pin is the voltage supply from the battery.

VOLTAGE REGULATOR THREE (V3)

This pin is a 10 Ω switch to VBAT, which is used to supply external contacts or relays.

FUNCTIONAL DEVICE OPERATION

Voltage Regulator V1

V1 is a 5.0 V, three percent low drop voltage regulator dedicated to the microcontroller supply. It can deliver up to 100 mA. It is totally protected against short-to-ground (current limitation) and over temperature. V1 is active in Normal Request, Normal, and Stand-by modes.

No forward parasitic diode exists from V1 to V_{BAT} . This means if V_{BAT} voltage drops below V1, high current flowing from V1 to V_{BAT} will not discharge the capacitor connected to V1. Its stored energy will only be used to supply the microcontroller and gives time to save all relevant data.

- Under Voltage Reset—V1 is monitored for under voltage (power-up, power down) and a reset is provided at \overline{RST} output for 1 ms. This ensures proper initialization of the microcontroller at power-on or after supply is lost. Furthermore, a flag is set in the Reset Source Register (RSR) and can be read via the SPI.
- Over Temperature Protection—V1 internal ballast transistor is monitored for over temperature. Two detection thresholds are provided. A pre-warning threshold at 145°C and a shut-off threshold at 175°C. Once the first threshold is reached, a flag is set in the Over Temperature Status Register (OTSR). A maskable interrupt can be sent to the microcontroller. Once the second threshold is reached, a flag is set in the OTSR, a maskable interrupt is sent to the microcontroller and V1 is switched OFF.

Once the junction temperature is back to the pre-warning threshold, V1 regulator will be automatically switched ON.

Table 6. V1 Control

Conditions for V1 ON	Conditions for V1 OFF
Normal Request Mode (at V1 Power ON)	Sleep Mode (via SPI)
Normal Mode (via SPI)	Shut-Off Temperature Threshold Reached
Stand-by Mode (via SPI)	No V_{BAT} Power Supply (cold start)
V1 Below Pre-Warning Temperature Threshold	Emergency Mode
During Rest	—

Note: Current capability of V1, V2 and V3 depends upon the thermal management. Over temperature shutdown might be reached and lead to turn OFF of V1, V2, and V3 for output current below their maximum current capability.

Voltage Regulator V2

V2 is a 5.0 V low drop voltage regulator dedicated to peripherals supply. It can deliver up to 200 mA and is protected against short to ground (current limitation) and over temperature. V2 is active in Normal mode.

- Under Voltage Detection—V2 is monitored for under voltage and a flag is set in the Voltage Supply Status Register (VSSR).
- Over Temperature Protection—V2 internal ballast transistor is monitored for overtemperature. Two detection thresholds are provided. A pre-warning threshold at 140°C and a shut-off threshold at 165°C. Once the first threshold is reached, a flag is set in the readable OTSR register. A maskable interrupt can be sent to microcontroller.

Once the second threshold is reached, a flag is set in the OTSR register, V2 is switched OFF. It can only be switched on again via the SPI.

Table 7. V2 Control

Conditions for V2 ON	Conditions for V2 OFF
Normal Mode (via SPI) and V2 Below Shut-Off Temperature Threshold	Sleep, Stand-by, Normal Request, or Emergency Modes (via SPI)
—	Shut-Off Temperature Threshold Reached
—	V1 Disabled (for any reason)

Switch V3

V3 is a 10 Ω switch to V_{BAT} . It can be used to supply external contacts or relays. A great flexibility is given for the different possible ways for its control. It is protected against short to ground (current limitation).

- Over Temperature Protection—V3 output transistor is monitored for over temperature. Once the threshold is reached, a flag is set in the VSSR register, V3 is switched OFF. It will be automatically switched ON once the junction temperature is back to the pre-warning threshold.

Table 8. V3 Control

Conditions For V3 ON	Conditions For V3 OFF
Permanently in Normal Mode if Configured via SPI	Permanently in Normal Mode if Configured
Permanently in Stand-by Mode if Configured via SPI	Normal Request Mode
In Sleep Mode, During Enable Time of Cyclic Sense if Configured	Permanently in Stand-by Mode if Configured
—	Permanently in Sleep Mode if Configured

speed applications up to 125 kBit/s in passenger cars. It provides differential transmission capability, but will switch in error condition to single wire transmitter and/or receiver.

The rise and fall slopes are limited to reduce radio frequency interference (RFI). This provides use of an unshielded twisted pair or a parallel pair of wires for the bus. It supports transmission capability on either bus wire if one of the bus wire is corrupted. The logic failure detection automatically selects a suitable transmission mode.

In a normal operation (no wiring failures), the differential bus state is the output to RX. The differential receiver inputs are connected to CANH and CANL through integrated filters. The filtered inputs signals are also used for the single wire receivers. The CANH and CANL receivers have threshold voltages, assuring maximum noise margin in single wire modes. In the RX Only mode, the transmitter is disabled; however, the receive part of the transceiver remains active. In this mode, RX reports bus and TX activity ($RX = TX$ or Bus dominant). Failure detection and management is the same as the Bus Normal mode.

Failure Detector

The failure detector is active in RXTX and RX Only operation modes. The detector recognizes the following single bus failures and switches to an appropriate mode.

1. CANH wire interrupted
2. CANL wire interrupted or shorted to 5.0 V
3. CANH short-circuit to battery
4. CANL short-circuit to ground
5. CANH short-circuit to ground
6. CANL short-circuit to battery
7. CANL mutually shorted to CANH
8. CANH to V2 (5.0 V)

Note: Shorts-circuit failures are detected for 0 to 50 Ω shorts.

The differential receiver (CANH-CANL) threshold is set at -2.8 V, this assures a proper reception in the normal operating modes. In case of failures 1, 2, and 5 the on-going message is not destroyed due to noise margin.

Failures 3 and 6 are detected by comparators respectively connected to CANH and CANL. If the comparator threshold is exceeded for a certain time (T_{AC3D} , T_{AC6D}), the reception is switched to single wire mode. This time is required to avoid false triggering by external RF fields. Recovery from these failures is detected automatically after a certain (T_{AC3R} , T_{AC6R}) time-out (filtering).

Failures 4 and 7 initially result in a permanent dominant level at RX. After a time-out, the CANL driver and the RTL pins are switched OFF. Only a weak pull-up at CANL remains. Reception continues by switching to Single Wire

mode through CANH. When Failures 4 or 7 are removed, the recessive bus levels are restored. If the differential voltage remains below the recessive threshold for a certain (T_{AC478R}) time, reception and transmission switch back to the Differential mode.

If any of the eight wiring failure occurs, a flag is set in the TESRH and TESRL Status registers. Eight different types of errors are distinguished out of these eight errors. They are separately stored in these register. Please refer to the [Tables 35 and 36](#). A maskable interrupt is sent to the microcontroller. On error recovery, the corresponding flag is reset after read-out operation.

During all single wire transmissions, the EMC performance (both immunity and emission) is worse than in the Differential mode. Integrated receiver filters suppress any high frequency noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and high frequency suppression. In the Single Wire mode, low frequency noise can not be distinguished from the expected signal.

In the event of a permanent dominant TX state (for more than 2.0 ms) the output drivers are disabled. That assures the operation of the complete system in case of a permanent dominant TX state of one control unit. The CAN interface of a defective ECU, which has TX permanently low, will automatically be set to the receive only mode and therefore will not lock the complete CAN bus.

Protection

A current limiting circuit protects the transmitter output stages against short-circuit to positive and negative battery voltage. If the junction temperature exceeds a maximum value, the transmitter output stages are disabled. Because the transmitter is responsible for a part of the power dissipation, this results in a reduced power dissipation resulting in a lower chip temperature. All other parts of the transceiver will remain operating. The CANH and CANL inputs are protected against electrical transients, and may occur in an automotive environment.

Thermal Management

The 33389 is proposed in two different packages:

1. HSOP-20 for high power applications
2. SO28WB with eight pins to the lead frame for medium power applications

HSOP20 Package

For such a package, the heat flow is mainly vertical and each heat source (dissipating element) can be seen as an independent thermal resistance to the Heatsink. The thermal network can be roughly depicted in [Figure 6](#).

OPERATIONAL MODES

CAN Transceiver Modes

The CAN transceiver has its own functioning modes: RXTX mode, Term V_{BAT} /Term V_{CC} mode, and RX Only mode. They are controlled by the Transceiver Control/Status Register (TCR).

- RXTX mode—Full transmitting and receiving capabilities are enabled. Full failure detection is enabled.

Note: Standard/RXTX and Extended/RXTX are equivalent.

- RX Only mode—The transmitter is disabled but the receive portion of the transceiver remains active. In this mode, RX reports bus and TX activity ($\overline{RX} = \overline{TX}$ or Bus dominant).

Note: Standard/RX Only and Extended/RX Only are equivalent.

- Bus Stand-by mode—Is the Low Power mode for the CAN transceiver. The driver and receivers are disabled. Wake-up capability on both bus lines as well as Failure 3, 4, 7, and 8 detection are enabled. RTL termination is set to V_{BAT} in the Bus Stand-by mode.

Low Power Modes

The transceiver provides a Low Power mode, entered and exited by a SPI command. This is the Bus Stand-by mode having the lowest power consumption for the transceiver. CANL is biased to the battery voltage via the RTL output and the pull-up current source on CANL and pull down current source on CANH are disabled. Wake-up requests are recognized by the transceiver when a dominant state is detected on either bus wake-up lines. On a Bus wake-up request, the SBC will activate the \overline{INT} output or, if it is in the Sleep mode, switch to the Normal Request mode. This event is stored in the Wake-Up Input Status Register (WUISR).

To prevent a false wake-up resulting from transients or (RF) fields, wake-up threshold levels have to be maintained for a certain time. While in the Transceiver Low Power mode, failure detection circuit remains partly active preventing increased power consumption in cases of error 3, 4, 7, and 8.

Power-On

After the VBAT supply is switched ON, the SBC is in Normal Request mode. Bus Stand-by is the corresponding mode for the CAN transceiver.

The CAN transceiver is supplied by V2. As long as V2 is below its under voltage threshold, the transceiver is forced to Bus Stand-by mode (fail safe property).

SBC MODES

Global Power Save Concept

The SBC minimizes power consumption of the ECU. Several operating modes are available to go to low power

consumption when the full activity is not required. Several possibilities are provided to wake-up the ECU. This permits peripherals or the microcontroller to be switched OFF when no activity on the ECU is required.

Two switchable independent supply voltages (V1 and V2) are provided for optimum ECU power management.

Generalities

The SBC can be operated in four modes:

1. Sleep
2. Stand-by
3. Normal
4. Emergency

After reset, the 33389 is automatically initialized to the temporary mode, Normal Request, while waiting for microcontroller configuration.

Reset Mode

This mode is entered after SBC power-up, or if an incorrect software watchdog trigger occurs. The minimum duration for reset mode is 1.0 ms typical, and unless there is a V1 failure condition, the SBC enters the Normal Request mode after reset.

In the case of a V1 failure condition leading to V1 low (ex: short to ground), the SBC switches to the Reset mode. If V1 is still below the reset threshold after 100 ms, the behavior depends upon the device version A or C:

- C version: The 33389CDW and the 33389CDH will remain in the reset mode.
- D version: The 33389DDW and the 33389DEG will remain in the reset mode. Note that the reset mode threshold for the D version is slightly higher than the C version.

Normal Request Mode

The Normal Request mode is the Default mode after 33389 reset. V1 is active, while V2 and V3 are passive. The SBC is not configured. The default values are set in the registers. The SBC awaits data configuration via the SPI.

If no SPI data is received 75 ms after the Reset is released, the SBC switches itself into the Sleep mode.

The software timing word (in SWCR) provides the data the SBC must receive to consider when the microcontroller begins the configuration sequence. Once received, this software timing word, and the watchdog timer, become active. Any other control data can then be sent from the microcontroller to SBC.

The watchdog is not active in the Normal Request mode before the software timing word is programmed into the SBC. In this mode, neither V2 nor the CAN transmitter are active.

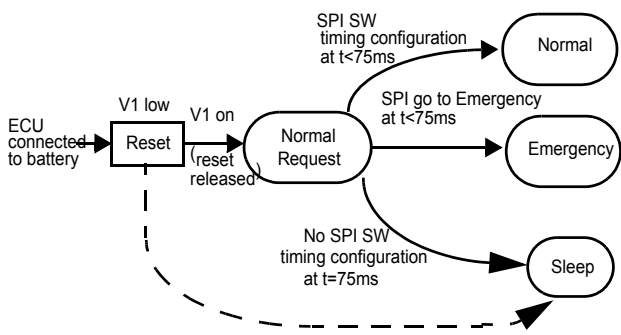


Figure 8. Typical Behavior at Power-On

Note: In the Normal Request mode, if a SPI command is received before the software timing configuration (SWCR register), it will not be taken into account by the SBC (except for the go-to Emergency mode).

Correspondence Between SBC and CAN Transceiver Modes

Table 14 provides different possible CAN transceiver modes versus SBC modes.

Table 14. CAN Modes vs. SBC Modes

When SBC Is In The Following Mode	CAN Transceiver Can Be In
Reset Condition	Bus Stand-by Mode
Normal Request	Bus Stand-by Mode
Normal	RXTX or RXOnly or BusStand-by
Stand-by	Bus Stand-by
Sleep	Bus Stand-by
Emergency	Bus Stand-by
Normal and V2 OFF (over load) In case V2 is turned OFF either by SPI command (Stand-by mode) or by the SBC itself due to V2 over load condition (V2 short to ground or V2 over temperature) the CAN is automatically set into the Bus Stand-by mode and does not return to TXRX mode automatically when V2 is back to 5.0 V. The CAN must be re configured to TXRX or RX Only mode after a V2 turn OFF	Bus Stand-by

Watchdog

The software window watchdog function monitors the microcontroller operation in the Normal and Stand-by modes.

The window watchdog timing is derived from the SBC clock. The desired watchdog timing must be first transmitted during the SBC configuration, in the Normal Request mode, via SPI to SWCR. It can also be changed later on. Selectable watchdog timings are 5.0 ms, 10 ms, 20 ms, 33 ms, 50 ms, 75 ms, 100 ms and 200 ms. These timings correspond to the full disable window plus full enable window.

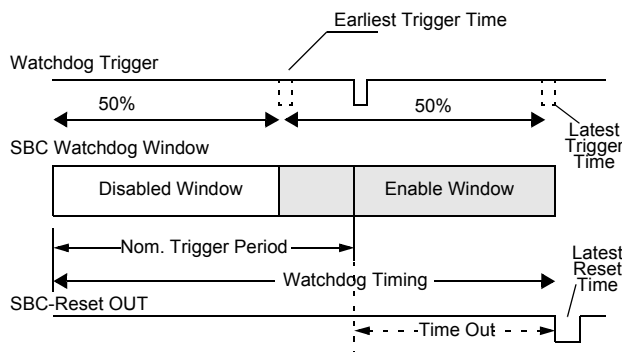


Figure 9. Window Watchdog Timing

As soon as the watchdog trigger is received in the Enable Window, the internal counter is reset and begins a new disable window. The SBC triggers the watchdog word at CS low-to-high transition. Any watchdog trigger outside the Enable Window leads to an SBC reset.

- Normal and Stand-by Modes— The SBC get the watchdog word from the microcontroller via SPI in the Normal mode. In case of a trigger time failure (no trigger or trigger outside the Enable Window) the SBC reset is switched to active.
- Normal Request, Sleep, and Emergency Mode— Watchdog is not active in these modes.

WAKE-UP CAPABILITIES

Several wake-up capabilities are available.

Forced Wake-Up

The forced wake-up is enabled and disabled by SPI in the V3 register. It is used to automatically wake-up the system by supplying V1 with proper reset in the Sleep mode. This corresponds to jump into the Normal Request mode. If the SBC is not properly configured within 75 ms, it switches back to the Sleep mode until the next wake-up. If both Cyclic Sense and Forced Wake-Up are enabled by the SPI while in the Sleep mode, only Cyclic Sense is active.

The period of Forced Wake-Up are 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, 1024 ms, 2048 ms, and 8192 ms chosen by SPI in the Cyclic Timing Control Register (CYTCR).

Wake-Up Inputs (Local Wake-Up)/Cyclic Sense

SBC provides three wake-up inputs to monitor external events such as closing/opening of switches. The wake-up feature is available in Normal, Stand-by, and Sleep modes.

The switches can be directly connected to V_{BAT} or to $V3$. The SBC must be properly configured by setting the bit $WI2V3$ in the $V3$ register. In this case, wake-ups are only detected when $V3$ is ON. It can take advantage of the $V3$ Cyclic Sense feature. If both Cyclic Sense and Forced Wake-Up are enabled by the SPI in the Sleep mode, only Cyclic Sense will be active.

Options for Wake Input

Different conditions for wake-up can be chosen for wake-up input pins (via SPI in the Wake-Up Input Control Register (WUICR)).

- No Wake-Up—Wake-ups are not detected whatever occurs on wake-up inputs.
- High-State—If the input pin voltage is above the detection threshold during more than a 20 μs filter time, a wake-up is detected. A flag is set in the WUISR.
- Low-State—If the input pin voltage is below the detection threshold during more than a 20 μs filter time, a wake-up is detected. A flag is set in the WUISR.
- Change of state—Each change of the wake-up input pin is considered as a wake-up if it lasts more than a 20 μs filter time. The first reference state (no wake-up) is the wake-up input state when the SBC is programmed to this option. A flag is set in the WUISR.
- Multiple Sampling Events—When wake-up inputs are used with $V3$ in Cyclic Sense in the Sleep mode.

For positive edge sensitivity, two samples Low followed by two samples High are necessary to validate the wake-up condition.

For negative edge sensitivity, two samples High followed by two samples Low are necessary to validate the wake-up condition.

For both edge sensitivity, two samples at a given state followed by two samples in the opposite state are necessary to validate the wake-up condition.

Wake-Up Inputs with Cyclic Sense

Connecting the external switches to $V3$ allows power saving because $V3$ can be programmed to be active, passive, or cyclic (Cyclic Sense). This provides great flexibility reducing total power consumption while allowing full wake-up capabilities. Cyclic Sense is available only in the Sleep mode.

The period of the Cyclic Sense can be chosen out of eight different timings: 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, 1024 ms, 2048 ms, and 8192 ms programmable via SPI in the CYTCR register. Once activated, $V3$ remains ON during 400 μs . The wake-up inputs states are sampled at 300 μs .

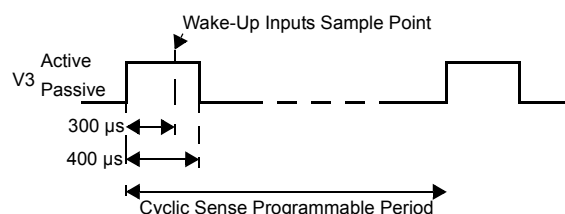


Figure 10. V3 Timing

Note: In Sleep mode, the Cyclic Sense feature 'EXCLUSIVE OR' the forced Wake-Up is chosen (not both).

Cyclic Sense connected to wake-up inputs. Example: with wake-up input L1 sensitivity to Low state and timing = 80 ms

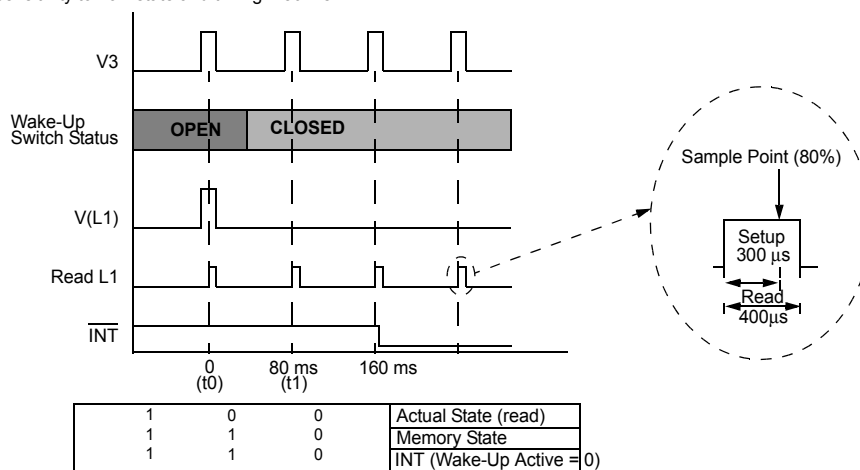


Figure 11. Cyclic Sense Timing

Wake-Up Inputs with Permanent Sense

Wake-up detection can also be accomplished in a permanent way in Normal and Stand-by modes. If the contacts are connected to $V3$, wake-ups are only detected if $V3$ is ON.

Wake-ups are also detected in a permanent way in the Sleep mode if the contacts are directly connected to V_{BAT} (if they are connected to $V3$, only Cyclic Sense is available in Sleep mode).

Sleep Mode Activation

Once in the Sleep mode, the SBC turns the V1 and V2 regulator OFF. Thus the microcontroller can not run any mode.

In order to have the microcontroller run again, the SBC should enable and turn ON V1. This is achieved by an SBC wake-up event.

Several options are available to wake-up the SBC and the application and have the microcontroller in Run mode.

Some wake-ups are selectable; some are always active in Sleep mode:

- Wake-up from CAN interface and wake-up from SPI (\overline{CS}) are always active.
- Wake-up from L0, L1, and L2 inputs, with and without cyclic sense and the forced wake-up (FWU) are selectable. The selection must be done while the SBC is in Normal or Stand-by mode, and prior to enter Sleep mode.

General Condition to Enter Sleep Mode

All previous wake-up conditions must be cleared, assuring the SBC enters the Sleep mode, and Write operations into the MCR and MCVR. To clear a wake-up condition requires reading the appropriate register.

Once the SBC has powered-up from zero (battery power-up or cold start), the following registers must be read:

- WUICR—possible wake-up event report from CAN bus
- RSR—report a V1 under voltage
- VSSR—reports a V_{BAT} fail flag

Once these read operations are completed, the wake-up conditions, or flags are reset.

The VBSR0 bit in the VSSR can be used to determine if the SBC has experienced a loss of battery voltage.

Once the SBC is awakened from *Sleep mode* the following registers indicate the wake-up source. They must be cleared to allow the SBC to enter Sleep mode again:

- WUICR—wake-up event report for CAN or SPI buses
- WUISR—wake-up event report for the L0, L1, and L2 inputs
- RSR—report a V1 under voltage
- VSSR—reports a V_{BAT} fail flag
- etc.

The ensuing paragraphs describe the write operation to be accomplished for the several Sleep modes and Wake-up control options.

In addition to FWU, cyclic sense and direct wake-up, the CAN and SPI wake will always be activated.

Sleep Mode with CAN and SPI Wake-Up

To enter the Sleep mode and activate the only CAN or SPI wake-up, there is no dedicated wake-up condition to be

completed. The SBC has CAN and SPI wake-up sources always active in the Sleep mode. To enter the Sleep mode in this case, while the SBC is in Normal or Stand-by mode:

- Write to V3R—data 0000 (this clears the W12V3 bit, is set to 1 after reset)
- Write to MCR—data SLEEP (100)
- Write to MCVR—data SLEEP (100)

The SBC then enters the Sleep mode.

Sleep Mode Enter with Forced Wake-Up

To enter the Sleep mode and activate the forced wake-up, write to the following registers:

- Write to V3R (data 0100) this set the FWU bit to 1
- Write the desired wake-up time to CYTCR. (This sets the time the SBC will stay in the Sleep mode).
- Write to MCR—data SLEEP (100)
- Write to MCVR—data SLEEP (100)

The SBC then enters the Sleep mode. It will wake-up after the time period is selected in the CYTCR.

Sleep Mode Enter with Cyclic Sense

To enter the Sleep mode and activate the cyclic sense wake-up the following registers must be written:

- Write to V3R (data 1010) this sets the V12V3 and CYS bits to 1
- Write to CYTCR the desired cyclic sense period. (This sets the time the SBC will wait in the Sleep mode to turn on V3 and sense the LX inputs)
- Write to WUICR bits 0 and 1 to select the edge sensitivity for the LX inputs
- Write to MCR—data SLEEP (100)
- Write to MCVR—data SLEEP (100)

The SBC then enters the Sleep mode. It will periodically turn on V3 and while V3 is on, sample the level of the Ls inputs.

If any of the 3 LX inputs is in the correct state for two consecutive samples, SBC will wake-up. If not, it will stay in the Sleep mode. Refer to device description for detail.

Sleep Mode Enter With Direct LX Input Wake-Up

To enter the Sleep mode and activate the direct wake-up from the LX inputs, the following registers must be written:

- Write to V3R (data 0000) this clear V12V3 bit
- Write to WUICR bits 0 and 1 to select the edge sensitivity for the LX inputs
- Write to MCR—data SLEEP (100)
- Write to MCVR—data SLEEP (100)

The SBC then enters the Sleep mode. It will wake-up as soon as any of the LX input read the correct state.

entered the MOSI pin starting with Bit15, followed by Bit14, Bit13, etc., to Bit0. For each fall of the SCLK signal, with CS held in a logic low state, a data bit is loaded into the shift register per the tidbit MOSI state. The shift register is full after sixteen bits of information have been entered.

MISO PIN

The serial output (MISO) pin is the tri-stateable output from the shift register. The MISO pin remains in a high impedance state until the CS pin goes to a logic low state. The MISO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. The MOSI/MISO shifting of data follows a first-in-first-out protocol with both input and output words transferring the MSB first.

Module Address Map, the module address map is shown in table.

Table 16. Module Address Map

Address	Register	Register Name
\$000	Mode Control Register	MCR
\$003	Mode Control Validation RegisterMCVR	MCVR
\$005	V3 control register	V3R
\$006	Cyclic timing control register	CYTCR
\$009	Software watchdog control register	SWCR
\$00A	Ground shift level register	GSLR
\$00C	Wake-up input control register	WUICR
\$00F	Wake-up input status register	WUISR
\$011	Wake up input real time information	WUIRTI
\$012	Overtemperature status regist	OTSR
\$014	Transceiver error status register for CANH	TESRH
\$017	Transceiver error status register for CANL	TESRL
\$018	Reset source register	RSR
\$01B	Voltage supply status regist	VSSR
\$01D	Interrupt mask control register 1	IMR1
\$01E	Interrupt mask control register 2	IMR2
\$021	Interrupt source register 1	ISR1
\$022	Interrupt source register 2	ISR2

Table 16. Module Address Map

Address	Register	Register Name
\$024	Transceiver control register	TCR

Control and Status Reporting of the 33389

The MCU is responsible for the control data transfer to the 33389, while the 33389 reports its status to the MCU. Major data for control and status reporting are summarized here:

- SPI initialization during start up
- 33389 control during operation
- Watchdog triggering
- Reading status registers of the 33389

Control Data

The control data are transferred from the MCU to the 33389. A control word includes an address of a control register and the appropriate data (see Figure 17). Basically, the following data will be transferred. Please see SPI Registers Descriptions on page 34.

- 33389 mode control
- Supply control
- Forced wake-up timing
- Cyclic sense control
- Watchdog control
- Transceiver control

Status Data

The status data are transmitted from the 33389 to the MCU. After receiving a valid register address from the MCU, the 33389 returns the appropriate status. Some of the major status data are listed below:

- Current operation mode status
- Wake-up sources
- Reset status
- Error status
- Over temperature status
- Transceiver status

Data Transfer

The data to and from the 33389 are transferred in form of two bytes. The structure of the transferred information is the same as for control and status reporting. The address field A5 to A0 (Bit 15 to Bit 10) contains the address of a control or status register in the 33389. RW (Bit 9 and Bit 8) contains the read/write flag for the data field. The parity field is located at P3 to P0 (Bit 7 to Bit 4). The data field D3 to D0 (Bit 3 to Bit 0) is part of the two-byte data word. Please see Figure 17.

Table 18. Mode Control Validating Register (MCVR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MCVR \$003	R						MSVR2	MSVR1	MSVR0
	W						MCR2	MCR1	MCR0
RESET		—	—	—	—	—	0	0	0

Table 19. MCR and MCVR Bit Definition

MC(V)R2	MC(V)R1	MC(V)R0	—	MSR2	MSR1	MSR0
Automatically Entered After Reset			Normal Request	0	0	0
0	0	1	Normal	0	0	1
0	1	0	Stand-by	0	1	0
1	0	0	Sleep	1	0	0
1	1	1	Emergency	1	1	1

This register configures the state of V3 high-side switch in Normal and Stand-by modes, and the V3 operation and the Forced wake-up or the cyclic sense option for the sleep mode operation.

Table 20. V3 Control Register (V3R)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
V3R \$005	R					WI2V3	FWU	CYS	V3R0
	W								
RESET		—	—	—	—	1	0	0	0

Table 21. V3R Bit Definition

WI2V3	FWU	CYS	V3R0	—	Comments
x	0	0	0	V3 OFF	Only in Normal and Stand-by Mode Available
x	0	0	1	V3 ON	
x	x	1	x	Cyclic Sense ON	—
x	1	0	x	Forced Wake-Up ON	Only in Sleep Mode Available
1	x	x	x	Wake-Up Inputs Linked to V3	

In low power modes, cyclic sense has priority. A reset of the register occurs when $\overline{RST} = \text{low}$.

Table 22. Cyclic Timing Control Register (CYTCR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CYTCR \$006	R						CYTCR2	CYTCR1	CYTCR0
	W								
RESET		—	—	—	—	—	0	0	0

This register is used to select the cyclic sense or force wake-up timing.

Table 23. CYTCR Bit Definition

CYTCR2	CYTCR1	CYTCR0	Comments	t(ms) Typical
0	0	0	Timer ON, t1 (Default)	32
0	0	1	Timer ON, t2	64
0	1	0	Timer ON, t3	128
0	1	1	Timer ON, t4	256
1	0	0	Timer ON, t5	512
1	0	1	Timer ON, t6	1024
1	1	0	Timer ON, t7	2048
1	1	1	Timer ON, t8	8192

Note: A reset of the register occurs when $\overline{\text{RST}} = \text{Low}$.

Table 24. Software Watchdog Control Register (SWCR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCR \$009	R						SWCR2	SWCR1	SWCR0
	W								
RESET		—	—	—	—	—	0	0	0

This register is used to select the window watchdog time period. Open window of the selected period is only the second half of the selected period.

Table 25. SWCR Bit Definition

SWCR2	SWCR1	SWCR0	Comments	t(ms) Typical
0	0	0	Timer ON, t1 (Default)	5
0	0	1	Timer ON, t2	10
0	1	0	Timer ON, t3	20
0	1	1	Timer ON, t4	33
1	0	0	Timer ON, t5	50
1	0	1	Timer ON, t6	75
1	1	0	Timer ON, t7	100
1	1	1	Timer ON, t8	200

Note: The software watchdog is only running in Normal and Stand-by modes. A reset of this register occurs when $\overline{\text{RST}} = \text{Low}$.

Table 26. Ground Shift Level Register (GSLR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GSLR \$00A	R					TXDOM	SHIFT	GSLR1	GSLR0
	W								
RESET		—	—	—	—	—	0	0	0

This register is used to monitor the ground shift of the vehicle network.

Table 27. GSLR Bit Definition

GSLR1	GSLR0	Typical Ground Shift Level
0	0	0.7 V
0	1	-1.2 V
1	0	-1.7 V
1	1	-2.2 V

SHIFT

- 1 = Ground shift above the threshold selected by GSLR1 and GSLR2
- 0 = No ground shift

The SHIFT information is latched until a read operation of the GSLR register occurs. The GSLR register is set to 0 after power-ON reset. A reset of GSLR1 and GSLR0 occurs when $\overline{\text{RST}} = \text{Low}$.

TXDOM

- 0 = No failure on TX
- 1 = TX permanent dominant

Table 28. Wake-Up Input Control Register (WUICR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUICR \$00C	R					SPIWU	BUSWU	WUCR1	WUICR0
	W								
RESET		—	—	—	—	0	0	0	0

This register configures the wake-up level for the L0, L1, and L2 inputs. It reports the CAN wake-up and SPI (CS) wake-up events during the Read operation.

Table 29. WUICR Bit Definition

WUICR1	WUICR0	Description
0	0	Wake-Up Inputs Disabled
0	1	Positive Edge Sensitive
1	0	Negative Edge Sensitive
1	1	Positive and Negative Sensitive

Table 30. WUICR Bit Definition

SPIWU	BUSWU	Description
0	0	No Wake-Up Events
0	1	Wake-Up Event on CAN Bus
1	0	Wake-Up Event on SPI Bus

The information is SPIWU and BUSWU is latched. Bits SPIWU and BUSWU will be reset by a read operation of the WUICR register and are set to 0 after a power-ON reset. A reset of WUICR1 and WUICR0 occurs when $\overline{\text{RST}} = \text{Low}$.

Table 31. Wake-Up Input Status Register (WUISR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUISR \$00F	R						WUISR2	WUISR1	WUISR0
	W								
RESET		—	—	—	—	—	0	0	0

This register reads back the wake input (L0, L1, L2) causing the SBC to wake-up.

Table 32. WUISR Bit Definition

WUISR2	WUISR1	WUISR0	Description
0	0	0	No Event on Wake-Up Inputs
x	x	1	Event on L0
x	1	x	Event on L1
1	x	x	Event on L2

In case of a wake-up event, the appropriate bit is set to 1. The bits will be reset by a Read operation of the register. After power-ON reset, all bits are set to 0.

Table 33. Wake-Up Input Real Time Information (WUIRTI)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUIRTI \$011	R						WUIRTI2	WUIRTI1	WUIRTI0
	W								
RESET		—	—	—	—	—	0	0	0

This register reports the real time information on the state; (High or Low) of the L0, L1, and L2 inputs. The bits WUIRTI 2:0 contain the real time logic value coming from the wake-up inputs (0 means input below threshold, 1 means input above threshold. Typical threshold is 3.5 V).

Table 34. Over Temperature Status Register (OTSR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTSR \$012	R					OPWV2	OPWV1	OPTV2	OTV1
	W							OTV2C	
RESET		—	—	—	—	0	0	0	0

This register reads back the over temperature status for the V1 and V2 regulators. It is used to turn V2 ON after a V2 over temperature shutdown occurred in the Write mode.

- OTV1: 1 = V1 over temperature shutdown, 0 = V1 no over temperature
- OTV2: 1 = V2 over temperature shutdown, 0 = V2 no over temperature
- OPWM1: 1 = V2 over temperature pre-warning, 0 = V2 normal temperature
- OPWV2: 1 = V2 over temperature pre-warning, 0 = V2 normal temperature

In case of V1 or V2 over temperature, the appropriate voltage regulators are switched OFF automatically, and the over temperature flags are set (latched). The flags can be reset by a Read operation of the register OTSR. Once V2 is switched OFF because of over temperature (OTV2 = 1) it can only be switched ON again by forcing OTV2C = 0 by a Write operation.

The V1 and V2 pre-warning flags are set as long as the first over temperature exists. The flags disappear, when the temperature is below the threshold. An over temperature of the V2 power supply will also switch OFF V3. After a power-ON reset, all bits of the register are set to 0.

Table 35. Transceiver Error Status Register for CANH (TESRH)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TESRH \$014	R					TESRH3	TESRH2	TESRH1	TESRH0
	W								
RESET		—	—	—	—	0	0	0	0

This register reports the CANH failure status.

Table 36. TESRH Bit Definition

TESRH3	TESRH2	TESRH1	TESRH0	Description
0	0	0	0	No Failure on CANH
0	x	0	1	CANH Wire Interruption
x	x	1	x	CANH Short Circuit to V_{BAT}
0	1	0	x	CANH Short Circuit to Ground
1	x	0	x	CANH Short Circuit to V_{CC}

In case of CANH line failures, the appropriate bit(s) are set according to [Table 36](#). This information is latched. The register can be reset by a Read operation. After power-ON is reset, all bits are set to 0.

Table 37. Transceiver Error Status Register for CANL and Tx (TESRL)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TESRL \$017	R					TESRL3	TESRL2	TESRL1	TESRL0
	W								
RESET		—	—	—	—	0	0	0	0

This register reports the CANL and Tx permanent failure status

Table 38. TESRL Bit Definition

TESRL3	TESRL2	TESRL1	TESRL0	Description
0	0	0	0	No Failure
0	x	0	1	CANL Wire Interruption
0	1	0	x	CANL Short Circuit to Ground/CANH mutually shorted to CANL
x	x	1	x	CANL Short Circuit to V_{BAT}
1	x	0	x	CANL Short Circuit to V_{DD}

In case of CANL line failures, the appropriate bit(s) are set according to [Table 38](#). This information is latched. The register can be reset by a Read operation. After power-ON is reset, all bits are set to 0.

Table 39. Reset Source Register (RSR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR \$018	R						RSR2	RSR1	RSR0
	W								
RESET		—	—	—	—	—	1	0	1

This register reports the source of a reset already occurred.

RSR0: 1 = > V_{DD1} under voltage occurred (RSR2 = 1 in this case), 0 = > no over voltage on V occurred

RSR1: 1 = > Software watchdog reset occurred (RSR 2 = 1 in this case), 0 = > no SW watchdog reset occurred

RSR2: 1 = > External reset occurred (RSR0 = RSR1 = 0 in this case), 0 = > no external reset occurred

Events related to the bits in register RSR are latched. All bits can be reset by a Read operation of the register. After a power-ON reset, RSR2 and RSR0 are set to 1. Therefore, the first read out of the register after power-ON delivers RSR[2:0] = [101].

Table 40. Voltage Supply Status Register (VSSR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VSSR \$01B	R					V3SR	V2SR	VBSR1	VBSR0
	W								
RESET		—	—	—	—	0	0	—	—
POR		—	—	—	—	0	0	0	1

This register monitors the status of the V2, V3, and V_{BAT} voltage level.

Table 41. VBSR1 VBSR0

VBSR1	VBSR0	Description
0	0	No Failure on VBAT
x	1	Under Voltage (BATFail)
1	x	Over Voltage (BATHigh)

V2SR: 1 = V2 ON, 0 = V2 OFF

V3SR: 1 = V3 over temperature, 0 = V3 no over temperature

VBSR1 is real time information. It cannot be reset. Bits V3SR, V2SR, and VBSR0 are latched and can be reset by a Read operation of the register.

The next two registers (IMR1 and IMR2) mask the interrupt function.

Table 42. Interrupt Mask Control Register 1 (IMR1)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IMR1 \$01D	R					HV	HTPW	MTPW	BATU
	W								
RESET		—	—	—	—	0	0	0	0

Table 43. Interrupt Mask Control Register 2 (IMR2)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IMR2 \$01E	R						BUSF	SPIE	WU
	W								
RESET		—	—	—	—	—	0	0	0

To enable the appropriate interrupt, the mask bit has to be set to 1. To disable the interrupt the bit, it must be cleared to 0. After a power-ON reset or RST = Low, the bits are cleared to 0. All interrupts are disabled. Explanation for the abbreviations:

HV = V_{BAT} High voltage

HT = High temperature on V1 or V2

MTPW = Medium temperature pre-warning on V1 or V2

BATU = Battery under voltage (BATFail)

BUSF = CAN bus failure

SPIE = SPI error

WU = Wake-up

The next two registers (ISR1 and ISR2) read the interrupt source. All bits in registers ISR1 and ISR2 are copies of the appropriate bits in different SPI registers. For a faster read-out, these bits are merged in ISR1 and ISR2. A reset cannot be completed for registers ISR1 and ISR2.

Table 44. Interrupt Source Register 1 (ISR1)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISR \$021	R					HV	HTPW	MTPW	BATU
	W								
RESET		—	—	—	—	0	0	0	0

Table 45. Interrupt Source Register 2 (ISR2)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISR \$022	R						BUSF	SPIE	WU
	W								
RESET		—	—	—	—	—	0	0	0

Table 46. Transceiver Control/Status Register (TCR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR \$024	R					TOT	TSR2	TSR1	TSR0
	W						TCR2	TCR1	TCR0
RESET		—	—	—	—	0	0	0	0

This register controls the state of the CAN transceiver (CAN transceiver is also dependent upon the SBC mode). When it is read, this register reports the CAN transceiver state and a CAN over temperature condition.

Table 47. TCR / TSR Data

TCR2	TCR1	TCR0	Description	TSR2	TSR1	TSR0
0	0	0	Standard/Term V _{BAT}	0	0	0
0	1	0	Standard/Rx Only	0	1	0
0	1	1	Standard/RxTx	0	1	1

TOT

1 => Transceiver over temperature

0 => Normal temperature

The MODE bit selects between the standard and extended physical layer mode. Any conditions forcing the transceiver to Term VBAT lead to reset of TCR0 and TCR01 bits. After power-ON reset all bits of the register are set to 0. The information TOT is latched. Reset TOT by reading the TCR. In case of $RST = Low$, the register content remains unchanged.

TYPICAL APPLICATIONS

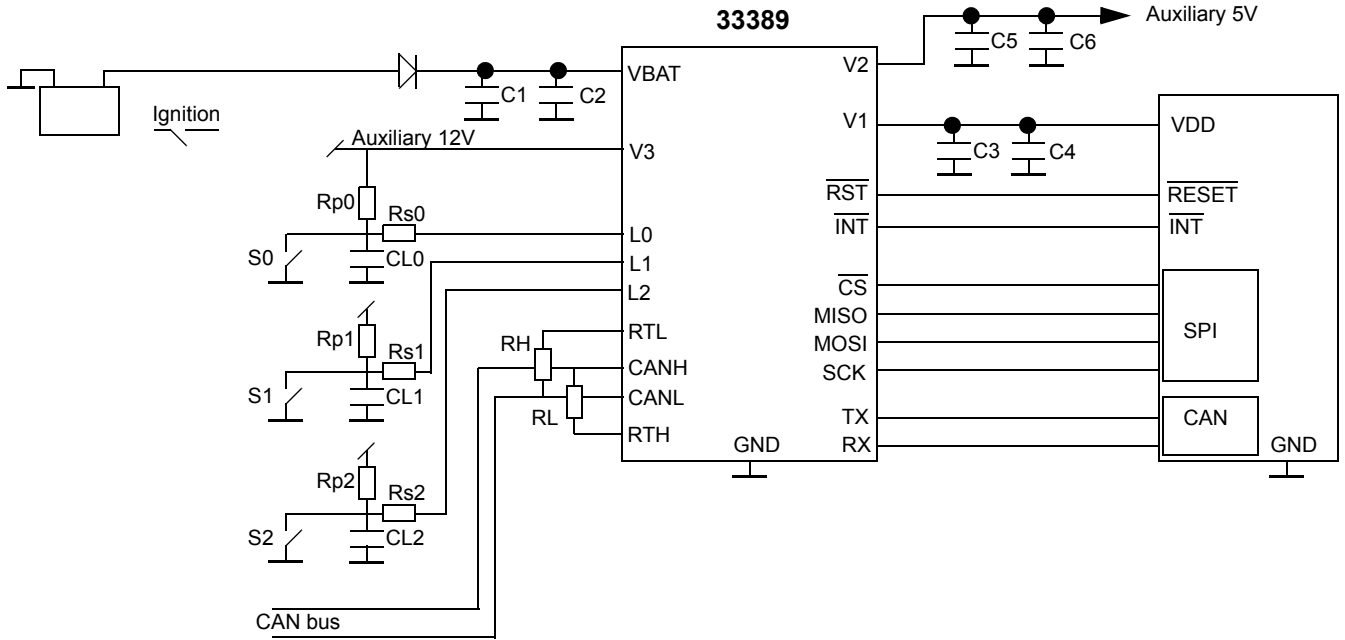


Figure 22. Typical Application Schematic 1

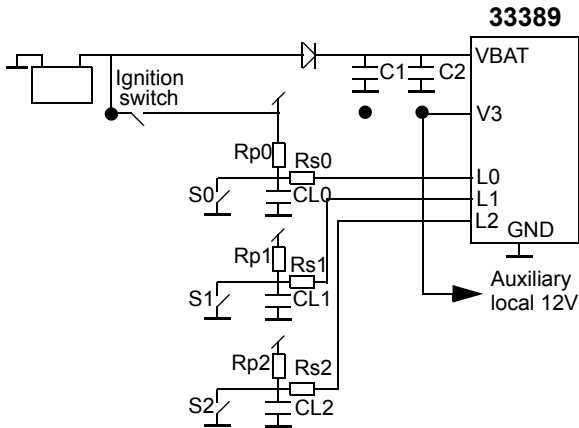


Figure 23. Typical Application: V3 Used as Auxiliary ECU Supply

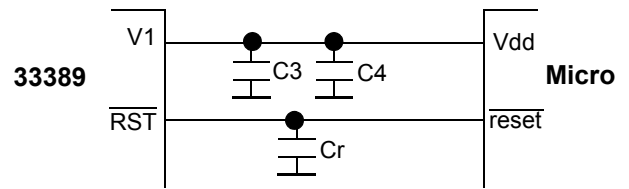
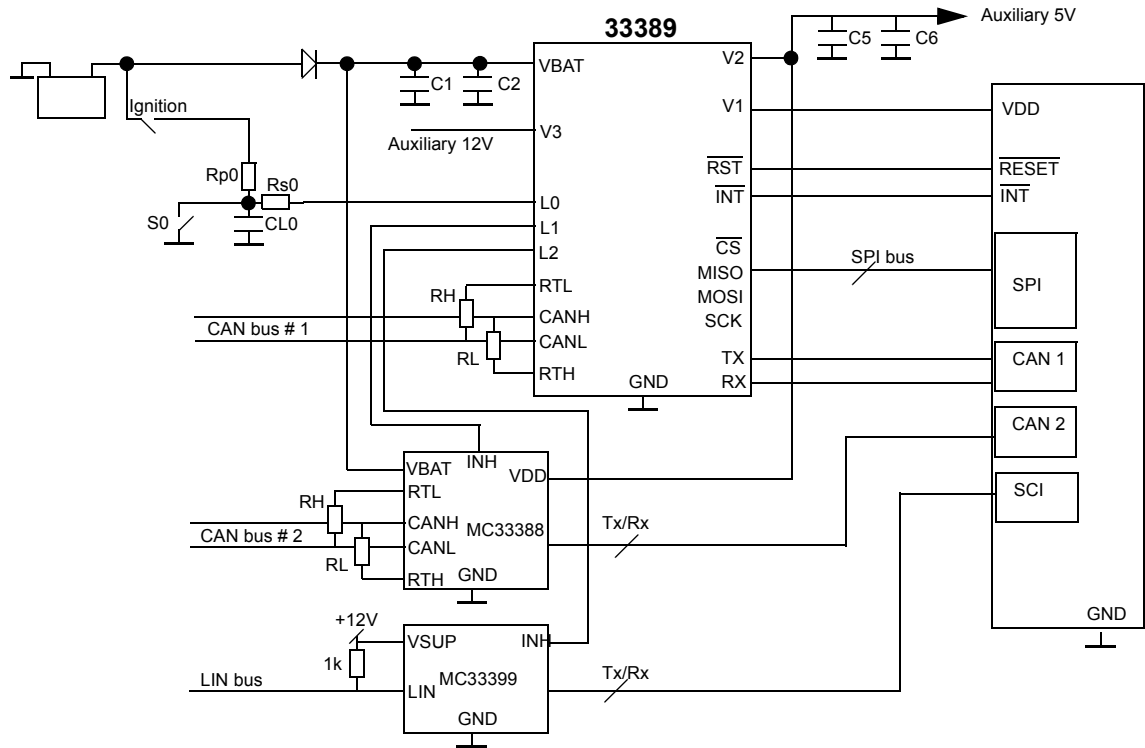


Figure 24. Reset Duration Extension



(Wake-up input linked to peripheral circuits: (ex: low speed CAN or LIN transceivers).

Figure 25. Typical Application Schematic 2

The SBC offers several capabilities to help users debug their application.

- External bias of V1 and reset pin
- Turn OFF software watchdog in the Stand-by mode
- Special debug samples with software watchdog disable at power-up (contact local Motorola representative)

DEBUG AND PROGRAM DOWNLOAD INTO FLASH MEMORY

While the SBC is powered, it enters Normal Request mode and expects during the 75 ms time period in the NR mode, an SPI trigger word (to enter Normal mode and select the watchdog time period). If this does not occur, the SBC enters the Sleep mode and turns off V1.

When the software is debugged, and when using development tools, it is not always easy to make sure these events happen properly. It is thus possible to externally power the V1 line with an external 5.0 V supply, and to force the Reset pin to V1 or to an external 5.0 V. These can be

done at nominal voltage and temperature. By doing this, 5.0 V is provided to the MCU V_{DD} and reset lines.

Under this condition the SBC is not operational. However, the reset pin is pulled low and is sinking 5 mA to ground. This means, the external circuitry driving reset must have a current capability higher than 5 mA in order to drive the reset in the high-state.

DISABLE OF SOFTWARE WATCHDOG IN STAND-BY MODE

The software watchdog can be disabled in Stand-by mode only. In order to disable it the following operation must be done:

- Write to MCR register—data 011 (bit 2, bit 1, bit 0)
- Write to MCVR register—data 011 (bit 2, bit 1, bit 0)

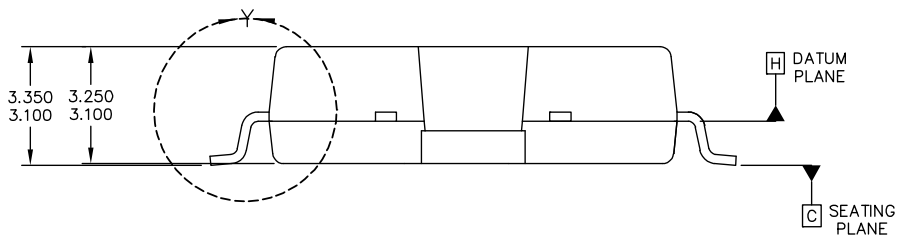
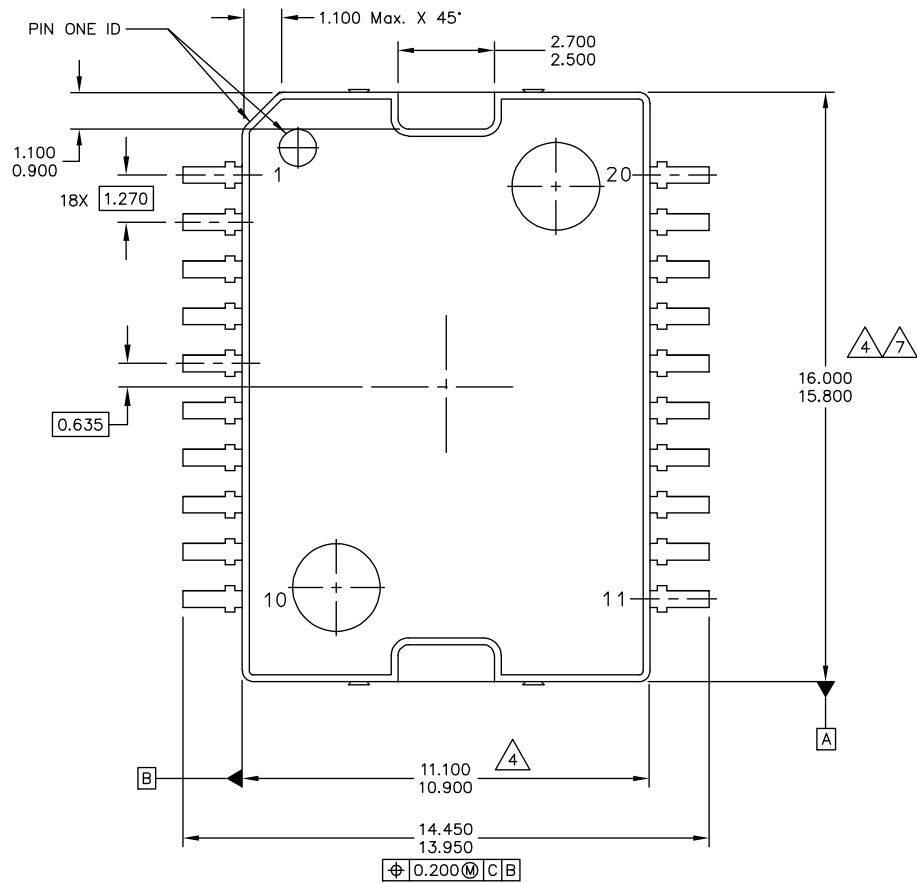
Then the SBC enters the Stand-by mode without software watchdog. However the V2 cannot be turned on, and the CAN cell cannot be used.

PACKAGING
PACKAGE DIMENSIONS

PACKAGING

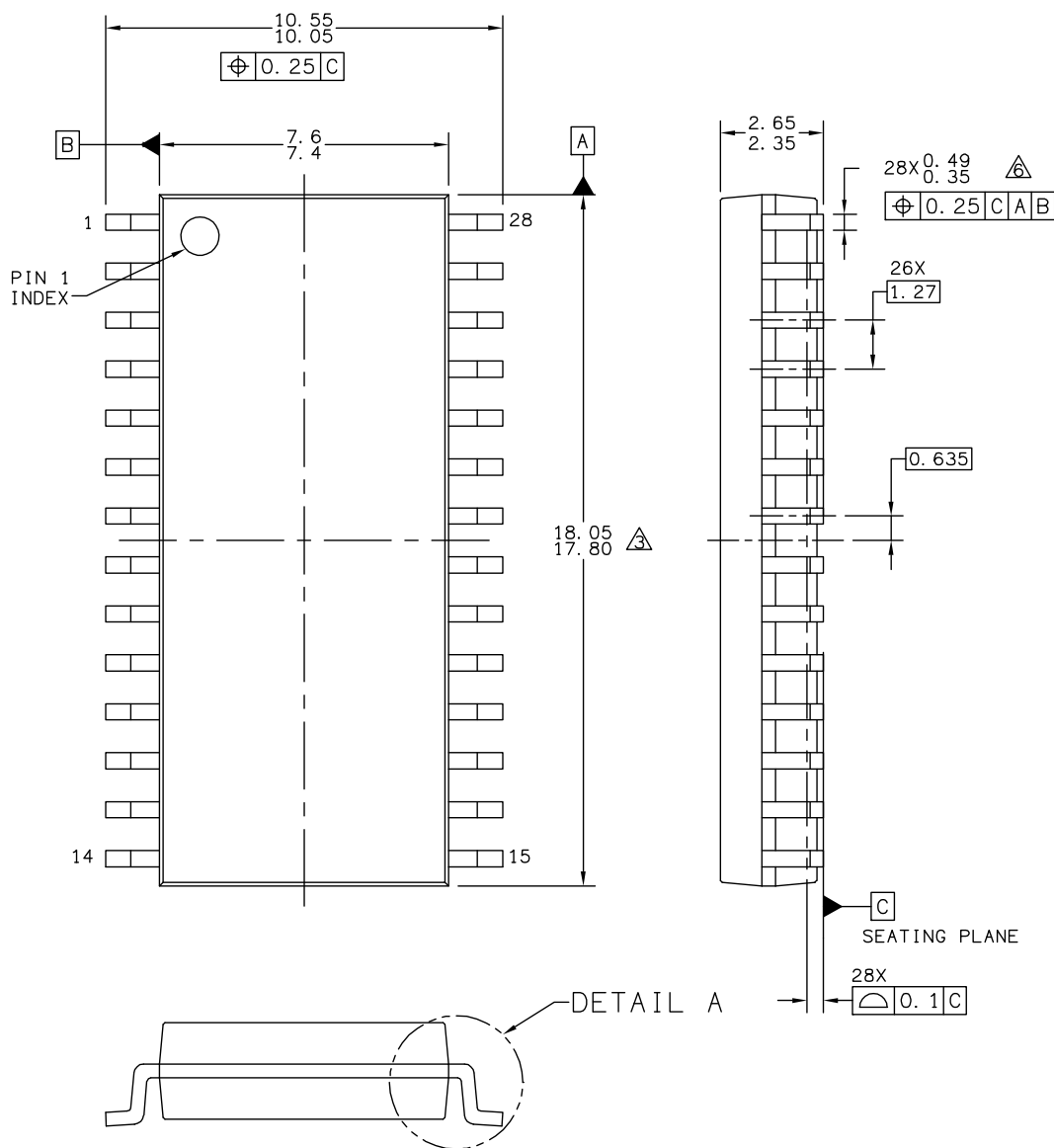
PACKAGE DIMENSIONS

For the most current package revision, visit www.freescale.com and perform a keyword search using the 98ASH70273A listed below.



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	STANDARD: NON-JEDEC		

DH SUFFIX
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20 PIN
PLASTIC PACKAGE
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	CASE NUMBER: 751F-05	10 MAR 2005	
	STANDARD: MS-013AE		

DW SUFFIX
EG SUFFIX (Pb-FREE)
28 PIN
PLASTIC PACKAGE
98ASB42345B
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