

MC56F8006/MC56F8002 Digital Signal Controller

This document applies to parts marked with 2M53M. The 56F8006/56F8002 is a member of the 56800E core-based family of digital signal controllers (DSCs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create a cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F8006/56F8002 is well-suited for many applications. It includes many peripherals that are especially useful for cost-sensitive applications, including:

- Industrial control
- Home appliances
- Smart sensors
- Fire and security systems
- Switched-mode power supply and power management
- Power metering
- Motor control (ACIM, BLDC, PMSM, SR, and stepper)
- Handheld power tools
- Arc detection
- Medical device/equipment
- Instrumentation
- Lighting ballast

The 56800E core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications. The 56F8006/56F8002 supports program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. The 56F8006/56F8002 also offers up to 40 general-purpose input/output (GPIO) lines, depending on peripheral configuration.

The 56F8006/56F8002 digital signal controller includes up to 16 KB of program flash and 2 KB of unified data/program

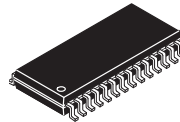
MC56F8006/MC56F8002



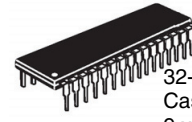
48-pin LQFP
 Case: 932-03
 7 x 7 mm²



32-pin LQFP
 Case: 873A-03
 7 x 7 mm²



28-pin SOIC
 Case: 751F-05
 7.5 x 18 mm²



32-pin PSDIP
 Case: 1376-02
 9 x 28.5 mm²

RAM. Program flash memory can be independently bulk erased or erased in small pages of 512 bytes (256 words).

On-chip features include:

- Up to 32 MIPS at 32 MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- On-chip memory
 - 56F8006: 16 KB (8K x 16) flash memory
 - 56F8002: 12 KB (6K x 16) flash memory
 - 2 KB (1K x 16) unified data/program RAM
- One 6-channel PWM module
- Two 28-channel, 12-bit analog-to-digital converters (ADCs)
- Two programmable gain amplifiers (PGA) with gain up to 32x
- Three analog comparators
- One programmable interval timer (PIT)
- One high-speed serial communication interface (SCI) with LIN slave functionality
- One serial peripheral interface (SPI)
- One 16-bit dual timer (2 x 16 bit timers)
- One programmable delay block (PDB)
- One SMBus compatible inter-integrated circuit (I²C) port
- One real time counter (RTC)
- Computer operating properly (COP)/watchdog
- Two on-chip relaxation oscillators — 1 kHz and 8 MHz (400 kHz at standby mode)
- Crystal oscillator
- Integrated power-on reset (POR) and low-voltage interrupt (LVI) module
- JTAG/enhanced on-chip emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 40 GPIO lines
- 28-pin SOIC, 32-pin LQFP, 32-pin PSDIP, and 48-pin LQFP packages

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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1 MC56F8006/MC56F8002 Family Configuration

MC56F8006/MC56F8002 device comparison in [Table 1](#).

Table 1. MC56F8006 Series Device Comparison

| Feature | MC56F8006 | | | MC56F8002 |
|--|-----------|--------|--------|-----------|
| | 28-pin | 32-pin | 48-pin | 28-pin |
| Flash memory size (Kbytes) | 16 | | | 12 |
| RAM size (Kbytes) | 2 | | | |
| Analog comparators (ACMP) | 3 | | | |
| Analog-to-digital converters (ADC) | 2 | | | |
| Unshielded ADC inputs | 6 | 7 | 7 | 6 |
| Shielded ADC inputs | 9 | 11 | 17 | 9 |
| Total number of ADC input pins ¹ | 15 | 18 | 24 | 15 |
| Programmable gain amplifiers (PGA) | 2 | | | |
| Pulse-width modulator (PWM) outputs | 6 | | | |
| PWM fault inputs | 3 | 4 | 4 | 3 |
| Inter-integrated circuit (IIC) | 1 | | | |
| Serial peripheral interface (SPI) | 1 | | | |
| High speed serial communications interface (SCI) | 1 | | | |
| Programmable interrupt timer (PIT) | 1 | | | |
| Programmable delay block (PDB) | 1 | | | |
| 16-bit multi-purpose timers (TMR) | 2 | | | |
| Real-time counter (RTC) | 1 | | | |
| Computer operating properly (COP) timer | Yes | | | |
| Phase-locked loop (PLL) | Yes | | | |
| 1 kHz on-chip oscillator | Yes | | | |
| 8 MHz (400 kHz at standby mode) on-chip ROSC | Yes | | | |
| Crystal oscillator | Yes | | | |
| Power management controller (PMC) | Yes | | | |
| IEEE 1149.1 Joint Test Action Group (JTAG) interface | Yes | | | |
| Enhanced on-chip emulator (EOnCE) IEEE 1149.1 Joint Test Action Group (JTAG) interface | Yes | | | |

¹ Some ADC inputs share the same pin. See [Table 4](#).

2 Block Diagram

Figure 1 shows a top-level block diagram of the MC56F8006/MC56F8002 digital signal controller. Package options for this family are described later in this document. Italics indicate a 56F8002 device parameter.

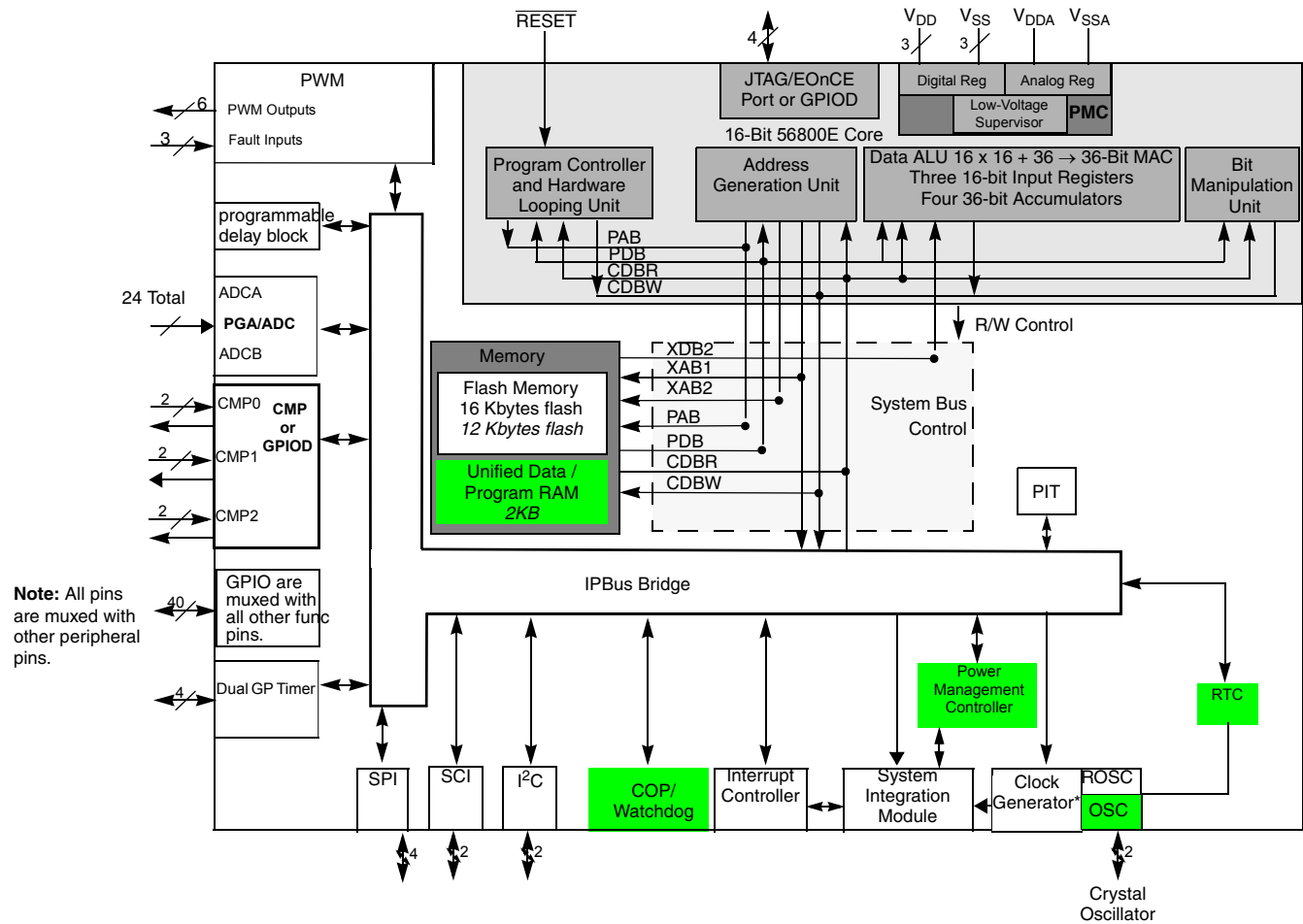


Figure 1. MC56F8006/MC56F8002 Block Diagram

3 Overview

3.1 56F8006/56F8002 Features

3.1.1 Core

- Efficient 16-bit 56800E family digital signal controller (DSC) engine with dual Harvard architecture
- As many as 32 million instructions per second (MIPS) at 32 MHz core frequency
- 155 basic instructions in conjunction with up to 20 address modes
- Single-cycle 16 × 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, processor speed-independent, real-time debugging

3.1.2 Operation Range

- 1.8 V to 3.6 V operation (power supplies and I/O)
- From power-on-reset: approximately 1.9 V to 3.6 V
- Ambient temperature operating range:
 - -40 °C to 125 °C

3.1.3 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal flash
- On-chip memory
 - 16 KB of program flash for 56F8006 and 12 KB of program flash for 56F8002
 - 2 KB of unified data/program RAM
- EEPROM emulation capability using flash

3.1.4 Interrupt Controller

- Five interrupt priority levels
 - Three user programmable priority levels for each interrupt source: Level 0, 1, 2
 - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction. Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, EOnCE trace buffer
 - Lowest-priority software interrupt: level LP
- Allow nested interrupt that higher priority level interrupt request can interrupt lower priority interrupt subroutine
- The masking of interrupt priority level is managed by the 56800E core
- One programmable fast interrupt that can be assigned to any interrupt source
- Notification to system integration module (SIM) to restart clock out of wait and stop states
- Ability to relocate interrupt vector table

3.1.5 Peripheral Highlights

- One multi-function, six-output pulse width modulator (PWM) module
 - Up to 96 MHz PWM operating clock
 - 15 bits of resolution
 - Center-aligned and edge-aligned PWM signal mode
 - Phase shifting PWM pulse generation

Overview

- Four programmable fault inputs with programmable digital filter
- Double-buffered PWM registers
- Separate deadtime insertions for rising and falling edges
- Separate top and bottom pulse-width correction by means of software
- Asymmetric PWM output within both Center Aligned and Edge Aligned operation
- Separate top and bottom polarity control
- Each complementary PWM signal pair allows selection of a PWM supply source from:
 - PWM generator
 - Internal timers
 - Analog comparator outputs
- Two independent 12-bit analog-to-digital converters (ADCs)
 - 2 x 14 channel external inputs plus seven internal inputs
 - Support simultaneous and software triggering conversions
 - ADC conversions can be synchronized by PWM and PDB modules
 - Sampling rate up to 400 KSPS for 10- or 12-bit conversion result; 470 KSPS for 8-bit conversion result
 - Two 16-word result registers
- Two programmable gain amplifier (PGAs)
 - Each PGA is designed to amplify and convert differential signals to a single-ended value fed to one of the ADC inputs
 - 1X, 2X, 4X, 8X, 16X, or 32X gain
 - Software and hardware triggers are available
 - Integrated sample/hold circuit
 - Includes additional calibration features:
 - Offset calibration eliminates any errors in the internal reference used to generate the VDDA/2 output center point
 - Gain calibration can be used to verify the gain of the overall datapath
 - Both features require software correction of the ADC result
- Three analog comparators (CMPs)
 - Selectable input source includes external pins, internal DACs
 - Programmable output polarity
 - Output can drive timer input, PWM fault input, PWM source, external pin output, and trigger ADCs
 - Output falling and rising edge detection able to generate interrupts
- One dual channel 16-bit multi-purpose timer module (TMR)
 - Two independent 16-bit counter/timers with cascading capability
 - Up to 96 MHz operating clock
 - Each timer has capture and compare and quadrature decoder capability
 - Up to 12 operating modes
 - Four external inputs and two external outputs
- One serial communication interface (SCI) with LIN slave functionality
 - Up to 96 MHz operating clock
 - Full-duplex or single-wire operation
 - Programmable 8- or 9- bit data format
 - Two receiver wakeup methods:
 - Idle line
 - Address mark

- 1/16 bit-time noise detection
- One serial peripheral interface (SPI)
 - Full-duplex operation
 - Master and slave modes
 - Programmable length transactions (2 to 16 bits)
 - Programmable transmit and receive shift order (MSB as first or last bit transmitted)
 - Maximum slave module frequency = module clock frequency/2
- One inter-integrated Circuit (I²C) port
 - Operates up to 400 kbps
 - Supports master and slave operation
 - Supports 10-bit address mode and broadcasting mode
 - Supports SMBus, Version 2
- One 16-bit programmable interval timer (PIT)
 - 16 bit counter with programmable counter modulo
 - Interrupt capability
- One 16-bit programmable delay block (PDB)
 - 16 bit counter with programmable counter modulo and delay time
 - Counter is initiated by positive transition of internal or external trigger pulse
 - Supports two independently controlled delay pulses used to synchronize PGA and ADC conversions with input trigger event
 - Two PDB outputs can be ORed together to schedule two conversions from one input trigger event
 - PDB outputs can be used to schedule precise edge placement for a pulsed output that generates the control signal for the CMP windowing comparison
 - Supports continuous or single shot mode
 - Bypass mode supported
- Computer operating properly (COP)/watchdog timer capable of selecting different clock sources
 - Programmable prescaler and timeout period
 - Programmable wait, stop, and partial powerdown mode operation
 - Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
 - Choice of clock sources from four sources in support of EN60730 and IEC61508:
 - On-chip relaxation oscillator
 - External crystal oscillator/external clock source
 - System clock (IPBus up to 32 MHz)
 - On-chip low power 1 kHz oscillator
- Real-timer counter (RTC)
 - 8-bit up-counter
 - Three software selectable clock sources
 - External crystal oscillator/external clock source
 - On-chip low-power 1 kHz oscillator
 - System bus (IPBus up to 32 MHz)
 - Can signal the device to exit power down mode
- Phase lock loop (PLL) provides a high-speed clock to the core and peripherals
 - Provides 3x system clock to PWM and dual timer and SCI
 - Loss of lock interrupt
 - Loss of reference clock interrupt

Overview

- Clock sources
 - On-chip relaxation oscillator with two user selectable frequencies: 400 kHz for low speed mode, 8 MHz for normal operation
 - On-chip low-power 1 kHz oscillator can be selected as clock source to the RTC and/or COP
 - External clock: crystal oscillator, ceramic resonator, and external clock source
- Power management controller (PMC)
 - On-chip regulator for digital and analog circuitry to lower cost and reduce noise
 - Integrated power-on reset (POR)
 - Low-voltage interrupt with a user selectable trip voltage of 1.81 V or 2.31 V
 - User selectable brown-out reset
 - Run, wait, and stop modes
 - Low-power run, wait, and stop modes
 - Partial power down mode
- Up to 40 general-purpose I/O (GPIO) pins
 - Individual control for each pin to be in peripheral or GPIO mode
 - Individual input/output direction control for each pin in GPIO mode
 - Hysteresis and configurable pullup device on all input pins
 - Configurable slew rate and drive strength and optional input low pass filters on all output pins
 - 20 mA sink/source current
- JTAG/EOnCE debug programming interface for real-time debugging
 - IEEE 1149.1 Joint Test Action Group (JTAG) interface
 - EOnCE interface for real-time debugging

3.1.6 Power Saving Features

- Three low power modes
 - Low-speed run, wait, and stop modes: 200 kHz IP bus clock provided by ROSC
 - Low-power run, wait, and stop modes: clock provided by external 32–38.4 kHz crystal
 - Partial power down mode
- Low power external oscillator can be used in any low-power mode to provide accurate clock to active peripherals
- Low power real time counter for use in run, wait, and stop modes with internal and external clock sources
- 32 μ s typical wakeup time from partial power down modes
- Each peripheral can be individually disabled to save power

3.2 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit, and development system cards support concurrent engineering. Together, PE, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

A full set of programmable peripherals — PWM, PGAs, ADCs, SCI, SPI, I²C, PIT, timers, and analog comparators — supports various applications. Each peripheral can be independently shut down to save power. Any pin in these peripherals can also be used as general-purpose input/outputs (GPIOs).

3.3 Architecture Block Diagram

The 56F8006/56F8002's architecture is shown in [Figure 2](#) and [Figure 3](#). [Figure 2](#) illustrates how the 56800E system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800E core. [Figure 3](#) shows the peripherals and control blocks connected to the IPBus bridge. Please see the system integration module (SIM) section in the *MC56F8006 Reference Manual* for information about which signals are multiplexed with those of other peripherals.

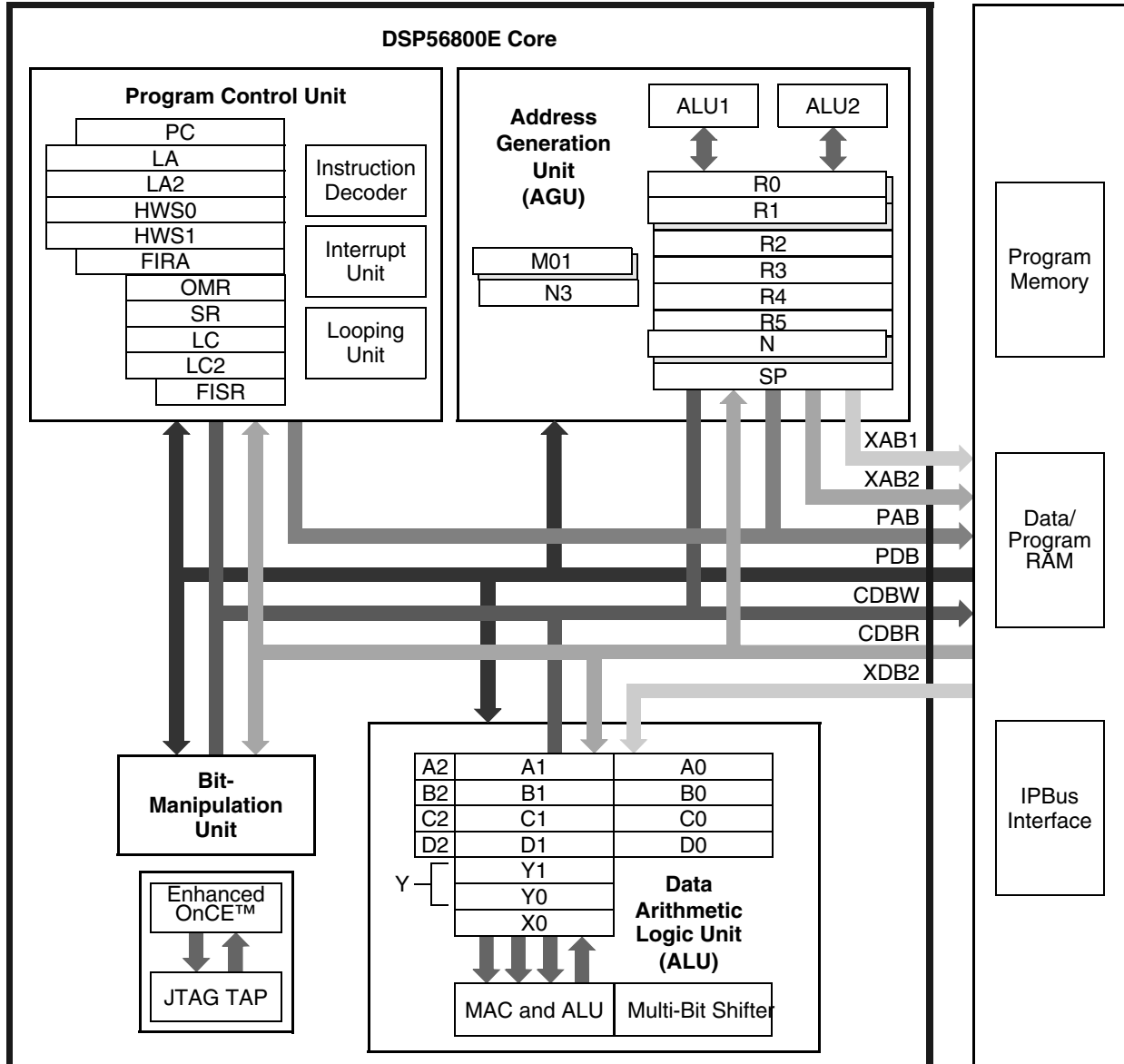


Figure 2. 56800E Core Block Diagram

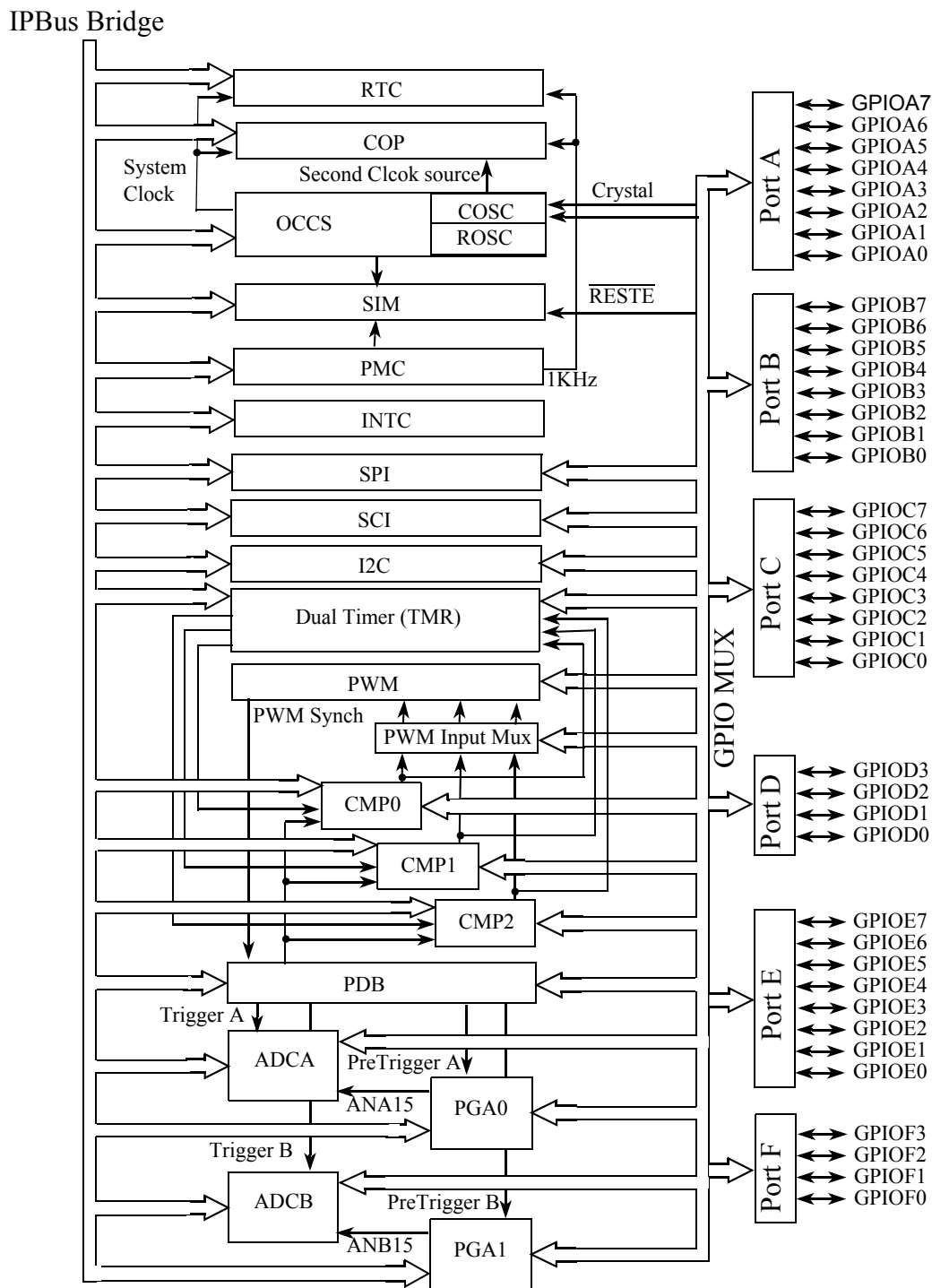


Figure 3. Peripheral Subsystem

3.4 Product Documentation

The documents listed in [Table 2](#) are required for a complete description and proper design with the 56F8006/56F8002. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at <http://www.freescale.com>.

Table 2. 56F8006/56F8002 Device Documentation

| Topic | Description | Order Number |
|--------------------------------------|--|--------------|
| DSP56800E Reference Manual | Detailed description of the 56800E family architecture, 16-bit digital signal controller core processor, and the instruction set | DSP56800ERM |
| 56F800x Peripheral Reference Manual | Detailed description of peripherals of the 56F8006 and 56F8002 devices | MC56F8006RM |
| 56F80x Serial Bootloader User Guide | Detailed description of the Serial Bootloader in the 56F800x family of devices | TBD |
| 56F8006/56F8002 Technical Data Sheet | Electrical and timing specifications, pin descriptions, and package descriptions (this document) | MC56F8006 |
| 56F8006/56F8002 Errata | Details any chip issues that might be present | MC56F8006E |

4 Signal/Connection Descriptions

4.1 Introduction

The input and output signals of the 56F8006/56F8002 are organized into functional groups, as detailed in [Table 3](#). [Table 4](#) summarizes all device pins. In [Table 4](#), each table row describes the signal or signals present on a pin, sorted by pin number.

Table 3. Functional Group Pin Allocations

| Functional Group | Number of Pins in 28 SOIC | Number of Pins in 32 LQFP | Number of Pins in 32 PSDIP | Number of Pins in 48 LQFP |
|--|---------------------------|---------------------------|----------------------------|---------------------------|
| Power Inputs (V_{DD} , V_{DDA}) | 2 | 2 | 2 | 4 |
| Ground (V_{SS} , V_{SSA}) | 3 | 3 | 3 | 4 |
| Reset ¹ | 1 | 1 | 1 | 1 |
| Pulse Width Modulator (PWM) Ports ¹ | 10 | 12 | 12 | 12 |
| Serial Peripheral Interface (SPI) Ports ¹ | 5 | 7 | 7 | 7 |
| Serial Communications Interface 0 (SCI) Ports ¹ | 4 | 5 | 5 | 5 |
| Inter-Integrated Circuit Interface (I ² C) Ports ¹ | 6 | 7 | 7 | 7 |
| Analog-to-Digital Converter (ADC) Inputs ¹ | 16 | 18 | 18 | 24 |
| High Speed Analog Comparators Inputs ¹ | 13 | 15 | 15 | 25 |
| Programmable Gain Amplifiers (PGA) ¹ | 4 | 4 | 4 | 4 |
| Dual Timer Module (TMR) Ports ¹ | 8 | 10 | 10 | 10 |
| Programmable Delay Block (PDB) ¹ | — | — | — | 1 |
| Clock ¹ | 5 | 5 | 5 | 5 |
| JTAG/Enhanced On-Chip Emulation (EOnCE ¹) | 4 | 4 | 4 | 4 |

¹ Pins may be shared with other peripherals. See [Table 4](#).

Signal/Connection Descriptions

In Table 4, peripheral pins in bold identify reset state.

Table 4. 56F8006/56F8002 Pins

| Pin Number | | | | Pin Name | Peripherals | | | | | | | | | | | |
|------------|---------|----------|---------|--|-------------|------------------|-----|-----------------|---|-------|-------------------|------------|--------|------------------|------|--------------------|
| 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | | GPIO | I ² C | SCI | SPI | ADC | PGA | COMP | Dual Timer | PWM | Power and Ground | JTAG | Misc. |
| | 1 | 29 | 1 | GPIOB6/RXD/SDA/ANA13 and CMP0_P2/CLKIN | B6 | SDA | RXD | | ANA13 ¹ | | CMP0_P2 | | | | | CLKIN |
| | 2 | 30 | 2 | GPIOB1/ \overline{SS} /SDA/ANA12 and CMP2_P3 | B1 | SDA | | \overline{SS} | ANA12 ¹ | | CMP2_P3 | | | | | |
| | 3 | 31 | 3 | GPIOB7/TXD/SCL/ANA11 and CMP2_M3 | B7 | SCL | TXD | | ANA11 ¹ | | CMP2_M3 | | | | | |
| | 4 | 32 | 4 | GPIOB5/T1/FAULT3/SCLK | B5 | | | SCLK | | | | T1 | FAULT3 | | | |
| | | | 5 | GPIOE0 | E0 | | | | | | | | | | | |
| | | | 6 | GPIOE1/ANB9 and CMP0_P1 | E1 | | | | ANB9 ¹ | | CMP0_P1 | | | | | |
| 28 | 5 | 1 | 7 | ANB8 and PGA1+ and CMP0_M2/GPIOC4 | C4 | | | | ANB8 ¹ | PGA1+ | CMP0_M2 | | | | | |
| | | | 8 | GPIOE2/ANB7 and CMP0_M1 | E2 | | | | ANB7 ¹ | | CMP0_M1 | | | | | |
| 1 | 6 | 2 | 9 | ANB6 and PGA1- and CMP0_P4/GPIOC5 | C5 | | | | ANB6 ¹ | PGA1- | CMP0_P4 | | | | | |
| | | | 10 | GPIOC7/ANB5 and CMP1_M2 | C7 | | | | ANB5 ¹ | | CMP1_M2 | | | | | |
| 2 | 7 | 3 | 11 | ANB4 and CMP1_P1/GPIOC6/PWM2 | C6 | | | | ANB4 ¹ | | CMP1_P1 | | PWM2 | | | |
| 3 | 8 | 4 | 12 | V _{DDA} | | | | | | | | | | | | V _{DDA} |
| 4 | 9 | 5 | 13 | V _{SSA} | | | | | | | | | | | | V _{SSA} |
| | | | 14 | GPIOE3/ANA10 and CMP2_M1 | E3 | | | | ANA10 ¹ | | CMP2_M1 | | | | | |
| 5 | 10 | 6 | 15 | ANA9 and PGA0- and CMP2_P4/GPIOC2 | C2 | | | | ANA9 ¹ | PGA0- | CMP2_P4 | | | | | |
| | | | 16 | GPIOE5/ANA8 and CMP2_P1 | E5 | | | | ANA8 ¹ | | CMP2_P1 | | | | | |
| 6 | 11 | 7 | 17 | ANA7 and PGA0+ and CMP2_M2/GPIOC1 | C1 | | | | ANA7 ¹ | PGA0+ | CMP2_M2 | | | | | |
| | | | 18 | GPIOE4/ANA6 and CMP2_P2 | E4 | | | | ANA6 ¹ | | CMP2_P2 | | | | | |
| 7 | 12 | 8 | 19 | ANA5 and CMP1_M1/GPIOC0/FAULT0 | C0 | | | | ANA5 ¹ | | CMP1_M1 | | FAULT0 | | | |
| 8 | 13 | 9 | 20 | V _{SS} | | | | | | | | | | | | V _{SS} |
| | | | 21 | V _{DD} | | | | | | | | | | | | V _{DD} |
| 9 | 14 | 10 | 22 | TCK/GPIOD2/ANA4 and CMP1_P2/CMP2_OUT | D2 | | | | ANA4 ¹ | | CMP1_P2, CMP2_OUT | | | | | TCK |
| 10 | 15 | 11 | 23 | \overline{RESET} /GPIOA7 | A7 | | | | | | | | | | | \overline{RESET} |
| 11 | 16 | 12 | 24 | GPIOB3/MOSI/TIN3/ANA3 and ANB3/PWM5/CMP1_OUT | B3 | | | MOSI | ANA3 ¹ and ANB3 ¹ | | CMP1_OUT | TIN3 | PWM5 | | | |
| | 17 | 13 | 25 | GPIOB2/MISO/TIN2/ANA2 and ANB2/CMP0_OUT | B2 | | | MISO | ANA2 and ANB2 | | CMP0_OUT | TIN2 | | | | |
| 12 | 18 | 14 | 26 | GPIOA6/FAULT0/ANA1 and ANB1/SCL/TXD/CLKO_1 | A6 | SCL | TXD | | ANA1 and ANB1 | | | | FAULT0 | | | CLKO_1 |
| 13 | 19 | 15 | 27 | GPIOB4/T0/CLKO_0/MISO/SDA/RXD/ANA0 and ANB0 | B4 | SDA | RXD | MISO | ANA0 and ANB0 | | | T0 | | | | CLKO_0 |

Table 4. 56F8006/56F8002 Pins (continued)

| Pin Number | | | | Pin Name | Peripherals | | | | | | | | | | | |
|------------|---------|----------|---------|-------------------------------------|-------------|------------------|-----|------|-------|---------|----------|--------------------------|-----------------|------------------|------|-------------|
| 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | | GPIO | I ² C | SCI | SPI | ADC | PGA | COMP | Dual Timer | PWM | Power and Ground | JTAG | Misc. |
| | | | 28 | GPIOE6 | E6 | | | | | | | | | | | |
| 14 | 20 | 16 | 29 | GPIOA5/PWM5/FAULT2 or EXT_SYNC/TIN3 | A5 | | | | | | TIN3 | PWM5, FAULT2 or EXT_SYNC | | | | |
| | | | 30 | V _{SS} | | | | | | | | | V _{SS} | | | |
| | | | 31 | V _{DD} | | | | | | | | | V _{DD} | | | |
| 15 | 21 | 17 | 32 | GPIOB0/SCLK/SCL/ANB13/PWM3/T1 | B0 | SCL | | SCLK | ANB13 | | T1 | PWM3 | | | | |
| 16 | 22 | 18 | 33 | GPIOA4/PWM4/SDA/FAULT1/TIN2 | A4 | SDA | | | | | TIN2 | PWM4, FAULT1 | | | | |
| | | | 34 | GPIOE7/CMP1_M3 | E7 | | | | | CMP1_M3 | | | | | | |
| | 23 | 19 | 35 | GPIOA2/PWM2 | A2 | | | | | | | PWM2 | | | | |
| 17 | 24 | 20 | 36 | GPIOA3/PWM3/TXD/EXTAL | A3 | | TXD | | | | | PWM3 | | | | EXTAL |
| 18 | 25 | 21 | 37 | GPIOF0/XTAL | F0 | | | | | | | | | | | XTAL |
| 19 | 26 | 22 | 38 | V _{DD} | | | | | | | | | V _{DD} | | | |
| 20 | 27 | 23 | 39 | V _{SS} | | | | | | | | | V _{SS} | | | |
| | | | 40 | GPIOF1/CMP1_P3 | F1 | | | | | CMP1_P3 | | | | | | |
| | | | 41 | GPIOF2/CMP0_M3 | F2 | | | | | CMP0_M3 | | | | | | |
| | | | 42 | GPIOF3/CMP0_P3 | F3 | | | | | CMP0_P3 | | | | | | |
| 21 | 28 | 24 | 43 | GPIOA1/PWM1 | A1 | | | | | | | PWM1 | | | | |
| 22 | 29 | 25 | 44 | GPIOA0/PWM0 | A0 | | | | | | | PWM0 | | | | |
| 23 | 30 | 26 | 45 | TDI/GPIOD0/ANB12/SS/TIN2/CMP0_OUT | D0 | | | SS | ANB12 | | CMP0_OUT | TIN2 | | | TDI | |
| | | | 46 | GPIOC3/EXT_TRIGGER | C3 | | | | | | | | | | | EXT_TRIGGER |
| 24 | 31 | 27 | 47 | TMS/GPIOD3/ANB11/T1/CMP1_OUT | D3 | | | | ANB11 | | CMP1_OUT | T1 | | | TMS | |
| 25 | 32 | 28 | 48 | TDO/GPIOD1/ANB10/T0/CMP2_OUT | D1 | | | | ANB10 | | CMP2_OUT | T0 | | | TDO | |

¹ Shielded ADC input.

4.2 Pin Assignment

MC56F8006 and MC56F8002 28-pin small outline IC (28SOIC) assignment is shown in [Figure 4](#); MC56F8006 32-pin low-profile quad flat pack (32LQFP) is shown in [Figure 5](#); MC56F8006 32-pin plastic shrink dual in-line package (PSDIP) is shown in [Figure 6](#); MC56F8006 48-pin low-profile quad flat pack (48LQFP) is shown in [Figure 7](#).

Signal/Connection Descriptions

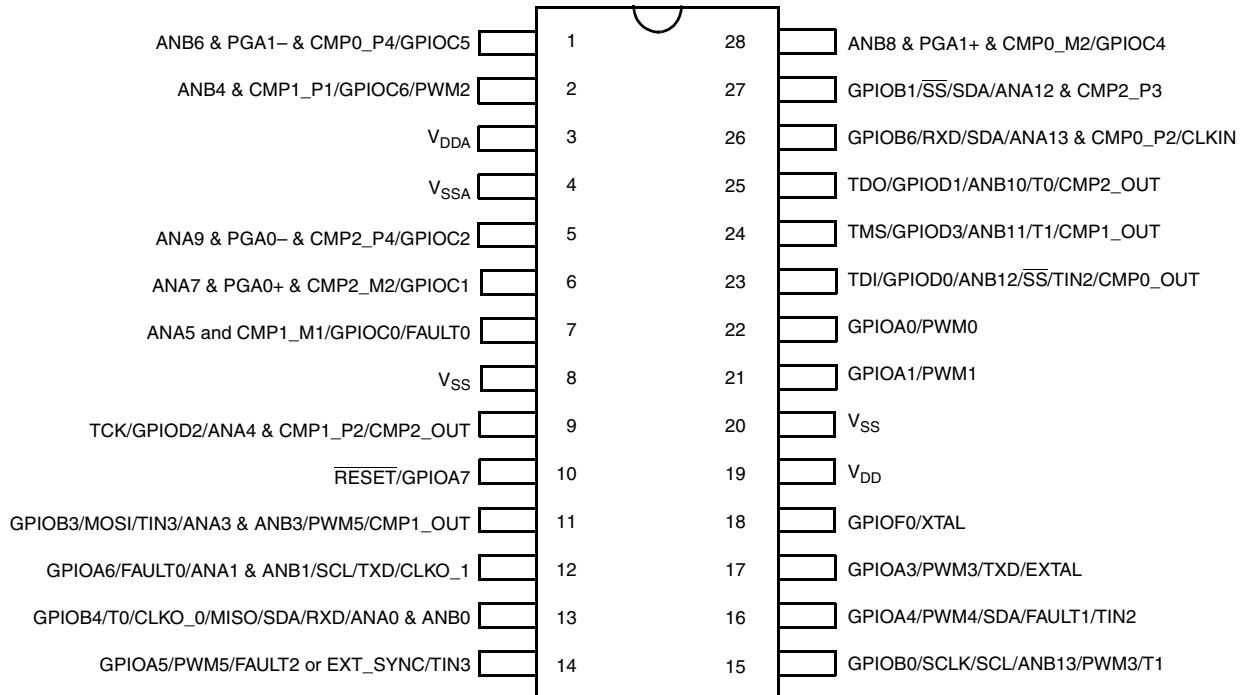


Figure 4. Top View, MC56F8006/MC56F8002 28-Pin SOIC Package

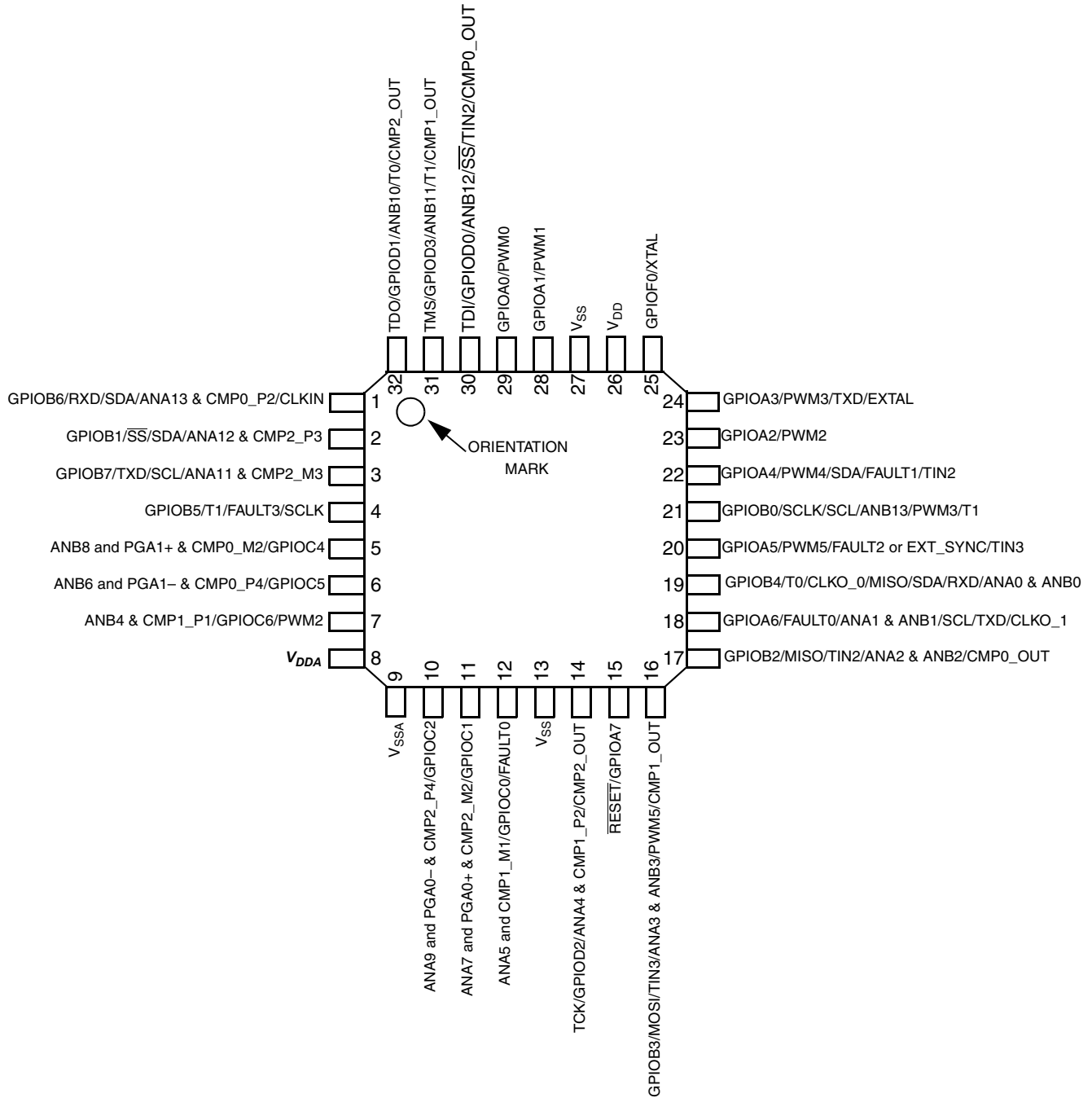


Figure 5. Top View, MC56F8006 32-Pin LQFP Package

Signal/Connection Descriptions

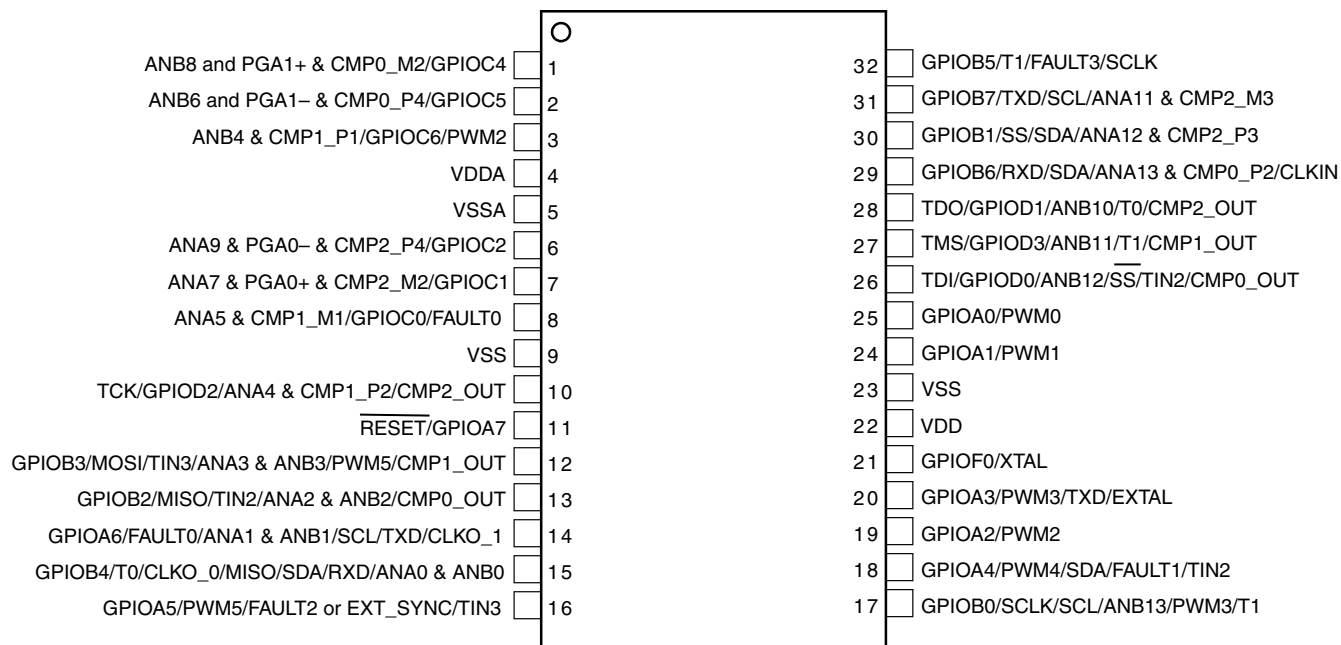


Figure 6. Top View, MC56F8006 32-Pin PSDIP Package

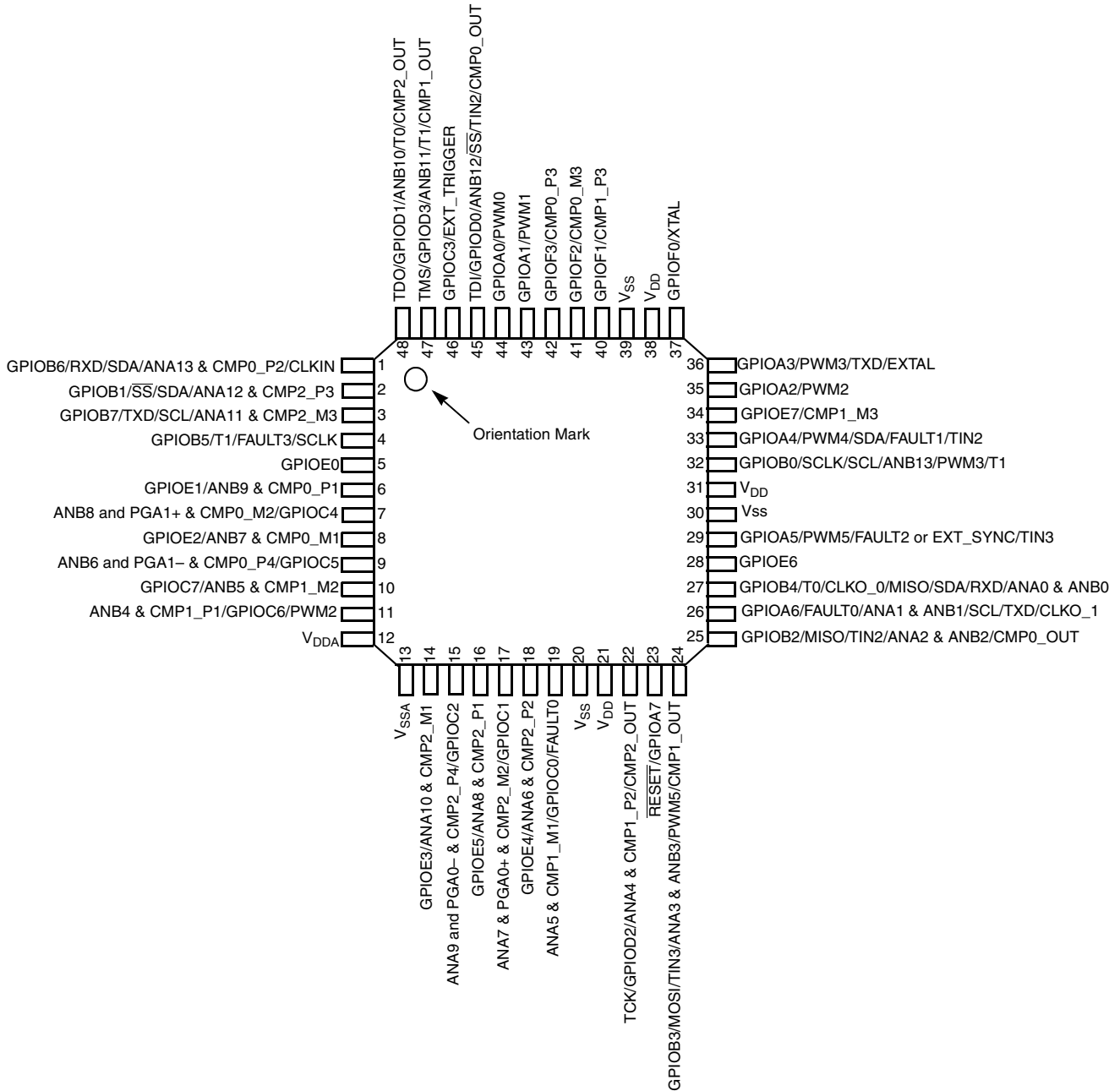


Figure 7. Top View, MC56F8006 48-Pin LQFP Package

4.3 56F8006/56F8002 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed via the GPIO module's peripheral enable registers (GPIO_x_PER) and SIM module's (GPS_xn) GPIO peripheral select registers. If CLKIN or XTAL is selected as device external clock input, the CLK_MOD bit in the OCCS oscillator control register (OSCTL) needs to be set too. EXT_SEL bit in OSCTL selects CLKIN or XTAL.

Table 5. 56F8006/56F8002 Signal and Package Information

| Signal Name | 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | Type | State During Reset | Signal Description |
|------------------|---------|---------|----------|---------|--------------|--------------------------------|--|
| V _{DD} | | | | 21 | Supply | Supply | I/O Power — This pin supplies 3.3 V power to the chip I/O interface. |
| V _{DD} | | | | 31 | | | |
| V _{DD} | 19 | 26 | 22 | 38 | | | |
| V _{SS} | 8 | 13 | 9 | 20 | Supply | Supply | I/O Ground — These pins provide ground for chip I/O interface. |
| V _{SS} | | | | 30 | | | |
| V _{SS} | 20 | 27 | 23 | 39 | | | |
| V _{DDA} | 3 | 8 | 4 | 12 | Supply | Supply | Analog Power — This pin supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply. |
| V _{SSA} | 4 | 9 | 5 | 13 | Supply | Supply | Analog Ground — This pin supplies an analog ground to the analog modules. It must be connected to a clean power supply. |
| RESET | 10 | 15 | 11 | 23 | Input | Input, internal pullup enabled | Reset — This input is a direct hardware reset on the processor. When RESET is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. |
| (GPIOA7) | | | | | Input/Output | | Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. RESET functionality is disabled in this mode and the chip can be reset only via POR, COP reset, or software reset. After reset, the default state is RESET. |
| GPIOA0 | 22 | 29 | 25 | 44 | Input/Output | Input, internal pullup enabled | Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. |
| (PWM0) | | | | | Output | | PWM0 — The PWM channel 0. After reset, the default state is GPIOA0. |
| GPIOA1 | 21 | 28 | 24 | 43 | Input/Output | Input, internal pullup enabled | Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. |
| (PWM1) | | | | | Output | | PWM1 — The PWM channel 1. After reset, the default state is GPIOA1. |
| GPIOA2 | | 23 | 19 | 35 | Input/Output | Input, internal pullup enabled | Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. |
| (PWM2) | | | | | Output | | PWM2 — The PWM channel 2. After reset, the default state is GPIOA2. |

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

| Signal Name | 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | Type | State During Reset | Signal Description |
|---|---------|---------|----------|---------|---|--------------------------------|---|
| GPIOA3 (PWM3) (TXD) (EXTAL) | 17 | 24 | 20 | 36 | Input/Output Output Output Analog Input | Input, internal pullup enabled | <p>Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>PWM3 — The PWM channel 3.</p> <p>TXD — The SCI transmit data output or transmit/receive in single wire operation.</p> <p>EXTAL — External Crystal Oscillator Input. This input can be connected to a 32.768 kHz or 1–16 MHz external crystal or ceramic resonator. When used to supply a source to the internal PLL, the crystal/resonator must be in the 4 MHz to 8 MHz range. Tie this pin low or configure as GPIO if XTAL is being driven by an external clock source.</p> <p>If using a 32.768 kHz crystal, place the crystal as close as possible to device pins to speed startup.</p> <p>After reset, the default state is GPIOA3.</p> |
| GPIOA4 (PWM4) (SDA) (FAULT1) (TIN2) | 16 | 22 | 18 | 33 | Input/Output Output Input/Open-drain Output Input Input | Input, internal pullup enabled | <p>Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>PWM4 — The PWM channel 4.</p> <p>SDA — The I²C serial data line.</p> <p>FAULT1 — PWM fault input 1 used for disabling selected PWM outputs in cases where fault conditions originate off-chip.</p> <p>TIN2 — Dual timer module channel 2 input</p> <p>After reset, the default state is GPIOA4.</p> |
| GPIOA5 (PWM5) (FAULT2/EXT_SYNC) (TIN3) | 14 | 20 | 16 | 29 | Input/Output Output Input/Output Input | Input, internal pullup enabled | <p>Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>PWM5 — The PWM channel 5.</p> <p>FAULT2 — PWM fault input 2 used for disabling selected PWM outputs in cases where fault conditions originate off-chip.</p> <p>EXT_SYNC — When not being used as a fault input, this pin can be used to receive a pulse to reset the PWM counter or to generate a positive pulse at the start of every PWM cycle.</p> <p>TIN3 — Dual timer module channel 3 input</p> <p>After reset, the default state is GPIOA5.</p> |

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

| Signal Name | 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | Type | State During Reset | Signal Description |
|---|---------|---------|----------|---------|---|--------------------------------|---|
| GPIOA6 (FAULT0) (ANA1 & ANB1) (SCL) (TXD) (CLKO_1) | 12 | 18 | 14 | 26 | Input/Output Input Analog Input Input/Open-drain Output Output Output | Input, internal pullup enabled | <p>Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>FAULT0 — PWM fault input 0 used for disabling selected PWM outputs in cases where fault conditions originate off-chip.</p> <p>ANA1 and ANB1 — Analog input to channel 1 of ADCA and ADCB.</p> <p>SCL — The I²C serial clock</p> <p>TXD — The SCI transmit data output or transmit/receive in single wire operation.</p> <p>CLKO_1 — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) in the SIM.</p> <p>When used as an analog input, the signal goes to the ANA1 and ANB1.</p> <p>After reset, the default state is GPIOA6.</p> |
| GPIOB0 (SCLK) (SCL) (ANB13) (PWM3) (T1) | 15 | 21 | 17 | 32 | Input/Output Input/Output Input/Open-drain Output Analog Input Output Input/Output | Input, internal pullup enabled | <p>Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>SCLK — The SPI serial clock. In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.</p> <p>SCL — The I²C serial clock.</p> <p>ANB13 — Analog input to channel 13 of ADCB</p> <p>PWM3 — The PWM channel 3.</p> <p>T1 — Dual timer module channel 1 input/output.</p> <p>After reset, the default state is GPIOB0.</p> |

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

| Signal Name | 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | Type | State During Reset | Signal Description |
|---|---------|---------|----------|---------|--|--------------------------------|---|
| GPIOB1 (\overline{SS}) (SDA) (ANA12 and CMP2_P3) | 27 | 2 | 30 | 2 | Input/Output Input/Output Input/Open-drain Output Analog input | Input, internal pullup enabled | <p>Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>\overline{SS} — \overline{SS} is used in slave mode to indicate to the SPI module that the current transfer is to be received.</p> <p>SDA — The I²C serial data line.</p> <p>ANA12 and CMP2_P3 — Analog input to channel 12 of ADCA and Positive input 3 of analog comparator 2.</p> <p>When used as an analog input, the signal goes to the ANA12 and CMP2_P3.</p> <p>After reset, the default state is GPIOB1.</p> |
| GPIOB2 (MISO) (TIN2) (ANA2 and ANB2) (CMP0_OUT) | | 17 | 13 | 25 | Input/Output Input/Output Input/Output Analog Input Output | Input, internal pullup enabled | <p>Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.</p> <p>TIN2 — Dual timer module channel 2 input.</p> <p>ANA2 and ANB2 — Analog input to channel 2 of ADCA and ADCB.</p> <p>CMP0_OUT— Analog comparator 0 output.</p> <p>When used as an analog input, the signal goes to the ANA2 and ANB2.</p> <p>After reset, the default state is GPIOB2.</p> |

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

| Signal Name | 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | Type | State During Reset | Signal Description |
|---|---------|---------|----------|---------|--|--------------------------------|--|
| GPIOB3 (MOSI) (TIN3) (ANA3 and ANB3) (PWM5) (CMP1_OUT) | 11 | 16 | 12 | 24 | Input/Output Input/Output Input/Output Input Output Output | Input, internal pullup enabled | Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. MOSI — Master out/slave in. In master mode, this pin serves as the data output. In slave mode, this pin serves as the data input. TIN3 — Dual timer module channel 3 input. ANA3 and ANB3 — Analog input to channel 3 of ADCA and ADCB. PWM5 — The PWM channel 5. CMP1_OUT— Analog comparator 1 output. When used as an analog input, the signal goes to the ANA3 and ANB3. After reset, the default state is GPIOB3. |
| GPIOB4 (T0) (CLKO_0) (MISO) (SDA) (RXD) (ANA0 and ANB0) | 13 | 19 | 15 | 27 | Input/Output Input/Output Output Input/Output Input/Open-drain Output Input Analog Input | Input, internal pullup enabled | Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. T0 — Dual timer module channel 0 input/output. CLKO_0 — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM. MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. SDA — The I ² C serial data line. RXD — The SCI receive data input. ANA0 and ANB0 — Analog input to channel 0 of ADCA and ADCB. When used as an analog input, the signal goes to the ANA0 and ANB0. After reset, the default state is GPIOB4. |

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

| Signal Name | 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | Type | State During Reset | Signal Description |
|---|---------|---------|----------|---------|---|--------------------------------|--|
| GPIOB5 (T1) (FAULT3) (SCLK) | | 4 | 32 | 4 | Input/Output Input/Output Input Input | Input, internal pullup enabled | <p>Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>T1 — Dual timer module channel 1 input/output.</p> <p>FAULT3 — PWM fault input 3 used for disabling selected PWM outputs in cases where fault conditions originate off-chip.</p> <p>SCLK — SPI serial clock. In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.</p> <p>After reset, the default state is GPIOB5.</p> |
| GPIOB6 (SDA) (ANA13 and CMP0_P2) (CLKIN) | 26 | 1 | 29 | 1 | Input/Output Input/Open-drain Output Analog Input Input | Input, internal pullup enabled | <p>Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>SDA — The I²C serial data line.</p> <p>ANA13 and CMP0_P2 — Analog input to channel 13 of ADCA and positive input 2 of analog comparator 0.</p> <p>External Clock Input — This pin serves as an external clock input.</p> <p>When used as an analog input, the signal goes to the ANA13 and CMP0_P2.</p> <p>After reset, the default state is GPIOB6.</p> |
| GPIOB7 (TXD) (SCL) (ANA11 and CMP2_M3) | | 3 | 31 | 3 | Input/Output Input/Output Input/Open-drain Output Analog Input | Input, internal pullup enabled | <p>Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>TXD — The SCI transmit data output or transmit/receive in single wire operation.</p> <p>SCL — The I²C serial clock.</p> <p>ANA11 and CMP2_M3 — Analog input to channel 11 of ADCA and negative input 3 of analog comparator 2.</p> <p>When used as an analog input, the signal goes to the ANA11 and CMP2_M3.</p> <p>After reset, the default state is GPIOB7.</p> |

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

| Signal Name | 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | Type | State During Reset | Signal Description |
|--|---------|---------|----------|---------|---|--------------------------------|---|
| ANA5 and CMP1_M1 (GPIOC0) (FAULT0) | 7 | 12 | 8 | 19 | Analog Input Analog Input Input | Analog Input | ANA5 and CMP1_M1— Analog input to channel 5 of ADCA and negative input 1 of analog comparator 1. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. FAULT0 — PWM fault input 0 is used for disabling selected PWM outputs in cases where fault conditions originate off-chip. When used as an analog input, the signal goes to the ANA5 and CMP1_M1. After reset, the default state is ANA5 and CMP1_M1. |
| ANA7 and PGA0+ and CMP2_M2 (GPIOC1) | 6 | 11 | 7 | 17 | Analog Input Input/Output | Analog Input | ANA7 and PGA0+ and CMP2_M2 — Analog input to channel 7 of ADCA and PGA0 positive input and negative input 2 of analog comparator 2. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. When used as an analog input, The signal goes to the ANA7 and PGA0+ and CMP2_M2. After reset, the default state is ANA7 and PGA0+ and CMP2_M2. |
| ANA9 and PGA0– and CMP2_P4 (GPIOC2) | 5 | 10 | 6 | 15 | Analog Input Input/Output | Analog Input | ANA9 and PGA0– and CMP2_P4 — Analog input to channel 9 of ADCA and PGA0 negative input and positive input 4 of analog comparator 2. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. When used as an analog input, The signal goes to the ANA9 and PGA0– and CMP2_P4. After reset, the default state is ANA9 and PGA0– and CMP2_P4. |
| GPIOC3 (EXT_TRIGGER) | | | | 46 | Input/Output Input | Input, internal pullup enabled | Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. EXT_TRIGGER — PDB external trigger input. After reset, the default state is GPIOC3. |

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

| Signal Name | 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | Type | State During Reset | Signal Description |
|--|---------|---------|----------|---------|--|--------------------------------|---|
| ANB8 and PGA1+ and CMP0_M2 (GPIOC4) | 28 | 5 | 1 | 7 | Analog Input Input/Output | Analog Input | ANB8 and PGA1+ and CMP0_M2 — Analog input to channel 8 of ADCB and PGA1 positive input and negative input 2 of analog comparator 0. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. When used as an analog input, the signal goes to the ANB8 and PGA1+ and CMP0_M2. After reset, the default state is ANB8 and PGA1+ and CMP0_M2. |
| ANB6 and PGA1– and CMP0_P4 (GPIOC5) | 1 | 6 | 2 | 9 | Input/Output Analog Input | Analog Input | ANB6 and PGA1– and CMP0_P4 — Analog input to channel 6 of ADCB and PGA1 negative input and positive input 4 of analog comparator 0. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. When used as an analog input, the signal goes to the ANB6 and PGA1– and CMP0_P4. After reset, the default state is ANB6 and PGA1– and CMP0_P4. |
| ANB4 and CMP1_P1 (GPIOC6) (PWM2) | 2 | 7 | 3 | 11 | Analog Input Input/Output Output | Analog Input | ANB4 and CMP1_P1 — Analog input to channel 4 of ADCB and positive input 1 of analog comparator 1. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM2 — The PWM channel 2. When used as an analog input, the signal goes to the ANB4 and CMP1_P1. After reset, the default state is ANB4 and CMP1_P1. |
| GPIOC7 (ANB5 and CMP1_M2) | | | | 10 | Input/Output Analog Input | Input, internal pullup enabled | Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB5 and CMP1_M2 — Analog input to channel 5 of ADCB and negative input 2 of analog comparator 1. After reset, the default state is GPIOC7. |

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

| Signal Name | 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | Type | State During Reset | Signal Description |
|---|---------|---------|----------|---------|---|---|---|
| TDI (GPIOD0) (ANB12) (\overline{SS}) (TIN2) (CMP0_OUT) | 23 | 30 | 26 | 45 | Input Input/Output Analog Input Input Input Output | Input, internal pullup enabled | <p>Test Data Input — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pullup resistor.</p> <p>Port D GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>ANB12 — Analog input to channel 12 of ADCB</p> <p>\overline{SS} — \overline{SS} is used in slave mode to indicate to the SPI module that the current transfer is to be received.</p> <p>TIN2 — Dual timer module channel 2 input.</p> <p>CMP1_OUT — Analog comparator 1 output.</p> <p>After reset, the default state is TDI.</p> |
| TDO (GPIOD1) (ANB10) (T0) (CMP2_OUT) | 25 | 32 | 28 | 48 | Output Input/Output Analog Input Input/Output Output | Output, tri-stated, internal pullup enabled | <p>Test Data Output — This three-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK.</p> <p>Port D GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>ANB10 — Analog input to channel 10 of ADCB.</p> <p>T0 — Dual timer module channel 0 input/output.</p> <p>CMP2_OUT — Analog comparator 2 output.</p> <p>After reset, the default state is TDO.</p> |
| TCK (GPIOD2) (ANA4 and CMP1_P2) (CMP2_OUT) | 9 | 14 | 10 | 22 | Input Input/Output Analog Input Output | Input, internal pullup enabled | <p>Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity.</p> <p>Port D GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>ANA4 and CMP1_P2 — Analog input to channel 4 of ADCA and positive input 2 of analog comparator 1.</p> <p>CMP2_OUT — Analog comparator 2 output.</p> <p>After reset, the default state is TCK.</p> |

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

| Signal Name | 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | Type | State During Reset | Signal Description |
|--|---------|---------|----------|---------|---|--------------------------------|---|
| TMS (GPIOD3) (ANB11) (T1) (CMP1_OUT) | 24 | 31 | 27 | 47 | Input Input/Output Analog Input Input/Output Output | Input, internal pullup enabled | <p>Test Mode Select Input — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pullup resistor.</p> <p>Port D GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>ANB11 — Analog input to channel 11 of ADCB.</p> <p>T1 — Dual timer module channel 1 input/output.</p> <p>CMP1_OUT — Analog comparator 2 output.</p> <p>After reset, the default state is TMS.</p> <p>Always tie the TMS pin to VDD through a 2.2 kΩ resistor.</p> |
| GPIOE0 | | | | 5 | Input/Output | Input, internal pullup enabled | <p>Port E GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>After reset, the default state is GPIOE0.</p> |
| GPIOE1 (ANB9 and CMP0_P1) | | | | 6 | Input/Output Analog Input | Input, internal pullup enabled | <p>Port E GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>ANB9 and CMP0_P1 — Analog input to channel 9 of ADCB and positive input 1 of analog comparator 0.</p> <p>After reset, the default state is GPIOE1.</p> |
| GPIOE2 (ANB7 and CMP0_M1) | | | | 8 | Input/Output Analog Input | Input, internal pullup enabled | <p>Port E GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>ANB7 and CMP0_M1 — Analog input to channel 7 of ADCB and negative input 1 of analog comparator 0.</p> <p>After reset, the default state is GPIOE2.</p> |
| GPIOE3 (ANA10 and CMP2_M1) | | | | 14 | Input/Output Analog Input | Input, internal pullup enabled | <p>Port E GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>ANA10 and CMP2_M1 — Analog input to channel 10 of ADCA and negative input 1 of analog comparator 2.</p> <p>After reset, the default state is GPIOE3.</p> |
| GPIOE4 (ANA6 and CMP2_P2) | | | | 18 | Input/Output Analog Input | Input, internal pullup enabled | <p>Port E GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>ANA6 and CMP2_P2 — Analog input to channel 6 of ADCA and positive input 2 of analog comparator 2.</p> <p>After reset, the default state is GPIOE4.</p> |

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

| Signal Name | 28 SOIC | 32 LQFP | 32 PSDIP | 48 LQFP | Type | State During Reset | Signal Description |
|----------------------------------|---------|---------|----------|---------|--|---|---|
| GPIOE5 (ANA8 and CMP2_P1) | | | | 16 | Input/ Output Analog Input | Input, internal pullup enabled | Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA8 and CMP2_P1— Analog input to channel 8 of ADCA and positive input 1 of analog comparator 2. After reset, the default state is GPIOE5. |
| GPIOE6 | | | | 28 | Input/ Output | Input, internal pullup enable | Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is GPIOE6. |
| GPIOE7 (CMP1_M3) | | | | 34 | Input/ Output Analog Input | Input, internal pullup enabled | Port E GPIO — This GPIO pin can be individually programmed as an input or output pin CMP1_M3 — Analog input to both negative input 3 of analog comparator 1. After reset, the default state is GPIOE7. |
| GPIOF0 (XTAL) | 18 | 25 | 21 | 37 | Input/ Output Analog Input/ Output | Input, internal pullup enabled | Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. XTAL — External Crystal Oscillator Output. This output connects the internal crystal oscillator output to an external crystal or ceramic resonator. After reset, the default state is GPIOF0. |
| GPIOF1 (CMP1_P3) | | | | 40 | Input/ Output Analog Input | Input, internal pullup enabled | Port F GPIO — This GPIO pin can be individually programmed as an input or output pin CMP1_P3 — Analog input to both positive input 3 of analog comparator 1. After reset, the default state is GPIOF1 |
| GPIOF2 (CMP0_M3) | | | | 41 | Input/ Output Analog Input | Input, internal pullup enabled | Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. CMP0_M3 — Analog input to both negative input 3 of analog comparator 0. After reset, the default state is GPIOF2. |
| GPIOF3 (CMP0_P3) | | | | 42 | Input/ Output Analog Input | Input, internal pullup enabled | Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. CMP0_P3 — Analog input to both positive input 3 of analog comparator 0. After reset, the default state is GPIOF3. |

5 Memory Maps

5.1 Introduction

The 56F8006/56F8002 device is based on the 56800E core. It uses a dual Harvard-style architecture with two independent memory spaces for Data and Program. On-chip RAM is shared by both data and program spaces and flash memory is used only in program space.

This section provides memory maps for:

- Program address space, including the interrupt vector table
- Data address space, including the EOnCE memory and peripheral memory maps

On-chip memory sizes for the device are summarized in [Table 6](#). Flash memories' restrictions are identified in the "Use Restrictions" column of [Table 6](#).

Table 6. Chip Memory Configurations

| On-Chip Memory | 56F8006 | 56F8002 | Use Restrictions |
|------------------------|------------------------|------------------------|--|
| Program Flash (PFLASH) | 8K x 16 or 16 KB | 6K x 16 or 12 KB | Erase/program via flash interface unit and word writes to CDBW |
| Unified RAM (RAM) | 1K x 16 or 2 KB | 1K x 16 or 2 KB | Usable by the program and data memory spaces |

5.2 Program Map

The 56F8006/56F8002 series provide up to 16 KB on-chip flash memory. It primarily accesses through the program memory buses (PAB; PDB). PAB is used to select program memory addresses; instruction fetches are performed over PDB. Data can be read and written to program memory space through primary data memory buses: CDBW for data write and CDBR for data read. Accessing program memory space over the data memory buses takes longer access time compared to accessing data memory space. The special MOVE instructions are provided to support these accesses. The benefit is that non time critical constants or tables can be stored and accessed in program memory.

The program memory map is shown in [Table 7](#) and [Table 8](#).

Table 7. Program Memory Map¹ for 56F8006 at Reset

| Begin/End Address | Memory Allocation |
|------------------------------|---|
| P: 0x1F FFFF P: 0x00 8800 | RESERVED |
| P: 0x00 83FF P: 0x00 8000 | On-Chip RAM ² : 2 KB |
| P: 0x00 7FFF P: 0x00 2000 | RESERVED |
| P: 0x00 1FFF P: 0x00 0000 | <ul style="list-style-type: none"> • Internal program flash: 16 KB • Interrupt vector table locates from 0x00 0000 to 0x00 0065 • COP reset address = 0x00 0002 • Boot location = 0x00 0000 |

¹ All addresses are 16-bit word addresses.

² This RAM is shared with data space starting at address X: 0x00 0000; see [Figure 8](#).

Table 8. Program Memory Map¹ for 56F8002 at Reset (continued)

| Begin/End Address | Memory Allocation |
|------------------------------|---|
| P: 0x1F FFFF P: 0x00 8800 | RESERVED |
| P: 0x00 83FF P: 0x00 8000 | On-Chip RAM ² : 2 KB |
| P: 0x00 7FFF P: 0x00 2000 | RESERVED |
| P: 0x00 1FFF P: 0x00 0800 | <ul style="list-style-type: none"> • Internal program flash: 12 KB • Interrupt vector table locates from 0x00 0800 to 0x00 0865 • COP reset address = 0x00 0802 • Boot location = 0x00 0800 |
| P: 0x00 07FF P: 0x00 0000 | RESERVED |

¹ All addresses are 16-bit word addresses.

² This RAM is shared with data space starting at address X: 0x00 0000; see [Figure 9](#).

5.3 Data Map

The 56F8006/56F8002 series contain a dual access memory. It can be accessed from core primary data buses (XAB1; CDBW; CDBR) and secondary data buses (XAB2; XDB2). Addresses in data memory are selected on the XAB1 and XAB2 buses. Byte, word, and long data transfers occur on the 32-bit CDBR and CDBW buses. A second 16-bit read operation can be performed in parallel on the XDB2 bus.

Peripheral registers and on-chip JTAG/EOnCE controller registers are memory-mapped into data memory access. A special direct address mode is supported for accessing a first 64-location in data memory by using a single word instruction.

The data memory map is shown in [Table 9](#).

Table 9. Data Memory Map¹

| Begin/End Address | Memory Allocation |
|----------------------------|---|
| X:0xFF FFFF X:0xFF FF00 | EOnCE 256 locations allocated |
| X:0xFF FEFF X:0x01 0000 | RESERVED |
| X:0x00 FFFF X:0x00 F000 | On-Chip Peripherals 4096 locations allocated |
| X:0x00 EFFF X:0x00 8800 | RESERVED |
| X:0x00 87FF X:0x00 8000 | RESERVED |
| X:0x00 7FFF X:0x00 0400 | RESERVED |
| X:0x00 03FF X:0x00 0000 | On-Chip Data RAM 2 KB ² |

¹ All addresses are 16-bit word addresses.

² This RAM is shared with Program space starting at P: 0x00 8000. See [Figure 8](#) and [Figure 9](#).

On-chip RAM is also mapped into program space starting at P: 0x00 8000. This makes for easier online reprogramming of on-chip flash.

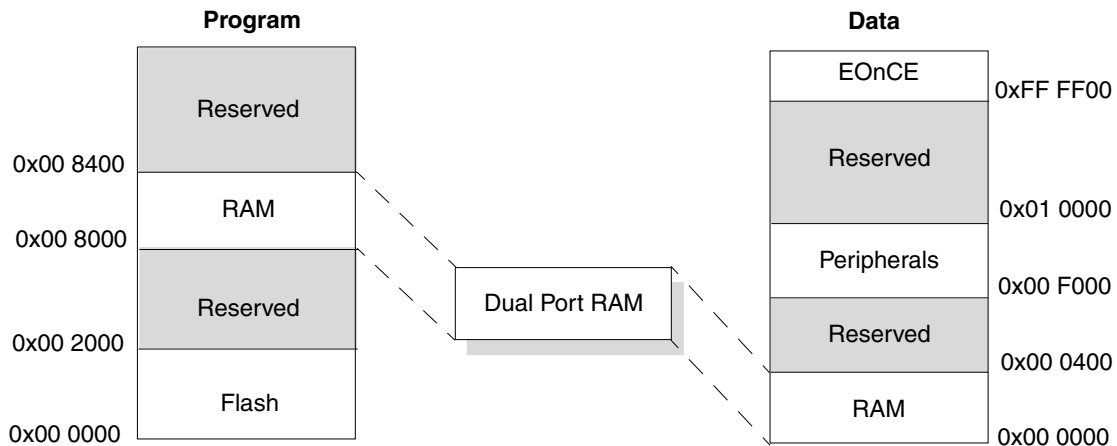


Figure 8. 56F8006 Dual Port RAM Map

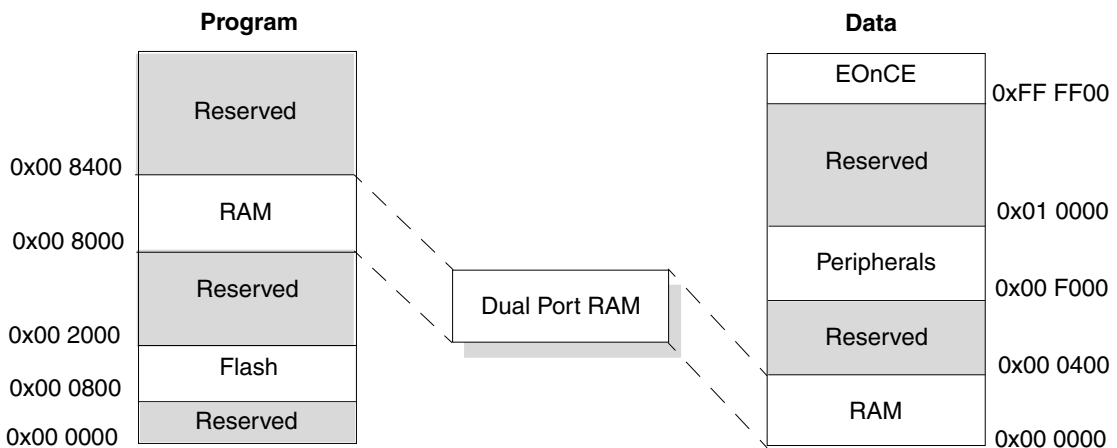


Figure 9. 56F8002 Dual Port RAM Map

5.4 Interrupt Vector Table and Reset Vector

The location of the vector table is determined by the vector base address register (VBA). The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower seven bits are determined based on the highest priority interrupt and are then appended onto VBA before presenting the full VAB to the core. Please see the *MC56F8006 Peripheral Reference Manual* for detail. The reset startup addresses of 56F8002 and 56F8006 are different.

- 56F8006 startup address is located at 0x00 0000. The reset value of VBA is reset to a value of 0x0000 that corresponds to address 0x00 0000
- 56F8002 startup address is located at 0x00 0800. The reset value of VBA is reset to a value of 0x0010 that corresponds to address 0x00 0800

By default, the chip reset address and COP reset address correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

The highest number vector, a user assignable vector USER6 (vector 50), can be defined as a fast interrupt if the instruction located in this vector location is not a JSR or BSR instruction. Please see section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for detail.

Table 43 provides the 56F8006/56F8002's reset and interrupt priority structure, including on-chip peripherals.

5.5 Peripheral Memory-Mapped Registers

The locations of on-chip peripheral registers are part of the data memory map on the 56800E series. These locations may be accessed with the same addressing modes used for ordinary data memory, except all peripheral registers should be read or written using word accesses only.

Table 10 summarizes the base addresses for the set of peripherals on the 56F8006/56F8002 devices. Peripherals are listed in order of the base address.

Table 10. Data Memory Peripheral Base Address Map Summary

| Peripheral | Prefix | Base Address |
|-------------------------------|------------------|--------------|
| Dual Channel Timer | TMR | X:0x00 F000 |
| PWM Module | PWM | X:0x00 F020 |
| Interrupt Controller | INTC | X:0x00 F040 |
| ADCA | ADCA | X:0x00 F060 |
| ADCB | ADCB | X:0x00 F080 |
| Programmable Gain Amplifier 0 | PGA0 | X:0x00 F0A0 |
| Programmable Gain Amplifier 1 | PGA1 | X:0x00 F0C0 |
| SCI | SCI | X:0x00 F0E0 |
| SPI | SPI | X:0x00 F100 |
| I ² C | I ² C | X:0x00 F120 |
| Computer Operating Properly | COP | X:0x00 F140 |
| On-Chip Clock Synthesis | OCCS | X:0x00 F160 |
| GPIO Port A | GPIOA | X:0x00 F180 |
| GPIO Port B | GPIOB | X:0x00 F1A0 |
| GPIO Port C | GPIOC | X:0x00 F1C0 |
| GPIO Port D | GPIOD | X:0x00 F1E0 |
| GPIO Port E | GPIOE | X:0x00 F200 |
| GPIO Port F | GPIOF | X:0x00 F220 |
| System Integration Module | SIM | X:0x00 F240 |
| Power Management Controller | PMC | X:0x00 F260 |
| Analog Comparator 0 | CMP0 | X:0x00 F280 |
| Analog Comparator 1 | CMP1 | X:0x00 F2A0 |
| Analog Comparator 2 | CMP2 | X:0x00 F2C0 |
| Programmable Interval Timer | PIT | X:0x00 F2E0 |
| Programmable Delay Block | PDB | X:0x00 F300 |
| Real Timer Clock | RTC | X:0x00 F320 |
| Flash Memory Interface | FM | X:0x00 F400 |

5.6 EOnCE Memory Map

Control registers of the EOnCE are located at the top of data memory space. These locations are fixed by the 56F800E core. These registers can also be accessed through JTAG port if flash security is not set. [Table 11](#) lists all EOnCE registers necessary to access or control the EOnCE.

Table 11. EOnCE Memory Map

| Address | Register Acronym | Register Name |
|------------------------------|---------------------------|---|
| X:0xFF FFFF | OTX1/ORX1 | Transmit Register Upper Word Receive Register Upper Word |
| X:0xFF FFFE | OTX/ORX (32 bits) | Transmit Register Receive Register |
| X:0xFF FFFD | OTXRCSR | Transmit and Receive Status and Control Register |
| X:0xFF FFFC | OCLSR | Core Lock/Unlock Status Register |
| X:0xFF FFFB– X:0xFF FFA1 | | Reserved |
| X:0xFF FFA0 | OCR | Control Register |
| X:0xFF FF9F– X:0xFF FF9E | OSCNR (24 bits) | Instruction Step Counter |
| X:0xFF FF9D | OSR | Status Register |
| X:0xFF FF9C | OBASE | Peripheral Base Address Register |
| X:0xFF FF9B | OTBCR | Trace Buffer Control Register |
| X:0xFF FF9A | OTBPR | Trace Buffer Pointer Register |
| X:0xFF FF99– X:0xFF FF98 | OTB (21–24 bits/stage) | Trace Buffer Register Stages |
| X:0xFF FF97– X:0xFF FF96 | OBCR (24 bits) | Breakpoint Unit Control Register |
| X:0xFF FF95– X:0xFF FF94 | OBAR1 (24 bits) | Breakpoint Unit Address Register 1 |
| X:0xFF FF93– X:0xFF FF92 | OBAR2 (32 bits) | Breakpoint Unit Address Register 2 |
| X:0xFF FF91– X:0xFF FF90 | OBMSK (32 bits) | Breakpoint Unit Mask Register 2 |
| X:0xFF FF8F | | Reserved |
| X:0xFF FF8E | OBCNTR | EOnCE Breakpoint Unit Counter |
| X:0xFF FF8D | | Reserved |
| X:0xFF FF8C | | Reserved |
| X:0xFF FF8B | | Reserved |
| X:0xFF FF8A | OESCR | External Signal Control Register |
| X:0xFF FF89 – X:0xFF FF00 | | Reserved |

6 General System Control Information

6.1 Overview

This section discusses power pins, reset sources, interrupt sources, clock sources, the system integration module (SIM), ADC synchronization, and JTAG/EOnCE interfaces.

6.2 Power Pins

V_{DD} , V_{SS} and V_{DDA} , V_{SSA} are the primary power supply pins for the devices. This voltage source supplies power to all on-chip peripherals, I/O buffer circuitry and to internal voltage regulators. Device has multiple internal voltages provide regulated lower-voltage source for the peripherals, core, memory, and on-chip relaxation oscillators.

Typically, there are at least two separate capacitors across the power pins to bypass the glitches and provide bulk charge storage. In this case, there should be a bulk electrolytic or tantalum capacitor, such as a 10 μF tantalum capacitor, to provide bulk charge storage for the overall system and a 0.1 μF ceramic bypass capacitor located as near to the device power pins as practical to suppress high-frequency noise. Each pin must have a bypass capacitor for best noise suppression.

V_{DDA} and V_{SSA} are the analog power supply pins for the device. This voltage source supplies power to the ADC, PGA, and CMP modules. A 0.1 μF ceramic bypass capacitor should be located as near to the device V_{DDA} and V_{SSA} pins as practical to suppress high-frequency noise. V_{DDA} and V_{SSA} are also the voltage reference high and voltage reference low inputs, respectively, for the ADC module.

6.3 Reset

Resetting the device provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values and the program counter is loaded from the reset vector. On-chip peripheral modules are disabled and I/O pins are initially configured as the reset status shown in [Table 5](#). The 56F8006/56F8002 has the following sources for reset:

- Power-on reset (POR)
- Partial power down reset (PPD)
- Low-voltage detect (LVD)
- External pin reset (EXTR)
- Computer operating properly loss of reference reset (COP_LOR)
- Computer operating properly time-out reset (COP_CPU)
- Software Reset (SWR)

Each of these sources has an associated bit in the reset status register (RSTAT) in the system integration module (SIM).

The external pin reset function is shared with an GPIO port A7 on the $\overline{\text{RESET}}$ /GPIOA7 pin. The reset function is enabled following any reset of the device. Bit 7 of GPIOA_PER register must be cleared to use this pin as an GPIO port pin. When enabled as the $\overline{\text{RESET}}$ pin, an internal pullup device is automatically enabled.

6.4 On-chip Clock Synthesis

The on-chip clock synthesis (OCCS) module allows designers using an internal relaxation oscillator, an external crystal, or an external clock to run 56F8000 family devices at user-selectable frequencies up to 32 MHz.

The features of OCCS module include:

- Ability to power down the internal relaxation oscillator or crystal oscillator
- Ability to put the internal relaxation oscillator into standby mode
- Ability to power down the PLL

- Provides a 3X system clock that operates at three times the system clock to PWM, timer, and SCI modules
- Safety shutdown feature is available if the PLL reference clock is lost
- Can be driven from an external clock source

The clock generation module provides the programming interface for the PLL, internal relaxation oscillator, and crystal oscillator. It also provides a postscaler to divide clock frequency down by 1, 2, 4, 8, 16, 32, 64, 128, 256 before feeding to the SIM. The SIM is responsible for further dividing these frequencies by two, which ensures a 50% duty cycle in the system clock output. For detail, see the OCCS chapter in the *MC56F8006 Peripheral Reference Manual*.

6.4.1 Internal Clock Source

An internal relaxation oscillator can supply the reference frequency when an external frequency source or crystal is not used. It is optimized for accuracy and programmability while providing several power-saving configurations that accommodate different operating conditions. The internal relaxation oscillator has little temperature and voltage variability. To optimize power, the internal relaxation oscillator supports a run state (8 MHz), standby state (400 kHz), and a power-down state.

During a boot or reset sequence, the relaxation oscillator is enabled by default (the PRECS bit in the PLLCR word is set to 0). Application code can then also switch to the external clock source and power down the internal oscillator, if desired. If a changeover between internal and external clock sources is required at power-on, ensure that the clock source is not switched until the desired external clock source is enabled and stable.

To compensate for variances in the device manufacturing process, the accuracy of the relaxation oscillator can be incrementally adjusted to within + 0.078% of 8 MHz by trimming an internal capacitor. Bits 0–9 of the OSCTL (oscillator control) register allow you to set in an additional offset (trim) to this preset value to increase or decrease capacitance. Each unit added or subtracted changes the output frequency by about 0.078% of 8 MHz, allowing incremental adjustment until the desired frequency accuracy is achieved.

The center frequency of the internal oscillator is calibrated at the factory to 8 MHz and the TRIM value is stored in the flash information block and loaded to the FMOPT1 register at reset. When using the relaxation oscillator, the boot code should read the FMOPT1 register and set this value as OSCTL TRIM. For further information, see the *MC56F8006 Peripheral Reference Manual*.

6.4.2 Crystal Oscillator/Ceramic Resonator

The internal crystal oscillator circuit is designed to interface with a parallel-resonant crystal resonator in the frequency range, specified for the external crystal, of 32.768 kHz (Typ) or 1–16 MHz. A ceramic resonator can be substituted for the 1–16 MHz range. When used to supply a source to the internal PLL, the recommended crystal/resonator is in the 4 MHz to 8 MHz (recommend 8 MHz) range to achieve optimized PLL performance. Oscillator circuits are shown in [Figure 10](#), [Figure 11](#), and [Figure 12](#). Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances. The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time. When using low-frequency, low-power mode, the only external component is the crystal itself. In the other oscillator modes, load capacitors (C_x , C_y) and feedback resistor (R_F) are required. In addition, a series resistor (R_S) may be used in high-gain modes. Recommended component values are listed in [Table 28](#).

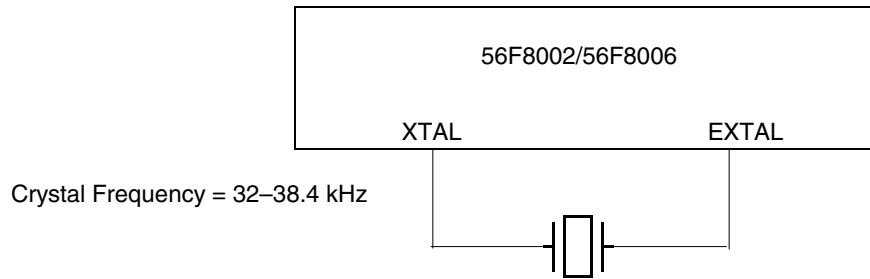


Figure 10. Typical Crystal Oscillator Circuit: Low-Range, Low-Power Mode

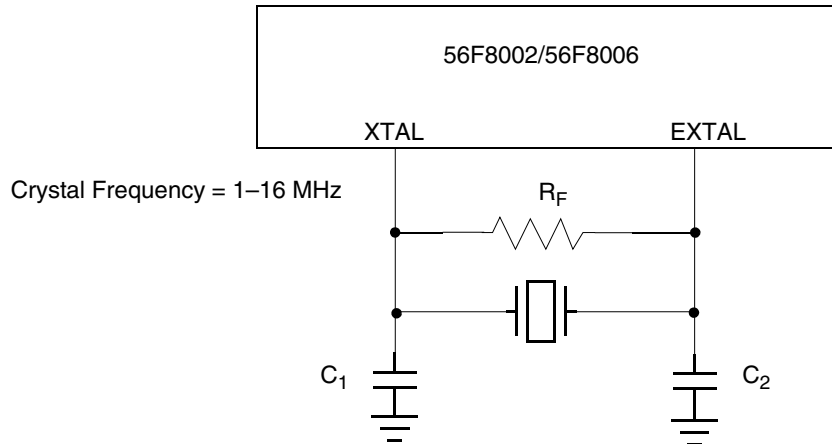


Figure 11. Typical Crystal or Ceramic Resonator Circuit: High-Range, Low-Power Mode

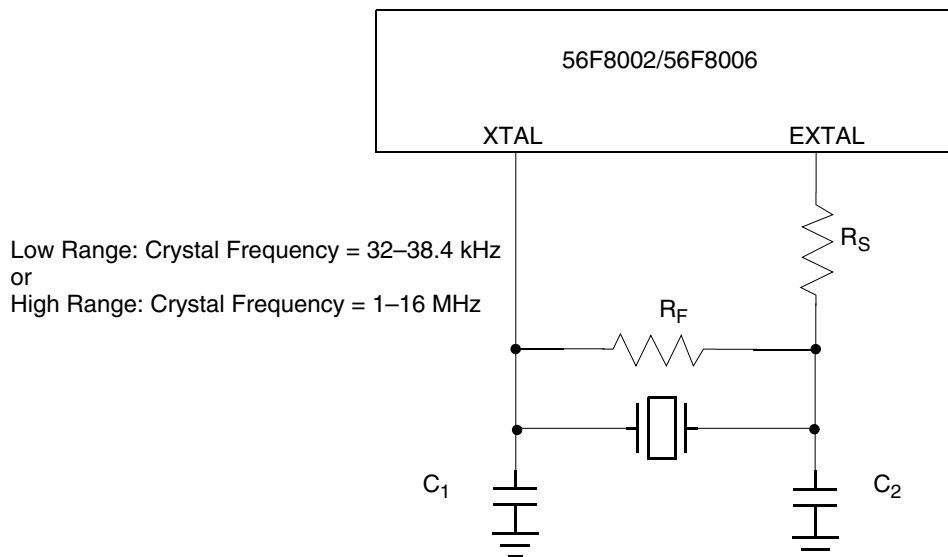


Figure 12. Typical Crystal or Ceramic Resonator Circuit: Low Range and High Range, High-Gain Mode

6.4.3 External Clock Input — Crystal Oscillator Option

The recommended method of connecting an external clock is illustrated in [Figure 13](#). The external clock source is connected to XTAL and the EXTAL pin is grounded or configured as GPIO while CLK_MOD bit in OSCTL register is set. The external clock input must be generated using a relatively low impedance driver with maximum frequency less than 8 MHz.

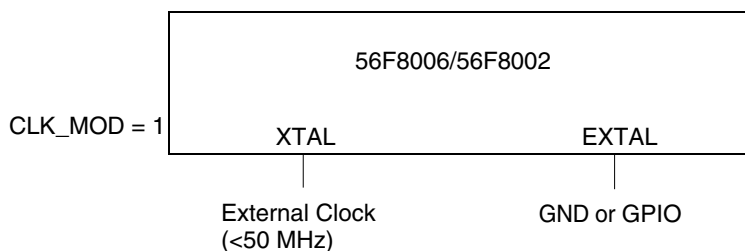


Figure 13. Connecting an External Clock Signal Using XTAL

6.4.4 Alternate External Clock Input

The recommended method of connecting an external clock is illustrated in Figure 14. The external clock source is connected to GPIOB6/RXD/SDA/ANA13 and CMP0_P2/CLKIN while EXT_SEL bit in OSCTL register is set and corresponding bits in GPIOB_PER register GPIO module and GPSB1 register in the system integration module (SIM) are set to the correct values. The external clock input must be generated using a relatively low impedance driver with maximum frequency not greater than 64 MHz.

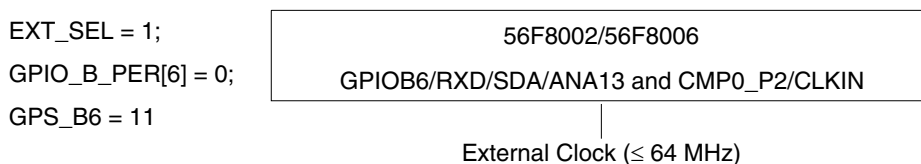


Figure 14. Connecting an External Clock Signal Using GPIO

6.5 Interrupt Controller

The 56F8006/56F8002 interrupt controller (INTC) module arbitrates the various interrupt requests (IRQs). The INTC signals to the 56800E core when an interrupt of sufficient priority exists and what address to jump to to service this interrupt.

The interrupt controller contains registers that allow up to three interrupt sources to be set to priority level 1 and other up to three interrupt sources to be set to priority level 2. By default, all peripheral interrupt sources are set to priority level 0. Next, all of the interrupt requests of a given level are priority encoded to determine the lowest numeric value of the active interrupt requests for that level. Within a given priority level, the lowest vector number is the highest priority and the highest vector number is the lowest.

The highest vector number, a user assignable vector USER6 (vector 50), can be defined as a fast interrupt if the instruction located in this vector location is not a JSR or BSR instruction. Please see section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for detail.

6.6 System Integration Module (SIM)

The SIM module is a system catchall for the glue logic that ties together the system-on-chip. It controls distribution of resets and clocks and provides a number of control features including the pin muxing control; inter-module connection control (for example connecting comparator output to PWM fault input); individual peripheral enable/disable; PWM, timer, and SCI clock rate control; enabling peripheral operation in stop mode; port configuration overwrite protection. For further information, see the *MC56F8006 Peripheral Reference Manual*.

The SIM is responsible for the following functions:

- Chip reset sequencing
- Core and peripheral clock control and distribution
- Stop/wait mode control
- System status control

General System Control Information

- Registers containing the JTAG ID of the chip
- Controls for programmable peripheral and GPIO connections
- Peripheral clocks for TMR and PWM and SCI with a high-speed (3X) option
- Power-saving clock gating for peripherals
- Controls the enable/disable functions of large regulator standby mode with write protection capability
- Permits selected peripherals to run in stop mode to generate stop recovery interrupts
- Controls for programmable peripheral and GPIO connections
- Software chip reset
- I/O short address base location control
- Peripheral protection control to provide runaway code protection for safety-critical applications
- Controls output of internal clock sources to CLKO pin
- Four general-purpose software control registers are reset only at power-on
- Peripherals stop mode clocking control

6.7 PWM, PDB, PGA, and ADC Connections

The comparators, timers, and PWM_reload_sync output can be connected to the programmable delay block (PDB) trigger input. The PDB pre-trigger A and trigger A outputs are connected to the ADCA and PGA0 hardware trigger inputs. The PDB pre-trigger B and trigger B outputs are connected to the ADCB and PGA1 hardware trigger inputs. When the input trigger of PDB is asserted, PDB trigger and pre-trigger outputs are asserted after a delay of a pre-programmed period. See the *MC56F8006 Peripheral Reference Manual* for additional information.

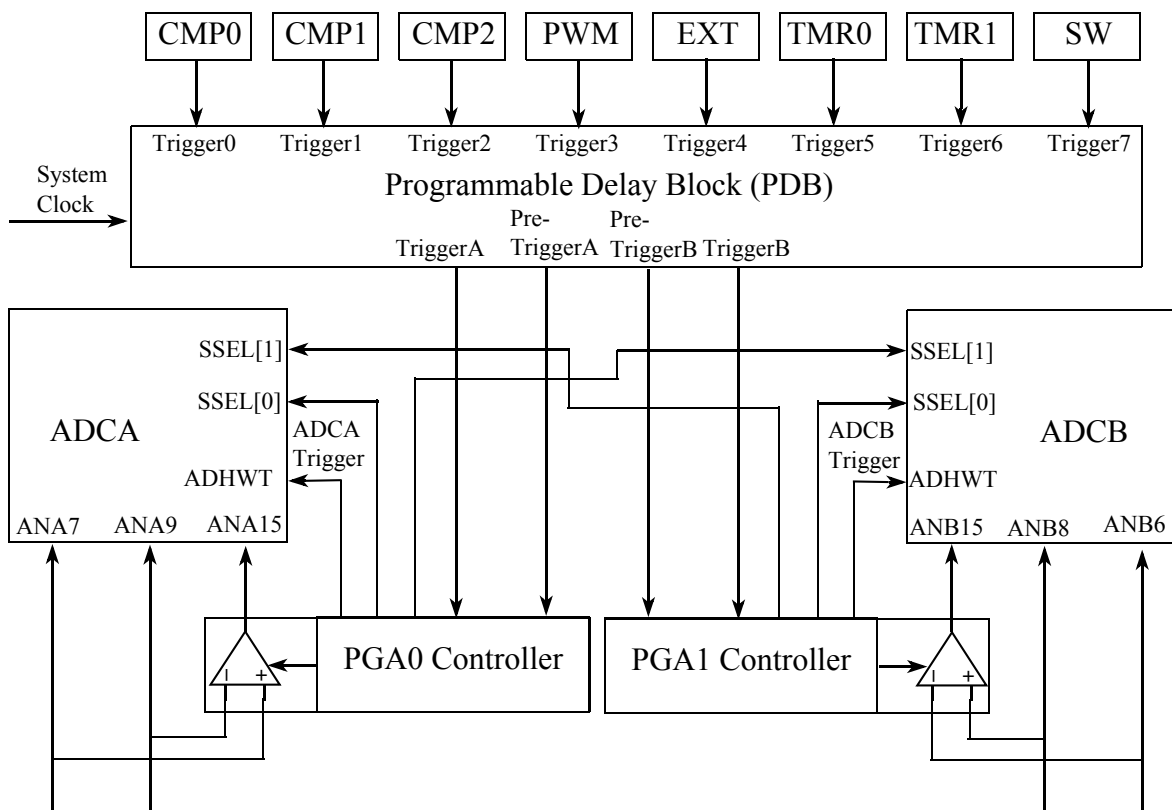


Figure 15. Synchronization of ADC, PDB

Each ADC contains a temperature sensor. Outputs of temperature sensors, PGAs, on-chip regulators and VDDA are internally routed to ADC inputs.

- Internal PGA0 output available on ANA15
- Internal PGA0 positive input calibration voltage available on ANA16
- Internal PGA0 negative input calibration voltage available on ANA17
- Internal PGA1 output available on ANB15
- Internal PGA1 positive input calibration voltage available on ANB16
- Internal PGA1 negative input calibration voltage available on ANB17
- ADCA temperature sensor available on ANA26
- ADCB temperature sensor available on ANB26
- Output of on-chip digital voltage regulator is routed to ANA24
- Output of on-chip analog voltage regulator is routed to ANA25
- Output of on-chip small voltage regulator for ROSC is routed to ANB24
- Output of on-chip small voltage regulator for PLL is routed to ANB25
- VDDA is routed to ANA27 and ANB27

6.8 Joint Test Action Group (JTAG)/Enhanced On-Chip Emulator (EOnCE)

The DSP56800E Family includes extensive integrated support for application software development and real-time debugging. Two modules, the Enhanced On-Chip Emulation module (EOnCE) and the core test access port (TAP, commonly called the JTAG port), work together to provide these capabilities. Both are accessed through a common 4-pin JTAG/EOnCE interface. These modules allow you to insert the 56F8006/56F8002 into a target system while retaining debug control. This capability is especially important for devices without an external bus, because it eliminates the need for a costly cable to bring out the footprint of the chip, as is required by a traditional emulator system.

The DSP56800E EOnCE module is a Freescale-designed module used to develop and debug application software used with the chip. This module allows non-intrusive interaction with the CPU and is accessible through the pins of the JTAG interface or by software program control of the DSP56800E core. Among the many features of the EOnCE module is the support for data communication between the controller and the host software development and debug systems in real-time program execution. Other features allow for hardware breakpoints, the monitoring and tracking of program execution, and the ability to examine and modify the contents of registers, memory, and on-chip peripherals, all in a special debug environment. No user-accessible resources need to be sacrificed to perform debugging operations.

The DSP56800E JTAG port is used to provide an interface for the EOnCE module to the DSP JTAG pins. Joint Test Action Group (JTAG) boundary scan is an IEEE 1149.1 standard methodology enabling access to test features using a test access port (TAP). A JTAG boundary scan consists of a TAP controller and boundary scan registers. Please contact your Freescale sales representative or authorized distributor for device-specific BSDL information.

NOTE

In normal operation, an external pullup on the TMS pin is highly recommend to place the JTAG state machine in reset state if this pin is not configured as GPIO.

7 Security Features

The 56F8006/56F8002 offers security features intended to prevent unauthorized users from reading the contents of the flash memory (FM) array. The 56F8006/56F8002's flash security consists of several hardware interlocks that prevent unauthorized users from gaining access to the flash array.

After flash security is set, an authorized user can be enabled to access on-chip memory if a user-defined software subroutine, which reads and transfers the contents of internal memory via peripherals, is included in the application software. This

application software could communicate over a serial port, for example, to validate the authenticity of the requested access, then grant it until the next device reset. The inclusion of such a back door technique is at the discretion of the system designer.

7.1 Operation with Security Enabled

After you have programmed flash with the application code, or as part of the programming of the flash with the application code, the 56F8006/56F8002 can be secured by programming the security word, 0x0002, into program memory location 0x001FF7. This can also be effected by use of the CodeWarrior IDE menu flash lock command. This nonvolatile word keeps the device secured after reset, caused, for example, by a power-down of the device. Refer to the flash memory chapter in the *MC56F8006 Peripheral Reference Manual* for detail. When flash security mode is enabled, the 56F8006/56F8002 disables the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

7.2 Flash Access Lock and Unlock Mechanisms

There are several methods that effectively lock or unlock the on-chip flash.

7.2.1 Disabling EOnCE Access

On-chip flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E CPU. The TCK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (test access port) is active and provides the chip's boundary scan capability and access to the ID register, but proper implementation of flash security blocks any attempt to access the internal flash memory via the EOnCE port when security is enabled. This protection is effective when the device comes out of reset, even prior to the execution of any code at startup.

7.2.2 Flash Lockout Recovery Using JTAG

If the device is secured, one lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared). This does not compromise security, as the entire contents of your secured code stored in flash are erased before security is disabled on the device on the next reset or power-up sequence.

To start the lockout recovery sequence via JTAG, the JTAG public instruction (LOCKOUT_RECOVERY) must first be shifted into the chip-level TAP controller's instruction register. After the LOCKOUT_RECOVERY instruction has been shifted into the instruction register, the clock divider value must be shifted into the corresponding 7-bit data register. After the data register has been updated, you must transition the TAP controller into the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence is complete. Refer to the *MC56F8006 Peripheral Reference Manual* for detail, or contact Freescale.

NOTE

After the lockout recovery sequence has completed, you must reset the JTAG-TAP controller and device to return to normal unsecured operation. Power-on reset resets both too.

7.2.3 Flash Lockout Recovery Using CodeWarrior

CodeWarrior can unlock a device by selecting the *Debug* menu, then selecting *DSP56800E*, followed by *Unlock Flash*. Another mechanism is also built into CodeWarrior using the device's memory configuration file. The command "*Unlock_Flash_on_Connect 1*" in the *.cfg* file accomplishes the same task as using the *Debug* menu.

This lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared).

7.2.4 Flash Lockout Recovery without Mass Erase

7.2.4.1 Without Presenting Back Door Access Keys to the Flash Unit

A user can un-secure a secured device by programming the word 0x0000 into program flash location 0x00 1FF7. After completing the programming, the JTAG TAP controller and the device must be reset to return to normal unsecured operation.

You are responsible for directing the device to invoke the flash programming subroutine to reprogram the word 0x0000 into program flash location 0x00 1FF7. This is done by, for example, toggling a specific pin or downloading a user-defined key through serial interfaces.

NOTE

Flash contents can be programmed only from 1s to 0s.

7.2.4.2 Presenting Back Door Access Key to the Flash Unit

It is possible to temporarily bypass the security through a back door access scheme, using a 4-word key, to temporarily unlock of the flash. A back door access requires support from the embedded software. This software would typically permit an external user to enter a four word code through one of the communications interfaces and then use it to attempt the unlock sequence. If your input matches the four word code stored at location 0x00 1FFC–0x00 1FFF in the flash memory, the part immediately becomes unsecured (at runtime) and you can access internal memory via JTAG/EOnCE port. Refer to the *MC56F8006 Peripheral Reference Manual* for detail. The key must be entered in four consecutive accesses to the flash, so this routine should be designed to run in RAM.

7.3 Product Analysis

The recommended method of unsecuring a secured device for product analysis of field failures is via the method described in [Section 7.2.4.2, “Presenting Back Door Access Key to the Flash Unit.”](#) The customer would need to supply technical support with the details of the protocol to access the subroutines in flash memory. An alternative method for performing analysis on a secured device would be to mass-erase and reprogram the flash with the original code, but modify the security word or not program the security word.

8 Specifications

8.1 General Characteristics

The 56F8006/56F8002 is fabricated in high-density low power and low leakage CMOS with a maximum voltage of 3.6 V digital inputs during normal operation without causing damage.

Absolute maximum ratings in [Table 12](#) are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of –40°C to 105°C ambient temperature over the following supply ranges: $V_{SS} = V_{SSA} = 0V$, $V_{DD} = V_{DDA} = 3.0\text{--}3.6 V$, $CL \leq 50 pF$, $f_{OP} = 32 MHz$

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

8.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified Table 12 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 12. Absolute Maximum Ratings

($V_{SS} = 0\text{ V}$, $V_{SSA} = 0\text{ V}$)

| Characteristic | Symbol | Notes | Min | Max | Unit |
|--|-----------------|-----------------|------|--------------|------|
| Supply Voltage Range | V_{DD} | | -0.3 | 3.8 | V |
| Analog Supply Voltage Range | V_{DDA} | | -0.3 | 3.6 | V |
| Voltage difference V_{DD} to V_{DDA} | ΔV_{DD} | | -0.3 | 0.3 | V |
| Voltage difference V_{SS} to V_{SSA} | ΔV_{SS} | | -0.3 | 0.3 | V |
| Digital Input Voltage Range | V_{IN} | Pin Groups 1, 2 | -0.3 | $V_{DD}+0.3$ | V |
| Oscillator Voltage Range | V_{OSC} | Pin Group 4 | TBD | TBD | V |
| Analog Input Voltage Range | V_{INA} | Pin Group 3 | -0.3 | 3.6 | V |
| Input clamp current, per pin ($V_{IN} < 0$) ^{1 2 3} | V_{IC} | | — | -25.0 | mA |
| Output clamp current, per pin ($V_O < 0$) ^{1 2 3} | V_{OC} | | — | -20.0 | mA |
| Output Voltage Range (Normal Push-Pull mode) | V_{OUT} | Pin Group 1 | -0.3 | V_{DD} | V |
| Ambient Temperature Industrial | T_A | | -40 | 105 | °C |
| Storage Temperature Range (Extended Industrial) | T_{STG} | | -55 | 150 | °C |

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{IN} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} loads shunt current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present or if the clock rate is low (which would reduce overall power consumption).

8.2.1 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 13. ESD and Latch-up Test Conditions

| Model | Description | Symbol | Value | Unit |
|------------|-----------------------------|--------|-------|----------|
| Human Body | Series Resistance | R1 | 1500 | Ω |
| | Storage Capacitance | C | 100 | pF |
| | Number of Pulses per Pin | — | 3 | |
| Machine | Series Resistance | R1 | 0 | Ω |
| | Storage Capacitance | C | 200 | pF |
| | Number of Pulses per Pin | — | 3 | |
| Latch-up | Minimum Input Voltage Limit | | -2.5 | V |
| | Maximum Input Voltage Limit | | 7.5 | V |

Table 14. 56F8006/56F8002 ESD Protection

| Characteristic ¹ | Min | Typ | Max | Unit |
|--|-----------|-----|-----|------|
| ESD for Human Body Model (HBM) | 2000 | — | — | V |
| ESD for Machine Model (MM) | 200 | — | — | V |
| ESD for Charge Device Model (CDM) | 750 | — | — | V |
| Latch-up current at $T_A = 85^\circ\text{C}$ (I_{LAT}) | ± 100 | | | mA |

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

8.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 15. 28SOIC Package Thermal Characteristics

| Characteristic | Comments | Symbol | Value (LQFP) | Unit |
|---|----------------------------|------------------|--------------|--------------------|
| Junction to ambient Natural convection | Single layer board (1s) | $R_{\theta JA}$ | 70 | $^\circ\text{C/W}$ |
| Junction to ambient Natural convection | Four layer board (2s2p) | $R_{\theta JMA}$ | 47 | $^\circ\text{C/W}$ |
| Junction to ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 55 | $^\circ\text{C/W}$ |

Table 15. 28SOIC Package Thermal Characteristics (continued)

| Characteristic | Comments | Symbol | Value (LQFP) | Unit |
|-----------------------------------|-------------------------|------------------|--------------|------|
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 42 | °C/W |
| Junction to board | | $R_{\theta JB}$ | 23 | °C/W |
| Junction to case | | $R_{\theta JC}$ | 26 | °C/W |
| Junction to package top | Natural Convection | Ψ_{JT} | 9 | °C/W |

Table 16. 32LQFP Package Thermal Characteristics

| Characteristic | Comments | Symbol | Value (LQFP) | Unit |
|--|-------------------------|------------------|--------------|------|
| Junction to ambient Natural convection | Single layer board (1s) | $R_{\theta JA}$ | 84 | °C/W |
| Junction to ambient Natural convection | Four layer board (2s2p) | $R_{\theta JMA}$ | 56 | °C/W |
| Junction to ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 70 | °C/W |
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 49 | °C/W |
| Junction to board | | $R_{\theta JB}$ | 33 | °C/W |
| Junction to case | | $R_{\theta JC}$ | 20 | °C/W |
| Junction to package top | Natural convection | Ψ_{JT} | 4 | °C/W |

Table 17. 32PSDIP Package Thermal Characteristics

| Characteristic | Comments | Symbol | Value (LQFP) | Unit |
|--|-------------------------|------------------|--------------|------|
| Junction to ambient Natural convection | Single layer board (1s) | $R_{\theta JA}$ | 56 | °C/W |
| Junction to ambient Natural convection | Four layer board (2s2p) | $R_{\theta JMA}$ | 41 | °C/W |
| Junction to ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 45 | °C/W |
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 36 | °C/W |
| Junction to board | | $R_{\theta JB}$ | 18 | °C/W |
| Junction to case | | $R_{\theta JC}$ | 24 | °C/W |
| Junction to package top | Natural convection | Ψ_{JT} | 10 | °C/W |

Table 18. 48LQFP Package Thermal Characteristics

| Characteristic | Comments | Symbol | Value (LQFP) | Unit |
|---|----------------------------|------------------|--------------|------|
| Junction to ambient Natural convection | Single layer board (1s) | $R_{\theta JA}$ | 79 | °C/W |
| Junction to ambient Natural convection | Four layer board (2s2p) | $R_{\theta JMA}$ | 55 | °C/W |
| Junction to ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 66 | °C/W |
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 48 | °C/W |
| Junction to board | | $R_{\theta JB}$ | 34 | °C/W |
| Junction to case | | $R_{\theta JC}$ | 20 | °C/W |
| Junction to package top | Natural Convection | Ψ_{JT} | 4 | °C/W |

NOTE

Junction-to-ambient thermal resistance determined per JEDEC JESD51–3 and JESD51–6. Thermal test board meets JEDEC specification for this package.

Junction-to-board thermal resistance determined per JEDEC JESD51–8. Thermal test board meets JEDEC specification for the specified package.

Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51–2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

See [Section 9.1, “Thermal Design Considerations,”](#) for more detail on thermal design considerations.

8.4 Recommended Operating Conditions

This section includes information about recommended operating conditions.

Table 19. Recommended Operating Conditions
 $(V_{REFLx} = 0\text{ V}, V_{SSA} = 0\text{ V}, V_{SS} = 0\text{ V})$

| Characteristic | Symbol | Notes | Min | Typ | Max | Unit |
|--|-------------------|--|--------|-----|-----------------|--------|
| Supply voltage | V_{DD}, V_{DDA} | | 3 | 3.3 | 3.6 | V |
| Voltage difference V_{DD} to V_{DDA} | ΔV_{DD} | | -0.1 | 0 | 0.1 | V |
| Voltage difference V_{SS} to V_{SSA} | ΔV_{SS} | | -0.1 | 0 | 0.1 | V |
| Device Clock Frequency Using relaxation oscillator Using external clock source | FSYSCLK | | 1 0 | | 32 32 | MHz |
| Input Voltage High (digital inputs) | V_{IH} | Pin Groups 1, 2 | 2.0 | | V_{DD} | V |
| Input Voltage Low (digital inputs) | V_{IL} | Pin Groups 1, 2 | -0.3 | | 0.8 | V |
| Oscillator Input Voltage High XTAL driven by an external clock source | V_{IHOSC} | Pin Group 4 | 2.0 | | $V_{DDA} + 0.3$ | V |
| Oscillator Input Voltage Low | V_{ILOSC} | Pin Group 4 | -0.3 | | 0.8 | V |
| Output Source Current High at $V_{OH\ min.}$ ¹ When programmed for low drive strength When programmed for high drive strength | I_{OH} | Pin Group 1 Pin Group 1 | — — | | -4 -8 | mA |
| Output Source Current Low (at $V_{OL\ max.}$) ¹ When programmed for low drive strength When programmed for high drive strength | I_{OL} | Pin Groups 1, 2 Pin Groups 1, 2 | — — | | 4 8 | mA |
| Ambient Operating Temperature (Extended Industrial) | T_A | | -40 | | 105 | °C |
| Flash Endurance (Program Erase Cycles) | N_F | $T_A = -40^\circ\text{C}$ to 125°C | 10,000 | | — | cycles |
| Flash Data Retention | t_R | $T_J \leq 85^\circ\text{C}$ avg | 15 | | — | years |
| Flash Data Retention with <100 Program/Erase Cycles | t_{FLRET} | $T_J \leq 85^\circ\text{C}$ avg | 20 | — | — | years |

¹ Total chip source or sink current cannot exceed 75 mA.

Table 20. Default Mode

| | |
|--------------------|---|
| Pin Group 1 | GPIO, TDI, TDO, TMS, TCK |
| Pin Group 2 | SCL, SDA |
| Pin Group 3 | ADC and Comparator Analog Inputs and PGA Inputs |
| Pin Group 4 | XTAL, EXTAL |

8.5 DC Electrical Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 21. DC Characteristics

| Characteristic | Symbol | Condition | Min | Typ ¹ | Max | Unit | Ambient temperature operating range |
|---|-------------------|---|------------------------|------------------|------------------------|------|-------------------------------------|
| Operating Voltage | | | 1.8 ² | | 3.6 | V | -40 °C ~ +125 °C |
| Output high voltage All I/O pins, low-drive strength All I/O pins, high-drive strength | V _{OH} | 1.8 V, I _{Load} = -2 mA | V _{DD} - 0.5 | — | — | V | |
| | | 2.7 V, I _{Load} = -10 mA | V _{DD} - 0.5 | — | — | V | |
| | | 2.3 V, I _{Load} = -6 mA | V _{DD} - 0.5 | — | — | V | |
| | | 1.8 V, I _{Load} = -3 mA | V _{DD} - 0.5 | — | — | V | |
| Output high current Max total I _{OH} for all ports | I _{OHT} | | — | — | 100 | mA | |
| Output low voltage All I/O pins, low-drive strength All I/O pins, high-drive strength | V _{OL} | 1.8 V, I _{Load} = 2 mA | — | — | 0.5 | V | |
| | | 2.7 V, I _{Load} = 10 mA | — | — | 0.5 | V | |
| | | 2.3 V, I _{Load} = 6 mA | — | — | 0.5 | V | |
| | | 1.8 V, I _{Load} = 3 mA | — | — | 0.5 | V | |
| Output low current Max total I _{OL} for all ports | I _{OLT} | | — | — | 100 | mA | |
| Input high voltage all digital inputs | V _{IH} | V _{DD} > 2.7 V | 0.70 x V _{DD} | — | — | V | |
| | | V _{DD} > 1.8 V | 0.85 x V _{DD} | — | — | V | |
| Input low voltage all digital inputs | V _{IL} | V _{DD} > 2.7 V | — | — | 0.35 x V _{DD} | V | |
| | | V _{DD} > 1.8 V | — | — | 0.30 x V _{DD} | V | |
| Input hysteresis all digital inputs | V _{hys} | | 0.06 x V _{DD} | — | — | mV | |
| Input leakage current all input only pins (Per pin) | I _{Iinl} | V _{In} = V _{DD} or V _{SS} | — | — | 1 | μA | |
| Hi-Z (off-state) leakage current all input/output (per pin) | I _{OZl} | V _{In} = V _{DD} or V _{SS} | — | — | 1 | μA | |
| Pullup resistors all digital inputs, when enabled | R _{PU} | | 17.5 | — | 52.5 | kΩ | |
| DC injection current ^{3, 4, 5} Single pin limit Total MCU limit, includes sum of all stressed pins | I _{IC} | V _{In} < V _{SS} , V _{In} > V _{DD} | -0.2 | — | 0.2 | mA | |
| | | | -5 | — | 5 | mA | |
| Input Capacitance, all pins | C _{In} | | — | — | 8 | pF | |
| RAM retention voltage | V _{RAM} | | — | 0.6 | 1.0 | V | |
| POR re-arm voltage ⁶ | V _{POR} | | 0.9 | 1.4 | 1.79 | V | |
| POR re-arm time | t _{POR} | | 10 | — | — | μs | |

Table 21. DC Characteristics (continued)

| Characteristic | Symbol | Condition | Min | Typ ¹ | Max | Unit | Ambient temperature operating range |
|---|-------------------------|------------------|------|------------------|------|------|-------------------------------------|
| Low-voltage detection threshold — high range ⁷ | V_{LVDH} ⁸ | V_{DD} falling | 2.31 | 2.34 | 2.36 | V | −40 °C ~ 105 °C |
| | | | 2.16 | 2.3 | 2.48 | | −40 °C ~ +125 °C |
| | | V_{DD} rising | 2.38 | 2.44 | 2.47 | | −40 °C ~ 105 °C |
| | | | 2.23 | 2.39 | 2.49 | | −40 °C ~ +125 °C |
| Low-voltage detection threshold — low range ⁷ | V_{LVDL} | V_{DD} falling | 1.8 | 1.84 | 1.87 | V | −40 °C ~ 105 °C |
| | | | N/A | N/A | N/A | | −40 °C ~ +125 °C |
| | | V_{DD} rising | 1.88 | 1.93 | 1.96 | | −40 °C ~ 105 °C |
| Low-voltage warning threshold | V_{LVW} ⁹ | V_{DD} falling | 2.58 | 2.62 | 2.71 | V | −40 °C ~ 105 °C |
| | | | 2.5 | 2.61 | 2.74 | | −40 °C ~ +125 °C |
| | | V_{DD} rising | 2.59 | 2.67 | 2.74 | | −40 °C ~ 105 °C |
| | | | 2.51 | 2.66 | 2.79 | | −40 °C ~ +125 °C |
| Low-voltage inhibit reset/recover hysteresis ⁷ | V_{hys} | | — | 50 | — | mV | −40 °C ~ +105 °C |
| Bandgap Voltage Reference ¹⁰ | V_{BG} | | 1.15 | 1.17 | 1.18 | V | −40 °C ~ 105 °C |
| | | | 1.14 | | | | −40 °C ~ +125 °C |

¹ Typical values are measured at 25 °C. Characterized, not tested

² As the supply voltage rises, the LVD circuit holds the MCU in reset until the supply has risen above V_{LVDL} . If the system clock frequency < 16 MHz, V_{DD} can be 1.7 V to 3.6 V.

³ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁴ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁵ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present or if clock rate is low (which would reduce overall power consumption).

⁶ Maximum is highest voltage that POR is guaranteed.

⁷ Low voltage detection and warning limits measured at 32 MHz bus frequency. This characteristic is not applicable to devices with a temperature range from −40 °C to 125 °C. Please see the PMC chapter in the reference manual for details.

- ⁸ Runs at 32 MHz bus frequency.
- ⁹ Both Low Voltage Warning (LVW) and Out Of Regulation (OOR) sample the same input source. The OOR flag is a stick bit which is in the PMC_SCR register.
- ¹⁰ Factory trimmed at $V_{DD} = 3.3$ V, Temp = 25 °C.

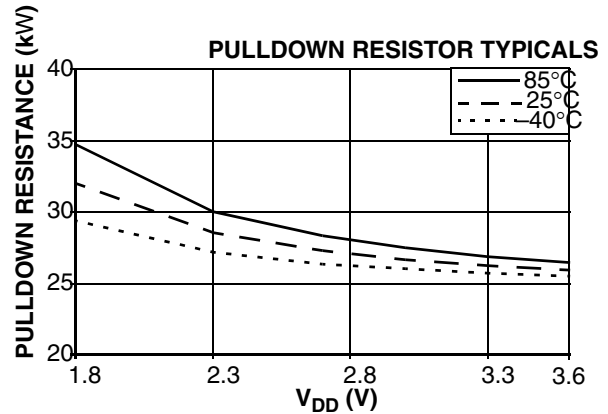
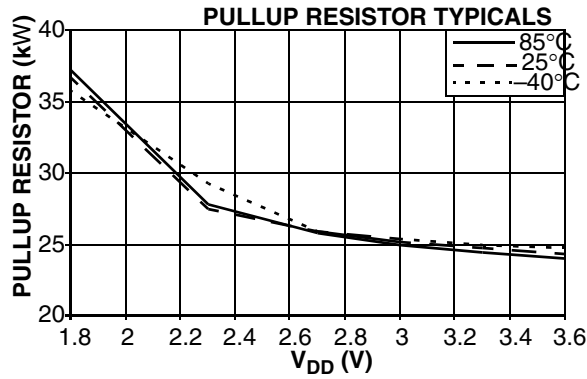


Figure 16. Pullup and Pulldown Typical Resistor Values

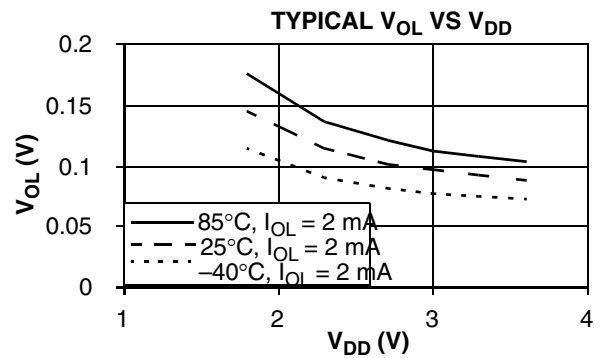
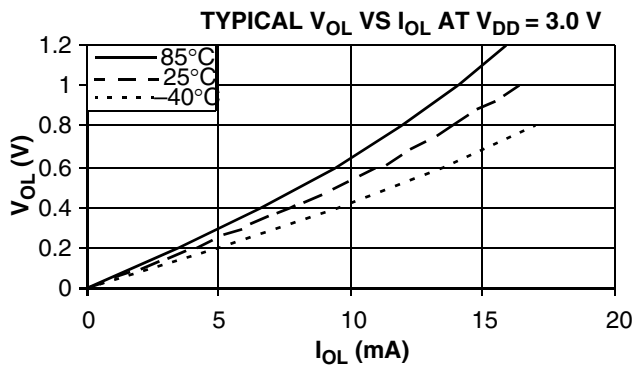


Figure 17. Typical Low-Side Driver (Sink) Characteristics — Low Drive ($GPIO_x_DRIVEN = 0$)

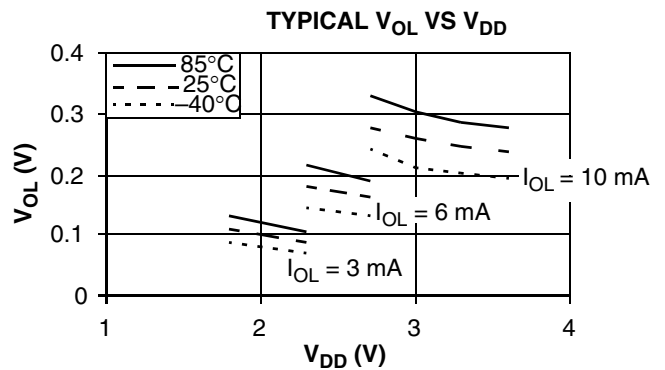
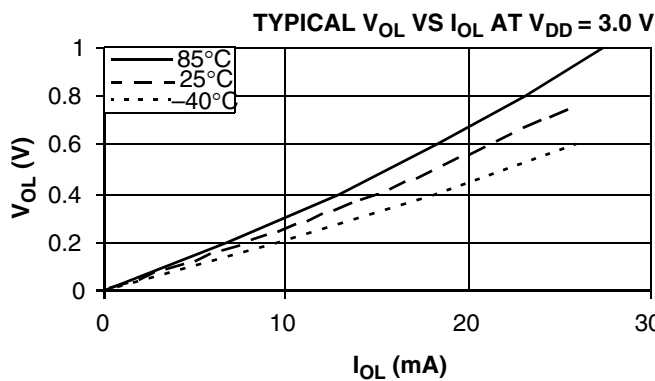


Figure 18. Typical Low-Side Driver (Sink) Characteristics — High Drive ($GPIO_x_DRIVEN = 1$)

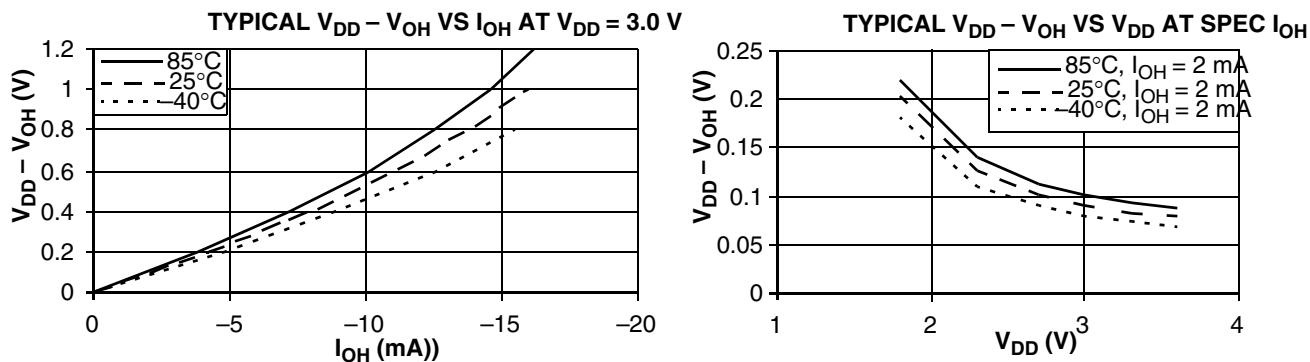


Figure 19. Typical High-Side (Source) Characteristics — Low Drive (GPIO_x_DRIVEN = 0)

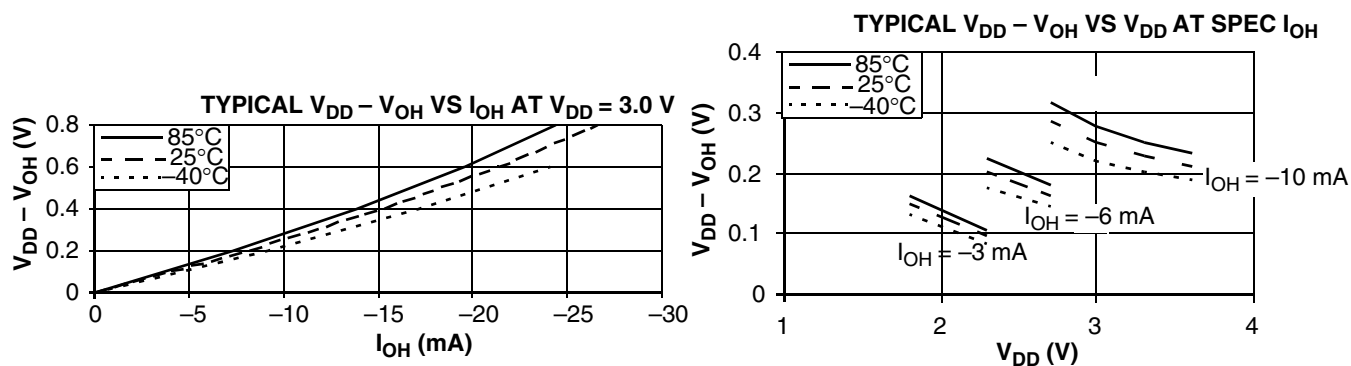


Figure 20. Typical High-Side (Source) Characteristics — High Drive (GPIO_x_DRIVEN = 1)

8.6 Supply Current Characteristics

Table 22. Supply Current Consumption

| Mode | Conditions | Typical @ 3.3 V, 25 °C | | Maximum @ 3.6 V, 105 °C | | Maximum @ 3.6 V, 125 °C | |
|---------------------|--|------------------------------|------------------|------------------------------|------------------|------------------------------|------------------|
| | | I _{DD} ¹ | I _{DDA} | I _{DD} ¹ | I _{DDA} | I _{DD} ¹ | I _{DDA} |
| Run | 32 MHz device clock; relaxation oscillator (ROSC) in high speed mode; PLL engaged; All peripheral modules enabled. TMR and PWM using 1X clock; continuous MAC instructions with fetches from program flash; ADC/DAC powered on and clocked; comparator powered on. | 41.52 mA | 1.71 mA | 53 mA | 2.7 mA | 53 mA | 2.9 mA |
| LSrun ² | 200 kHz device clock; relaxation oscillator (ROSC) in standby mode; PLL disabled All peripheral modules disabled and clock gated off; simple loop with fetches from program flash; | 340.75 μA | 1.70 mA | 480 μA | 2.5 mA | 495 μA | 2.6 mA |
| LPrun ³ | 32.768 kHz device clock; Clocked by a 32.768 kHz external crystal relaxation oscillator (ROSC) in power down; PLL disabled All peripheral modules disabled and clock gated off; simple loop with fetches from program flash; | 166.30 μA | 1.74 mA | 390 μA | 3.4 mA | 399 μA | 3.8 mA |
| Wait | 32 MHz device clock relaxation oscillator (ROSC) in high speed mode PLL engaged; All non-communication peripherals enabled and running; all communication peripherals disabled but clocked; processor core in wait state | 19.3 mA | 1.78 mA | 28 mA | 2.7 mA | 28 mA | 2.8 mA |
| LSwait ² | 200 kHz device clock; relaxation oscillator (ROSC) in standby mode; PLL disabled; All peripheral modules disabled and clock gated off; processor core in wait state | 265.42 μA | 1.70 mA | 380 μA | 2.5 mA | 398 μA | 2.6 mA |

Table 22. Supply Current Consumption (continued)

| Mode | Conditions | Typical @ 3.3 V, 25 °C | | Maximum @ 3.6 V, 105 °C | | Maximum @ 3.6 V, 125 °C | |
|--|--|------------------------------|------------------|------------------------------|------------------|------------------------------|------------------|
| | | I _{DD} ¹ | I _{DDA} | I _{DD} ¹ | I _{DDA} | I _{DD} ¹ | I _{DDA} |
| LPwait ³ | 32.768 kHz device clock; Clocked by a 32.768 kHz external crystal oscillator in power down; PLL disabled; All peripheral modules disabled and clock gated off; processor core in wait state | 157.55 μA | 1.57 mA | 380 μA | 3.4 mA | 398 μA | 3.6 mA |
| Stop | 32 MHz device clock relaxation oscillator (ROSC) in high speed mode; PLL engaged; all peripheral module and core clocks are off; ADC/DAC/comparator powered off; processor core in stop state | 8.21 mA | 65.51 μA | 9.8 mA | 130 μA | 10.3 mA | 132 μA |
| LSstop ² | 200 kHz device clock; relaxation oscillator (ROSC) in standby mode; PLL disabled; all peripheral modules disabled and clock gated off; processor core in stop state. | 194.69 μA | 65.51 μA | 340 μA | 120 μA | 357 μA | 123 μA |
| LPstop ² | 32.768 kHz device clock; Clocked by a 32.768 kHz external crystal relaxation oscillator (ROSC) in power down; PLL disabled; all peripheral modules disabled and clock gated off; processor core in stop state. | 2.77 μA | 13.99 nA | 45 μA | 3.0 μA | 58 μA | 3.6 μA |
| PPD ⁴ with XOSC | 32.768 kHz clock fed on XTAL RTC or COP monitoring XOSC (but no wakeup) processor core in stop state | 879.72 nA | 11.56 nA | 18 μA | 2.4 μA | 22 μA | 3.0 μA |
| PPD with LP oscillator (1 kHz) enabled | RTC or COP monitoring LP oscillator (but no wakeup); processor core in stop state. | 499.15 nA | 13.9 nA | 14 μA | 2.4 μA | 17 μA | 2.8 mA |
| PPD with no clock monitoring | RTC and LP oscillator are disabled; processor core in stop state. | 494.04 nA | 12.88 nA | 14 μA | 2.4 μA | 17 μA | 2.8 μA |

¹ No output switching; all ports configured as inputs; all inputs low; no DC loads.

² Low speed mode: LPR (lower voltage regulator control bit) = 0 and voltage regulator is in full regulation. Characterization only.

³ Low power mode: LPR (lower voltage regulator control bit) = 1; the voltage regulator is put into standby.

⁴ Partial power down mode: PPDE (partial power down enable bit) = 1; power management controller (PMC) enters partial power down mode the next time that the STOP command is executed.

8.7 Flash Memory Characteristics

Table 23. Flash Timing Parameters

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---------------------------|--------------------|-----|-----|-----|---------------|
| Program time ¹ | t_{prog} | 20 | — | 40 | μs |
| Erase time ² | t_{erase} | 20 | — | — | ms |
| Mass erase time | t_{me} | 100 | — | — | ms |

¹ There is additional overhead that is part of the programming sequence. See the *MC56F8006 Peripheral Reference Manual* for detail.

² Specifies page erase time. There are 512 bytes per page in the program flash memory.

8.8 External Clock Operation Timing

Table 24. External Clock Operation Timing Requirements¹

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-------------------|---------------------|-----|--------------------|------|
| Frequency of operation (external clock driver) ² | f_{osc} | — | — | 64 | MHz |
| Clock pulse width ³ | t_{PW} | 6.25 | — | — | ns |
| External clock input rise time ⁴ | t_{rise} | — | — | 3 | ns |
| External clock input fall time ⁵ | t_{fall} | — | — | 3 | ns |
| Input high voltage overdrive by an external clock | V_{ih} | $0.85V_{\text{DD}}$ | — | — | V |
| Input high voltage overdrive by an external clock | V_{il} | — | — | $0.3V_{\text{DD}}$ | V |

¹ Parameters listed are guaranteed by design.

² See [Figure 21](#) for detail on using the recommended connection of an external clock driver.

³ The chip may not function if the high or low pulse width is smaller than 6.25 ns.

⁴ External clock input rise time is measured from 10% to 90%.

⁵ External clock input fall time is measured from 90% to 10%.

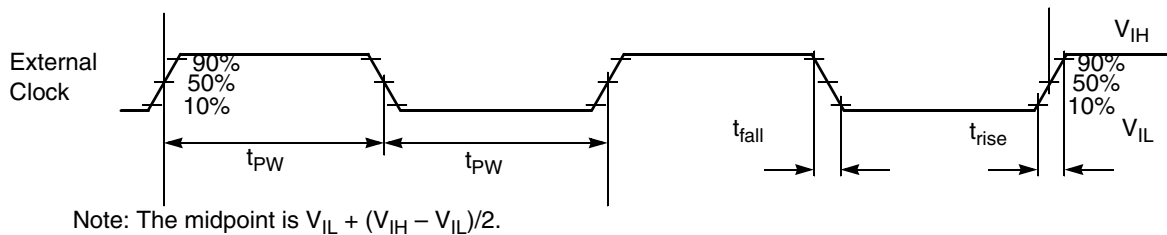


Figure 21. External Clock Timing

8.9 Phase Locked Loop Timing

Table 25. Phase Locked Loop Timing

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-----------------|-----|-----|------|---------|
| PLL input reference frequency ¹ | f_{ref} | 4 | 8 | — | MHz |
| PLL output frequency ² | f_{op} | 120 | 192 | — | MHz |
| PLL lock time ^{3 4} | t_{pils} | — | 40 | 100 | μ s |
| Accumulated jitter using an 8 MHz external crystal as the PLL source ⁵ | J_A | — | — | 0.37 | % |
| Cycle-to-cycle jitter | $t_{jitterpll}$ | — | 350 | — | ps |

¹ An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.

² The core system clock operates at 1/6 of the PLL output frequency.

³ This is the time required after the PLL is enabled to ensure reliable operation.

⁴ From powerdown to powerup state at 32 MHz system clock state.

⁵ This is measured on the CLKO signal (programmed as system clock) over 264 system clocks at 32 MHz system clock frequency and using an 8 MHz oscillator frequency.

8.10 Relaxation Oscillator Timing

Table 26. Relaxation Oscillator Timing

| Characteristic | Symbol | Minimum | Typical | Maximum | Unit |
|--|------------------|---------|-------------|------------------|------------|
| Relaxation oscillator output frequency ¹ Normal Mode Standby Mode | f_{op} | — | 8.05 400 | — | MHz kHz |
| Relaxation oscillator stabilization time ² | t_{roscs} | — | 1 | 3 | ms |
| Cycle-to-cycle jitter. This is measured on the CLKO signal (programmed prescaler_clock) over 264 clocks ³ | $t_{jitterrosc}$ | — | 400 | — | ps |
| Variation over temperature $-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$ ⁴ | | — | — | -3.0 to $+2.0$ | % |
| Variation over temperature $0\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$ ⁵ | | — | — | -2.0 to $+2.0$ | % |
| Variation over temperature $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ ⁴ | | — | — | -3.5 to $+3.0$ | % |

¹ Output frequency after factory trim.

² This is the time required from standby to normal mode transition.

³ J_A is required to meet QSCI requirements.

⁴ See Figure 22. The power supply VDD must be greater than or equal to 2.6 V. Below 2.6 V, the maximum variation over the whole temperature and whole voltage range from 1.8 V to 2.6 V will be +/-16%.

⁵ This data is only applied to devices with temperature range from $-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$.

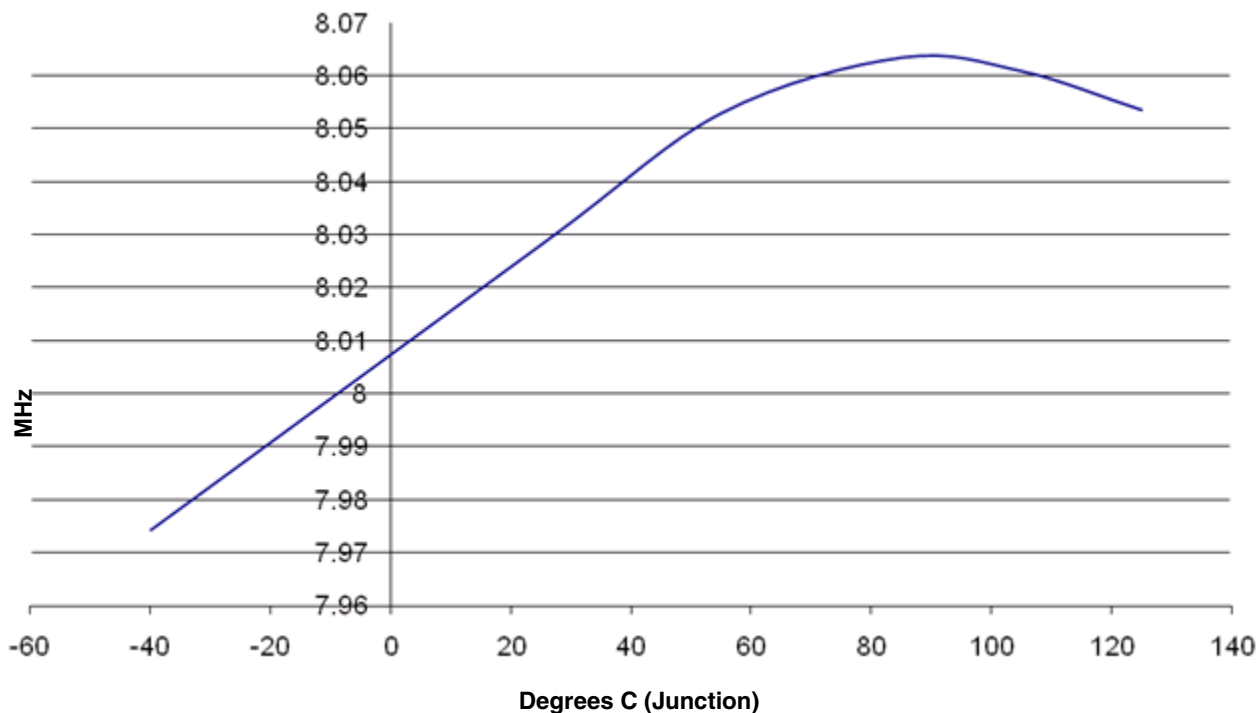


Figure 22. Relaxation Oscillator Temperature Variation (Typical) After Trim for devices with temperature operating range from $-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$

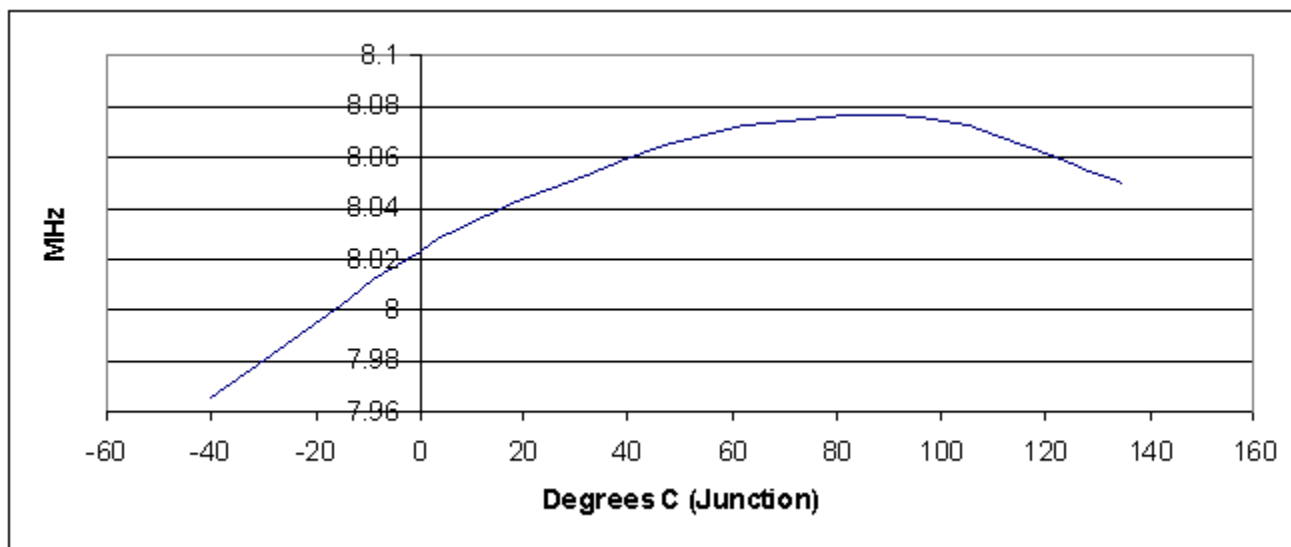


Figure 23. Relaxation Oscillator Temperature Variation (Typical) After Trim for devices with temperature operating range from $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$

8.11 Reset, Stop, Wait, Mode Select, and Interrupt Timing

NOTE

All address and data buses described here are internal.

Table 27. Reset, Stop, Wait, Mode Select, and Interrupt Timing^{1,2}

| Characteristic | Symbol | Typical Min | Typical Max | Unit | See Figure |
|---|------------------|--------------------------|--------------------------|------|------------|
| Minimum $\overline{\text{RESET}}$ Assertion Duration | t_{RA} | 4T | — | ns | — |
| Minimum GPIO pin Assertion for Interrupt | t_{IW} | 2T | — | ns | Figure 24 |
| $\overline{\text{RESET}}$ deassertion to First Address Fetch | t_{RDA} | $96T_{\text{OSC}} + 64T$ | $97T_{\text{OSC}} + 65T$ | ns | — |
| Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop) | t_{IF} | — | 6T | ns | — |

¹ In the formulas, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 32 MHz, T = 31.25 ns. At 4 MHz (used coming out of reset and stop modes), T = 250 ns.

² Parameters listed are guaranteed by design.

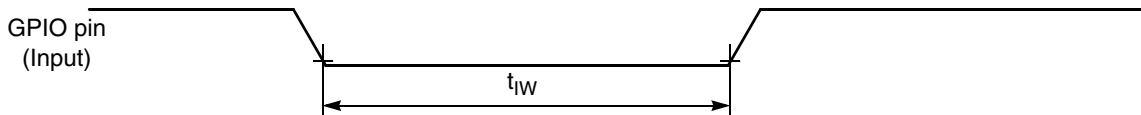


Figure 24. GPIO Interrupt Timing (Negative Edge-Sensitive)

8.12 External Oscillator (XOSC) Characteristics

Reference [Figure 10](#), and [Figure 11](#), and [Figure 12](#) for crystal or resonator circuits.

Table 28. Crystal Oscillator Characteristics

| Characteristic | Symbol | Min | Typ ¹ | Max | Unit |
|--|------------|--|------------------|------|-----------|
| Oscillator crystal or resonator (PRECS = 1, CLK_MOD = 0) | | | | | |
| Low range (RANGE = 0) | f_{lo} | 32 | — | 38.4 | kHz |
| High range (RANGE = 1), high gain (COHL = 0) | f_{hi} | 1 | — | 16 | MHz |
| High range (RANGE = 1), low power (COHL = 1) | f_{hi} | 1 | — | 8 | MHz |
| Load capacitors | C_1, C_2 | See Note ² See Note ³ | | | |
| Feedback resistor | R_F | | | | $M\Omega$ |
| Low range, low power (RANGE=0, COHL = 1) ² | | — | — | — | |
| Low range, high gain (RANGE=0, COHL = 0) | | — | 10 | — | |
| High range (RANGE=1, COHL=X) | | — | 1 | — | |
| Series resistor | R_S | | | | $k\Omega$ |
| Low range, low power (RANGE = 0, COHL = 1) ² | | — | 0 | — | |
| Low range, high gain (RANGE = 0, COHL = 0) | | — | 100 | — | |
| High range, low power (RANGE = 1, COHL = 1) | | — | 0 | — | |
| High range, high gain (RANGE = 1, COHL = 0) | | | | | |
| ≥ 8 MHz | | — | 0 | 0 | |
| 4 MHz | | — | 0 | 10 | |
| 1 MHz | | — | 0 | 20 | |
| Crystal start-up time ⁴ | | | | | ms |
| Low range, low power | t_{CSTL} | — | TBD | — | |
| Low range, high gain | | — | TBD | — | |
| High range, low power | t_{CSTH} | — | TBD | — | |
| High range, high gain | | — | TBD | — | |
| Square wave input clock frequency (PRECS = 1, CLK_MOD = 1) | f_{xtal} | — | — | 50.0 | MHz |

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

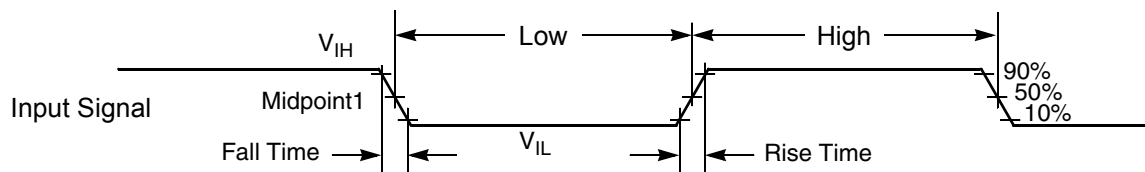
² Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

³ See crystal or resonator manufacturer's recommendation.

⁴ Proper PC board layout procedures must be followed to achieve specifications.

8.13 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 22. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 25.



The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 25. Input Signal Measurement References

Figure 26 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state

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- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

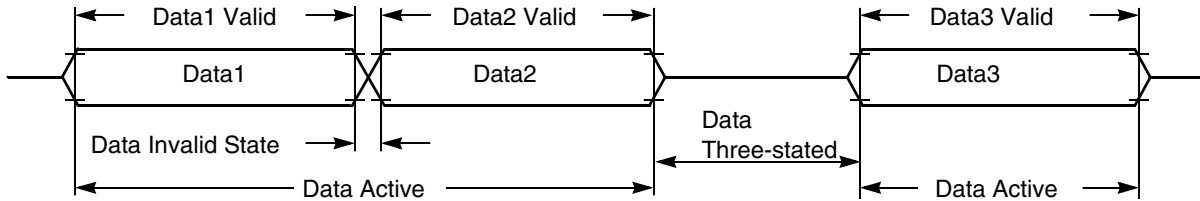


Figure 26. Signal States

8.13.1 Serial Peripheral Interface (SPI) Timing

Table 29. SPI Timing¹

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|--|-----------|-------------|--------|----------|---|
| Cycle time Master Slave | t_C | 125 62.5 | — — | ns ns | Figure 27, Figure 28, Figure 29, Figure 30 |
| Enable lead time Master Slave | t_{ELD} | — 31 | — — | ns ns | Figure 30 |
| Enable lag time Master Slave | t_{ELG} | — 125 | — — | ns ns | Figure 30 |
| Clock (SCK) high time Master Slave | t_{CH} | 50 31 | — — | ns ns | Figure 27, Figure 28, Figure 29, Figure 30 |
| Clock (SCK) low time Master Slave | t_{CL} | 50 31 | — — | ns ns | Figure 30 |
| Data set-up time required for inputs Master Slave | t_{DS} | 20 0 | — — | ns ns | Figure 27, Figure 28, Figure 29, Figure 30 |
| Data hold time required for inputs Master Slave | t_{DH} | 0 2 | — — | ns ns | Figure 27, Figure 28, Figure 29, Figure 30 |
| Access time (time to data active from high-impedance state) Slave | t_A | 4.8 | 15 | ns | Figure 30 |
| Disable time (hold time to high-impedance state) Slave | t_D | 3.7 | 15.2 | ns | Figure 30 |

Table 29. SPI Timing¹ (continued)

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|---|----------|--------|--------------|----------|---|
| Data valid for outputs Master Slave (after enable edge) | t_{DV} | — — | 4.5 20.4 | ns ns | Figure 27, Figure 28, Figure 29, Figure 30 |
| Data invalid Master Slave | t_{DI} | 0 0 | — — | ns ns | Figure 27, Figure 28, Figure 29, Figure 30 |
| Rise time Master Slave | t_R | — — | 11.5 10.0 | ns ns | Figure 27, Figure 28, Figure 29, Figure 30 |
| Fall time Master Slave | t_F | — — | 9.7 9.0 | ns ns | Figure 27, Figure 28, Figure 29, Figure 30 |

¹ Parameters listed are guaranteed by design.

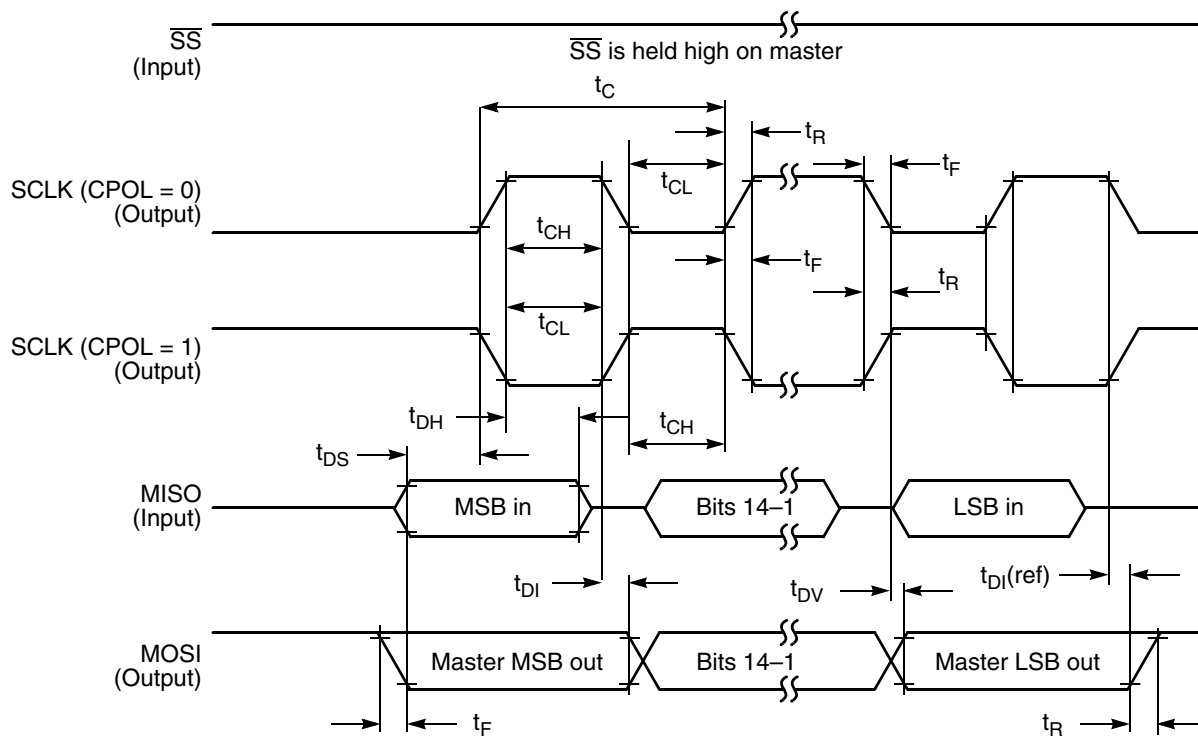


Figure 27. SPI Master Timing (CPHA = 0)

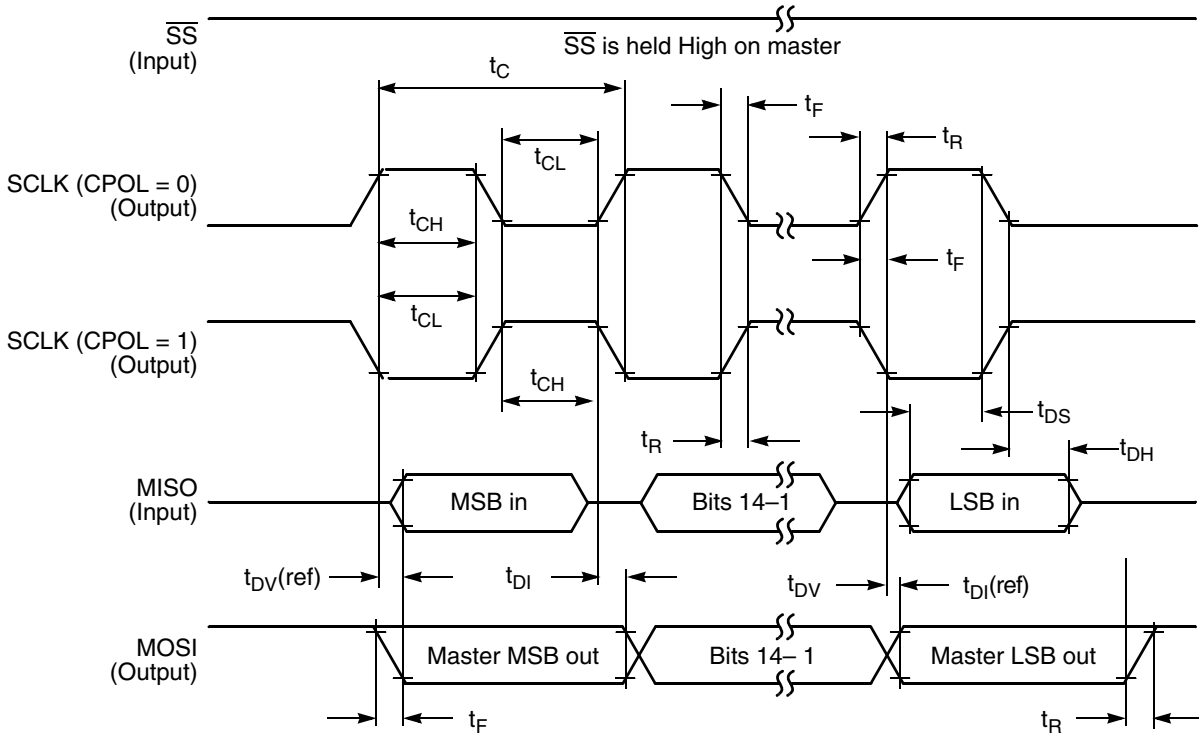


Figure 28. SPI Master Timing (CPHA = 1)

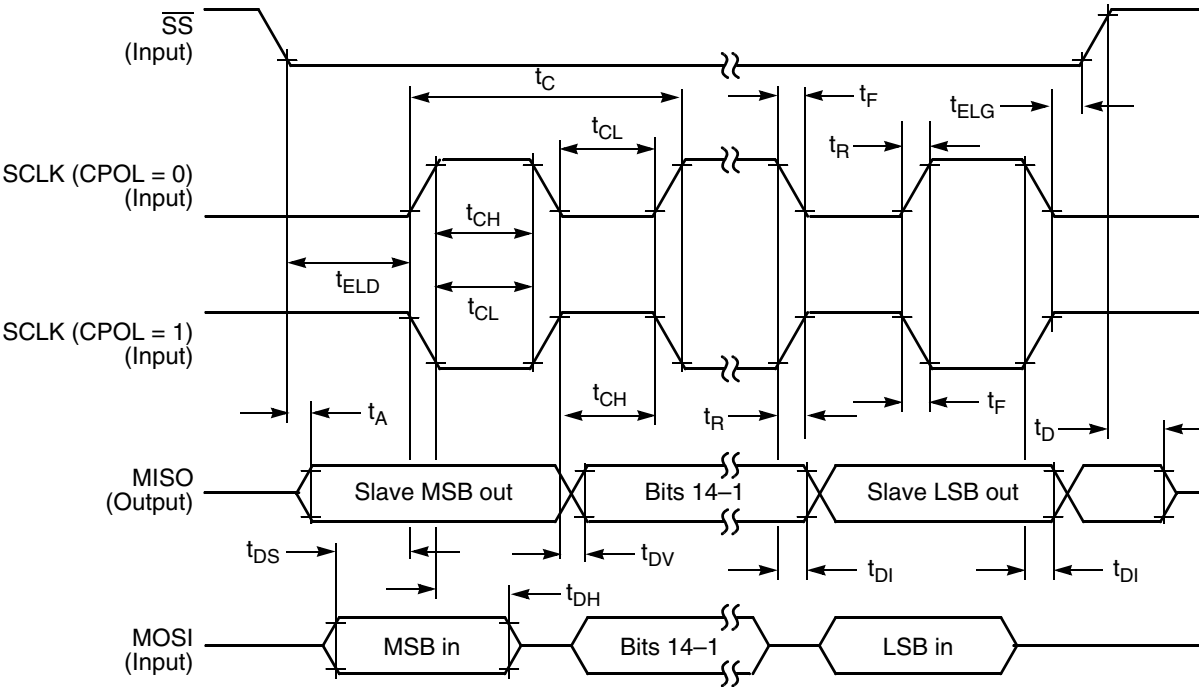


Figure 29. SPI Slave Timing (CPHA = 0)

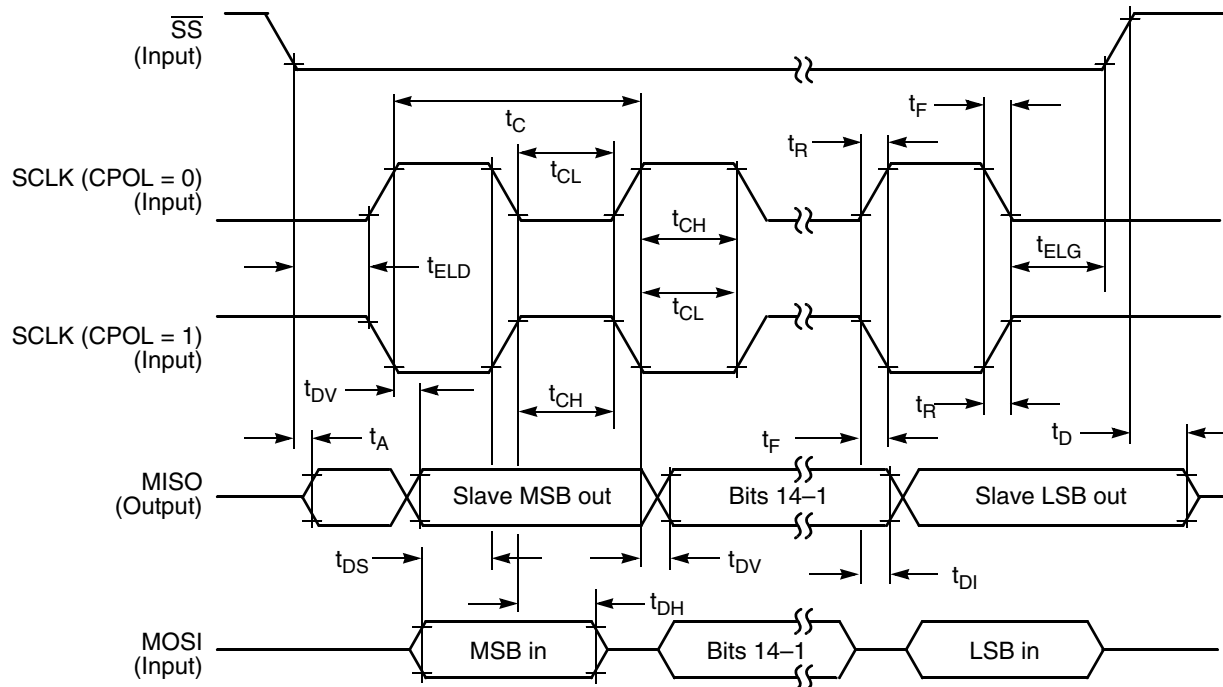


Figure 30. SPI Slave Timing (CPHA = 1)

8.13.2 Serial Communication Interface (SCI) Timing

 Table 30. SCI Timing¹

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|---|--------------------------|----------|------------------|-------------------------|------------|
| Baud rate ² | BR | — | ($f_{MAX}/16$) | Mbps | — |
| RXD pulse width | RXD _{PW} | 0.965/BR | 1.04/BR | ns | Figure 31 |
| TXD pulse width | TXD _{PW} | 0.965/BR | 1.04/BR | ns | Figure 32 |
| LIN Slave Mode | | | | | |
| Deviation of slave node clock from nominal clock rate before synchronization | F _{TOL_UNSYNCH} | -14 | 14 | % | — |
| Deviation of slave node clock relative to the master node clock after synchronization | F _{TOL_SYNCH} | -2 | 2 | % | — |
| Minimum break character length | T _{BREAK} | 13 | — | Master node bit periods | — |
| | | 11 | — | Slave node bit periods | — |

¹ Parameters listed are guaranteed by design.

² f_{MAX} is the frequency of operation of the SCI in MHz, which can be selected system clock (max. 32 MHz) or 3x system clock (max. 96 MHz) for the 56F8006/56F8002 device.

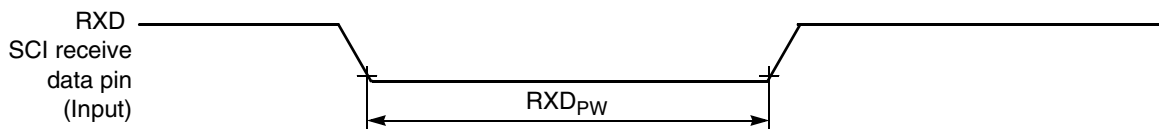


Figure 31. RXD Pulse Width

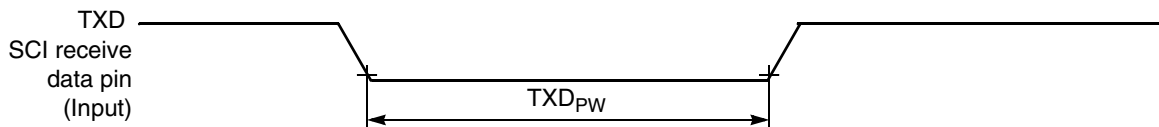


Figure 32. TXD Pulse Width

8.13.3 Inter-Integrated Circuit Interface (I²C) Timing

Table 31. I²C Timing

| Characteristic | Symbol | Standard Mode | | Unit |
|---|---------------|----------------|-------------------|---------|
| | | Minimum | Maximum | |
| SCL Clock Frequency | f_{SCL} | 0 | 100 | MHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD; STA}$ | 4.0 | — | μs |
| LOW period of the SCL clock | t_{LOW} | 4.7 | — | μs |
| HIGH period of the SCL clock | t_{HIGH} | 4.0 | — | μs |
| Set-up time for a repeated START condition | $t_{SU; STA}$ | 4.7 | — | μs |
| Data hold time for I ² C bus devices | $t_{HD; DAT}$ | 0 ¹ | 3.45 ² | μs |
| Data set-up time | $t_{SU; DAT}$ | 250 | — | ns |
| Rise time of SDA and SCL signals | t_r | — | 1000 | ns |
| Fall time of SDA and SCL signals | t_f | — | 300 | ns |
| Set-up time for STOP condition | $t_{SU; STO}$ | 4.0 | — | μs |
| Bus free time between STOP and START condition | t_{BUF} | 4.7 | — | μs |
| Pulse width of spikes that must be suppressed by the input filter | t_{SP} | N/A | N/A | ns |

¹ The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

² The maximum $t_{HD; DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

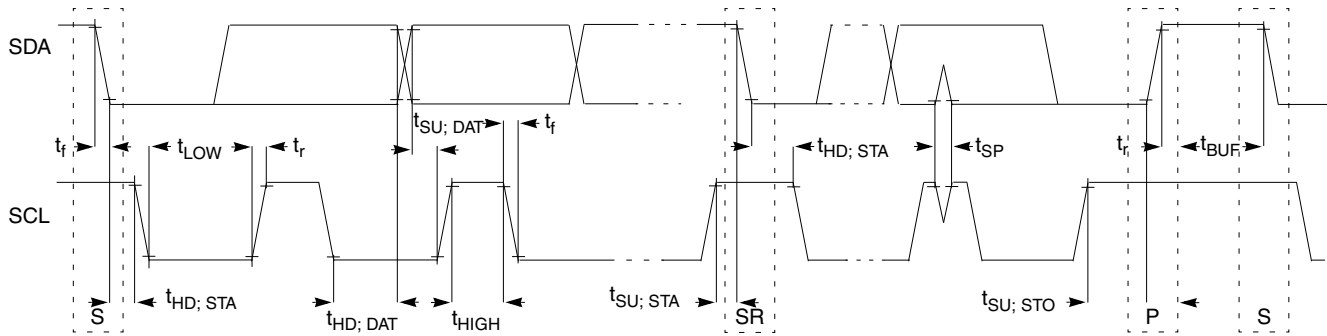


Figure 33. Timing Definition for Standard Mode Devices on the I²C Bus

8.13.4 JTAG Timing

Table 32. JTAG Timing

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|---|-----------------|-----|-----------|------|------------|
| TCK frequency of operation ¹ | f _{OP} | DC | SYS_CLK/8 | MHz | Figure 34 |
| TCK clock pulse width | t _{PW} | 50 | — | ns | Figure 34 |
| TMS, TDI data set-up time | t _{DS} | 5 | — | ns | Figure 35 |
| TMS, TDI data hold time | t _{DH} | 5 | — | ns | Figure 35 |
| TCK low to TDO data valid | t _{DV} | — | 30 | ns | Figure 35 |
| TCK low to TDO tri-state | t _{TS} | — | 30 | ns | Figure 35 |

¹ TCK frequency of operation must be less than 1/8 the processor rate.

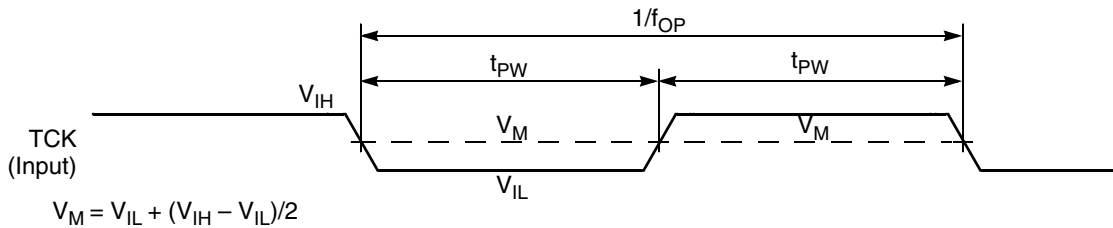


Figure 34. Test Clock Input Timing Diagram

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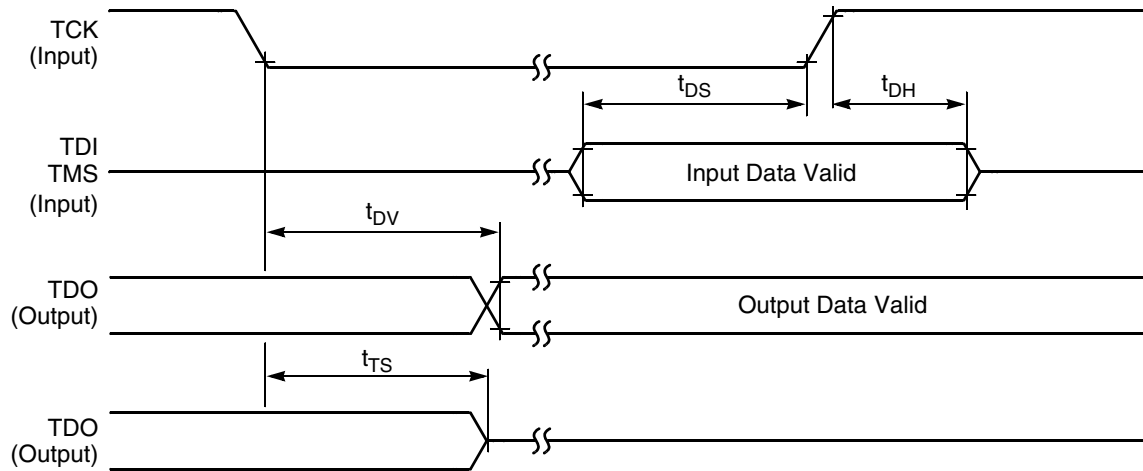


Figure 35. Test Access Port Timing Diagram

8.13.5 Dual Timer Timing

Table 33. Timer Timing^{1, 2}

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|------------------------------|-------------|----------|-----|------|------------|
| Timer input period | P_{IN} | $2T + 6$ | — | ns | Figure 36 |
| Timer input high/low period | P_{INHL} | $1T + 3$ | — | ns | Figure 36 |
| Timer output period | P_{OUT} | 125 | — | ns | Figure 36 |
| Timer output high/low period | P_{OUTHL} | 50 | — | ns | Figure 36 |

¹ In the formulas listed, T = the clock cycle. For 32 MHz operation, T = 31.25ns.

² Parameters listed are guaranteed by design.

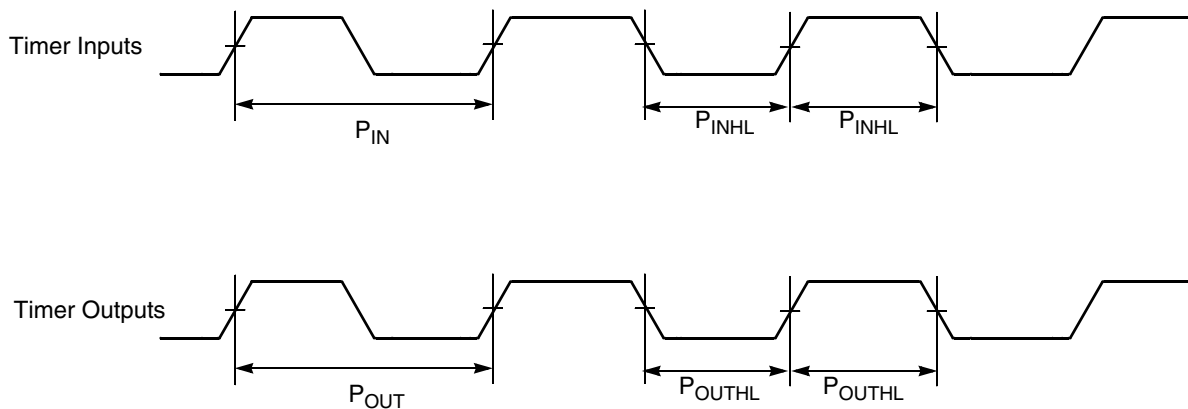


Figure 36. Timer Timing

8.14 COP Specifications

Table 34. COP Specifications

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|--------|-----|------|------|------|
| Oscillator output frequency | LPFosc | 500 | 1000 | 1500 | Hz |
| Oscillator current consumption in partial power down mode | IDD | | TBD | | nA |

8.15 PGA Specifications

Table 35. PGA Specifications

| Parameter | Symbol | Min | Max | Unit |
|--|---------------|--|--|------|
| Digital logic inputs amplitude (_2p5 signal) | V_{2p5} | | 2.75 | V |
| DC analog input level (@ $V_{DD} = avdd3p3$) PGA S/H stage enabled (BP=0) PGA S/H stage disabled (BP=1) | V_{IL} | 0 | V_{DD} $V_{DD} - 0.5$ | V |
| Max differential input voltage (@ Gain and $V_{DD} = avdd3p3$) | $V_{DIFFMAX}$ | | $(V_{DD} - 1) \times 0.5/\text{gain}$ | V |
| Linearity (@ voltage gain) 1x 2x 4x 8x 16x 32x | L_V | 1 - 1/2 LSB 2 - 1/2 LSB 4 - 1 LSB 8 - 1 LSB 16 - 4 LSB 32 - 4 LSB | 1 + 1/2 LSB 2 + 1/2 LSB 4 + 1 LSB 8 + 1 LSB 16 + 4 LSB 32 + 4 LSB | V/V |
| Gain error (@ voltage gain) 1x 2x 4x 8x 16x 32x | A_V | | 1% | V/V |
| Sampling frequency (pga_clk_2p5) normal mode (pga_lp_2p5 asserted) low power mode (pga_lp_2p5 negated) | SF_{max} | | 8 4 | MHz |
| Input signal bandwidth Motor Control mode (BP=0) General Purpose mode (BP=1) | BW_{max} | | PGA sampling rate/2 PGA sampling rate/8 | Hz |
| Internal voltage doubler clock frequency(pga_clk_doubler_2p5) | VD_{clk} | 100 | 2000 | kHz |
| Operating temperature | T | -40 | 125 | °C |

8.16 ADC Specifications

Table 36. ADC Operating Conditions

| Characteristic | Conditions | Symb | Min | Typ ¹ | Max | Unit | Comment |
|----------------------------|---|------------|-------------------------|------------------|-------------------------|------------|-----------------|
| Input voltage | | V_{ADIN} | V_{REFL} ² | — | V_{REFH} ³ | V | |
| Input capacitance | | C_{ADIN} | — | 4.5 | 5.5 | pF | |
| Input resistance | | R_{ADIN} | — | 5 | 7 | k Ω | |
| Analog source resistance | 12-bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz | R_{AS} | — | — | 2 | k Ω | External to MCU |
| | 10-bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz | | — | — | 5 | | |
| | 8-bit mode (all valid f_{ADCK}) | | — | — | 10 | | |
| ADC conversion clock freq. | High speed (ADLPC=0) | f_{ADCK} | 0.4 | — | 8.0 | MHz | |
| | Low power (ADLPC=1) | | 0.4 | — | 4.0 | | |

¹ Typical values assume $V_{DDAD} = 3.0$ V, Temp = 25°C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² $V_{REFL} = V_{SSA}$

³ $V_{REFH} = V_{DDA}$

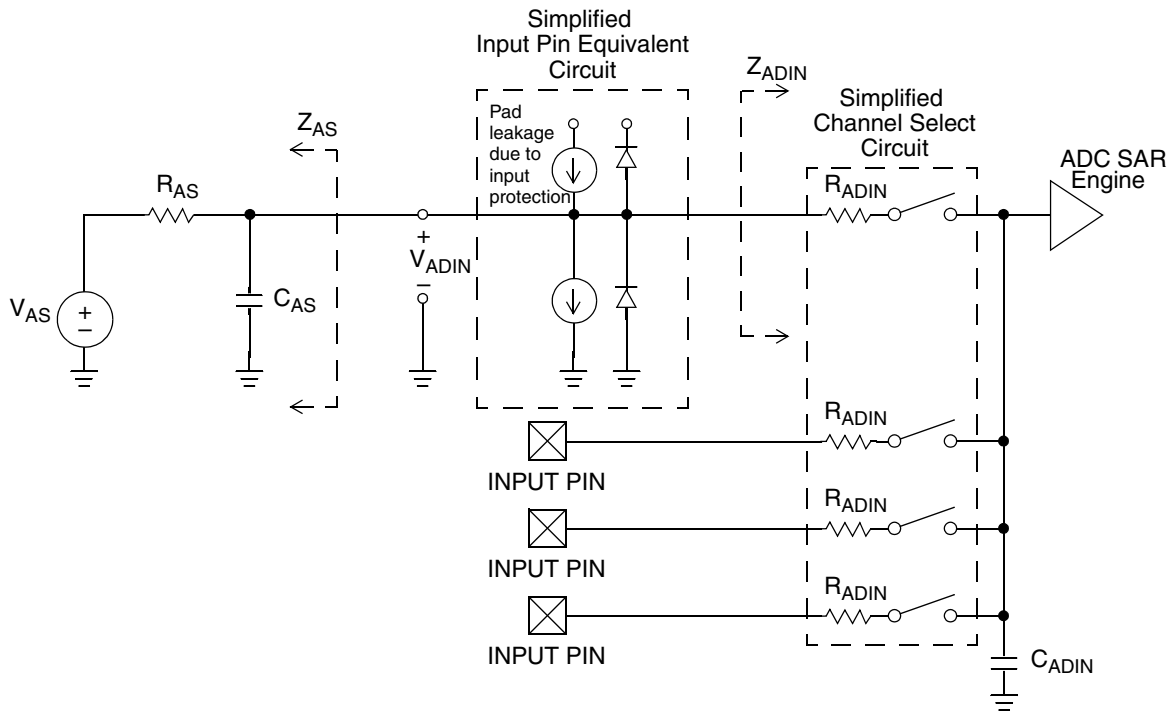


Figure 37. ADC Input Impedance Equivalency Diagram

Table 37. ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Characteristic | Conditions | Symb | Min | Typ ¹ | Max | Unit | Comment |
|---|--------------------------|--------------|------|------------------|-----------|----------------|--|
| Supply current ADLPC=1 ADLSMP=1 ADCO=1 | | I_{DDAD} | — | 120 | — | μA | |
| Supply current ADLPC=1 ADLSMP=0 ADCO=1 | | I_{DDAD} | — | 202 | — | μA | |
| Supply current ADLPC=0 ADLSMP=1 ADCO=1 | | I_{DDAD} | — | 288 | — | μA | |
| Supply current ADLPC=0 ADLSMP=0 ADCO=1 | | I_{DDAD} | — | 0.532 | 1 | mA | |
| ADC asynchronous clock source | High speed (ADLPC=0) | f_{ADACK} | 2 | 3.3 | 5 | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | Low power (ADLPC=1) | | 1.25 | 2 | 3.3 | | |
| Conversion time (including sample time) | Short sample (ADLSMP=0) | t_{ADC} | — | 20 | — | ADCK cycles | |
| | Long sample (ADLSMP=1) | | — | 40 | — | | |
| Sample time | Short sample (ADLSMP=0) | t_{ADS} | — | 3.5 | — | ADCK cycles | |
| | Long sample (ADLSMP=1) | | — | 23.5 | — | | |
| Differential Non-linearity | 12-bit mode | DNL | — | ± 1.75 | — | LSB^2 | |
| | 10-bit mode ³ | | — | ± 0.5 | ± 1.0 | | |
| | 8-bit mode ³ | | — | ± 0.3 | ± 0.5 | | |
| Integral non-linearity | 12-bit mode | INL | — | ± 1.5 | — | LSB^2 | |
| | 10-bit mode | | — | ± 0.5 | ± 1.0 | | |
| | 8-bit mode | | — | ± 0.3 | ± 0.5 | | |
| Quantization error | 12-bit mode | E_Q | — | -1 to 0 | — | LSB^2 | |
| | 10-bit mode | | — | — | ± 0.5 | | |
| | 8-bit mode | | — | — | ± 0.5 | | |
| Input leakage error | 12-bit mode | E_{IL} | — | ± 2 | — | LSB^2 | Pad leakage ⁴ * R_{AS} |
| | 10-bit mode | | — | ± 0.2 | ± 4 | | |
| | 8-bit mode | | — | ± 0.1 | ± 1.2 | | |
| Temp sensor slope | -40°C–25°C | m | — | 1.646 | — | mV/°C | |
| | 25°C–125°C | | — | 1.769 | — | | |
| Temp sensor voltage | 25°C | V_{TEMP25} | — | 701.2 | — | mV | |

Specifications

- ¹ Typical values assume $V_{DDA} = 3.0\text{ V}$, $\text{Temp} = 25^\circ\text{C}$, $f_{ADCK}=1.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.
- ² $1\text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
- ³ Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
- ⁴ Based on input pad leakage current. Refer to pad electricals.

8.17 HSCMP Specifications

Table 38. HSCMP Specifications

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---------------|------------------|-----|------------------|---------------|
| Supply voltage | V_{PWR} | 1.8 | | 3.6 | V |
| Supply current, high speed mode (EN=1, PMODE=1, $V_{DDA} \geq V_{LVI_trip}$) | I_{DDAHS} | | 150 | | μA |
| Supply current, low speed mode (EN=1, PMODE=0) | I_{DDALS} | | 10 | | μA |
| Supply current, off mode (EN=0,) | I_{DDAOFF} | | | 100 | nA |
| Analog input voltage | V_{AIN} | $V_{SSA} - 0.01$ | | $V_{DDA} + 0.01$ | V |
| Analog input offset voltage | V_{AIO} | | | 40 | mV |
| Analog comparator hysteresis | V_H | 3.0 | | 20.0 | mV |
| Propagation Delay, high speed mode (EN=1, PMODE=1), $2.4\text{ V} < V_{DDA} < 3.6\text{ V}$ | t_{DHSN}^1 | | 70 | 140 | ns |
| Propagation Delay, High Speed Mode (EN=1, PMODE=1), $1.8\text{ V} < V_{DDA} < 2.4\text{ V}$ | t_{DHSB}^2 | | 70 | 249 | ns |
| Propagation Delay, Low Speed Mode (EN=1, PMODE=0), $2.4\text{ V} < V_{DDA} < 3.6\text{ V}$ | t_{AINIT}^3 | | 400 | 600 | ns |
| Propagation Delay, Low Speed Mode (EN=1, PMODE=0), $1.8\text{ V} < V_{DDA} < 2.4\text{ V}$ | t_{AINIT}^4 | | 400 | 600 | ns |

¹ Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. $V_{DDA} > V_{LVI_WARNING} \Rightarrow \text{LVI_WARNING NOT ASSERTED}$.

² Measured with an input waveform that switches 30mV above and below the reference, to the CMPO output pin. $V_{DDA} < V_{LVI_WARNING} \Rightarrow \text{LVI_WARNING ASSERTED}$.

³ Measured with an input waveform that switches 30mV above and below the reference, to the CMPO output pin. $V_{DDA} > V_{LVI_WARNING} \Rightarrow \text{LVI_WARNING NOT ASSERTED}$.

⁴ Measured with an input waveform that switches 30mV above and below the reference, to the CMPO output pin. $V_{DDA} < V_{LVI_WARNING} \Rightarrow \text{LVI_WARNING ASSERTED}$.

8.18 Optimize Power Consumption

See Section 8.6, “Supply Current Characteristics,” for a list of I_{DD} requirements for the 56F8006/56F8002. This section provides additional detail that can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Eqn. 1

$$\begin{aligned} \text{Total power} = & \quad \text{A:} \quad \text{internal [static component]} \\ & \quad \text{+B:} \quad \text{internal [state-dependent component]} \\ & \quad \text{+C:} \quad \text{internal [dynamic component]} \\ & \quad \text{+D:} \quad \text{external [dynamic component]} \\ & \quad \text{+E:} \quad \text{external [static component]} \end{aligned}$$

A, the internal [static] component, is comprised of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent] component, reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, flash memory, and the ADCs.

C, the internal [dynamic] component, is classic $C \cdot V^2 \cdot F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic] component, reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C \cdot V^2 \cdot F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 39. I/O Loading Coefficients at 10 MHz

| | Intercept | Slope |
|------------|-----------|------------|
| 8 mA drive | 1.3 | 0.11 mW/pF |
| 4 mA drive | 1.15 mW | 0.11 mW/pF |

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. Table 39 provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases:

$$\text{TotalPower} = \Sigma((\text{Intercept} + \text{Slope} \cdot \text{Cload}) \cdot \text{frequency} / 10 \text{ MHz}) \quad \text{Eqn. 2}$$

where:

- Summation is performed over all output pins with capacitive loads
- Total power is expressed in mW
- C_{load} is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume $V = 0.5$ for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10 mA into LEDs, then $P = 8 \cdot 0.5 \cdot 0.01 = 40 \text{ mW}$.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

9 Design Considerations

9.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \text{Eqn. 3}$$

where:

$$\begin{aligned} T_A &= \text{Ambient temperature for the package (}^\circ\text{C)} \\ R_{\theta JA} &= \text{Junction-to-ambient thermal resistance (}^\circ\text{C/W)} \\ P_D &= \text{Power dissipation in the package (W)} \end{aligned}$$

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 4}$$

where:

$$\begin{aligned} R_{\theta JA} &= \text{Package junction-to-ambient thermal resistance (}^\circ\text{C/W)} \\ R_{\theta JC} &= \text{Package junction-to-case thermal resistance (}^\circ\text{C/W)} \\ R_{\theta CA} &= \text{Package case-to-ambient thermal resistance (}^\circ\text{C/W)} \end{aligned}$$

$R_{\theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 5}$$

where:

$$\begin{aligned} T_T &= \text{Thermocouple temperature on top of package (}^\circ\text{C)} \\ \Psi_{JT} &= \text{Thermal characterization parameter (}^\circ\text{C/W)} \\ P_D &= \text{Power dissipation in package (W)} \end{aligned}$$

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the

junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

9.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8006/56F8002:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the 56F8006/56F8002 and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 μF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA} . Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 μF , plus the number of 0.1 μF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF} , V_{DDA} , and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with V_{DDA} and V_{SSA} traces.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I²C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 k Ω –10 k Ω ; the capacitor value should be in the range of 0.22 μF –4.7 μF .
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 k Ω external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input state with internal pullup enabled. The typical value of internal pullup is around 33 k Ω . These internal pullups can be disabled by software.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10 Ω RC filter.
- External clamp diodes on analog input pins are recommended.

9.3 Ordering Information

Table 40 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order devices.

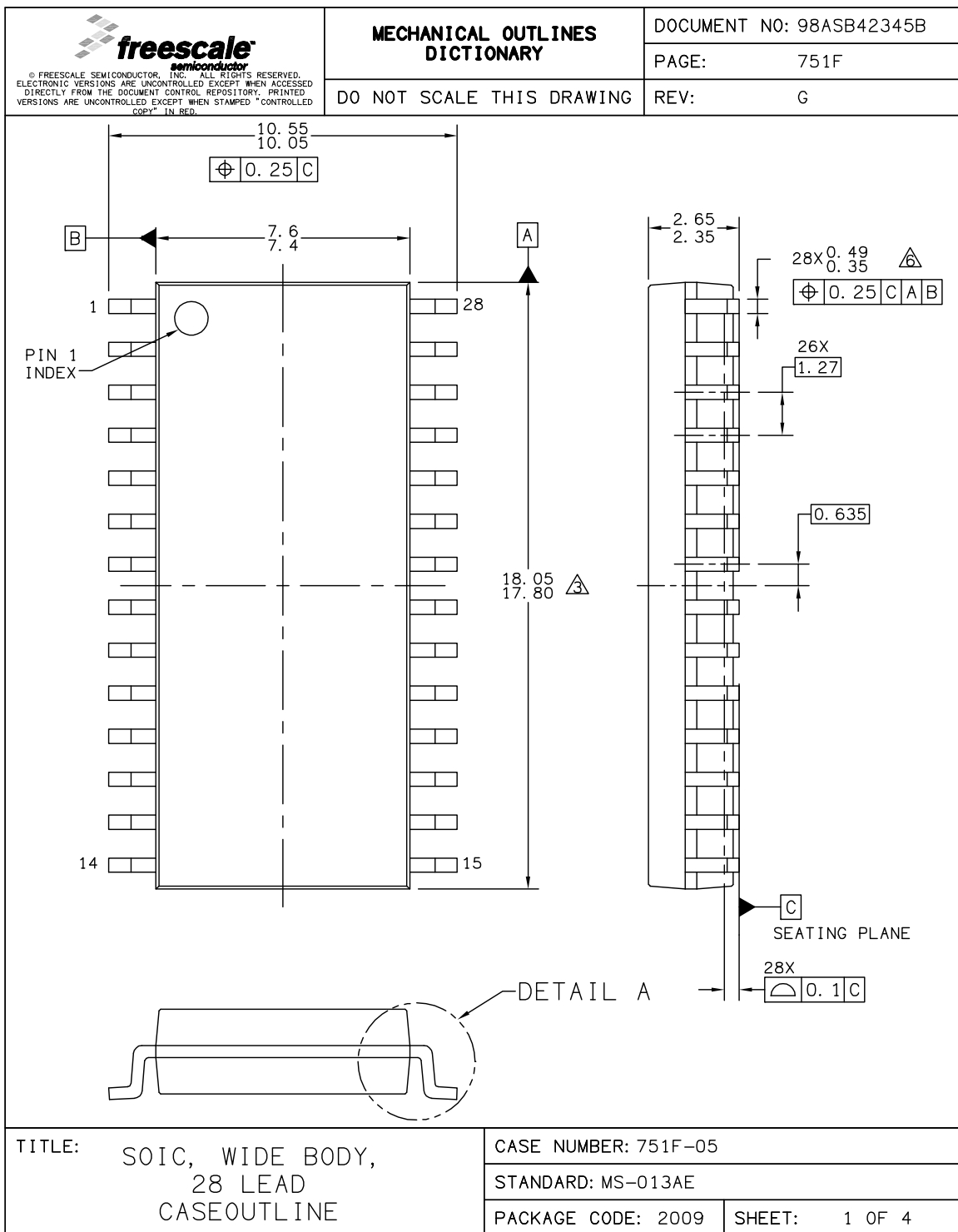
Table 40. 56F8006/56F8002 Ordering Information

| Device | Supply Voltage | Package Type | Pin Count | Frequency (MHz) | Ambient Temperature Range | Order Number |
|-----------|----------------|---|-----------|-----------------|--------------------------------------|---|
| MC56F8002 | 1.8–3.6 V | Small Outline IC (SOIC) | 28 | 32 | –40° to + 105° C –40° to + 125° C | MC56F8002VWL MC56F8002MWL ¹ |
| MC56F8006 | 1.8–3.6 V | Small Outline IC (SOIC) | 28 | 32 | –40° to + 105° C –40° to + 125° C | MC56F8006VWL MC56F8006MWL ¹ |
| MC56F8006 | 1.8–3.6 V | Low-Profile Quad Flat Pack (LQFP) | 32 | 32 | –40° to + 105° C –40° to + 125° C | MC56F8006VLC MC56F8006MLC ¹ |
| MC56F8006 | 1.8–3.6 V | Low-Profile Quad Flat Pack (LQFP) | 48 | 32 | –40° to + 105° C –40° to + 125° C | MC56F8006VLF MC56F8006MLF ¹ |
| MC56F8006 | 1.8–3.6 V | Plastic Shrink Dual In-line Package (PSDIP) | 32 | 32 | –40° to + 105° C | MC56F8006VBM |

¹ This package is RoHS compliant.

10 Package Mechanical Outline Drawings

10.1 28-pin SOIC Package

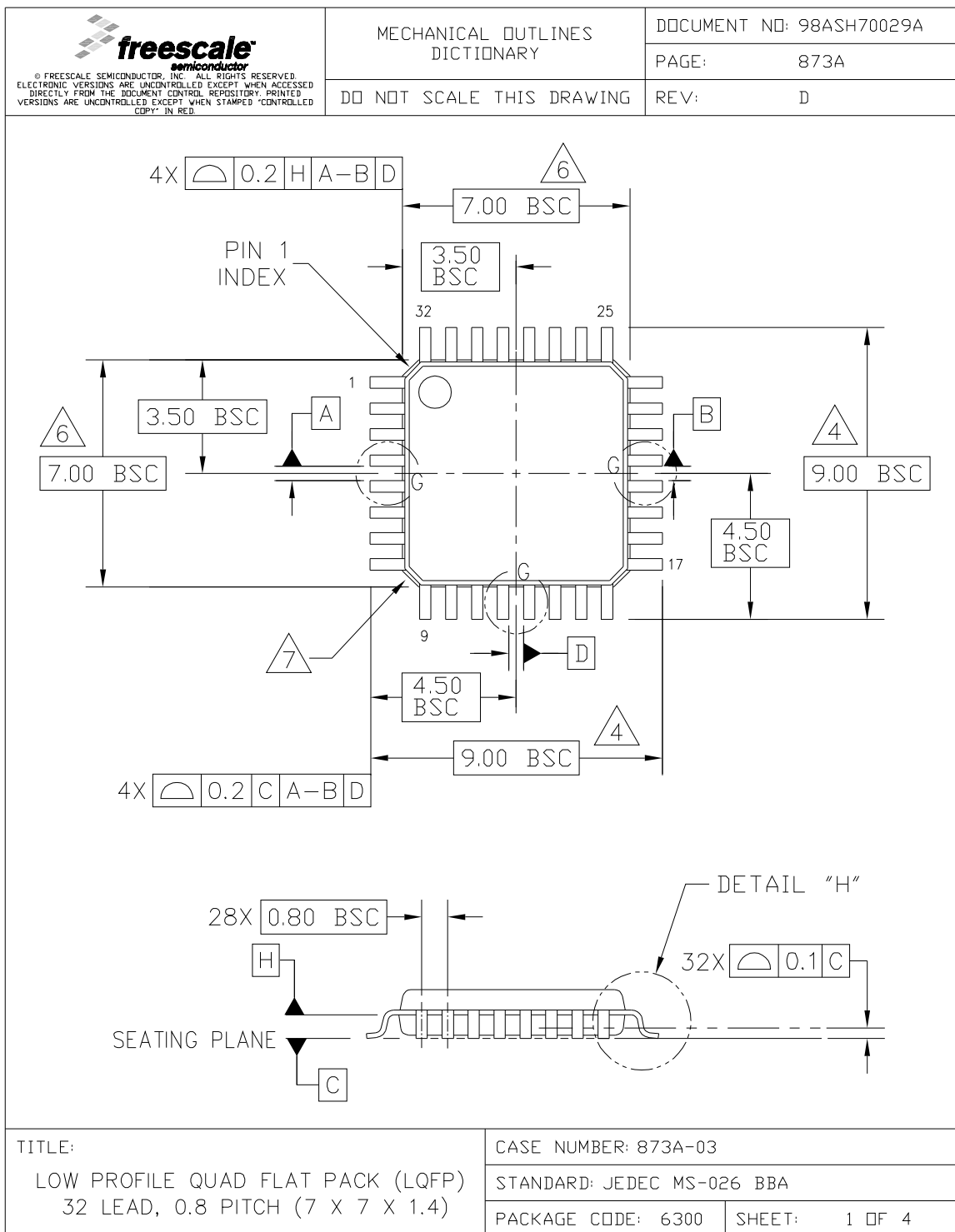


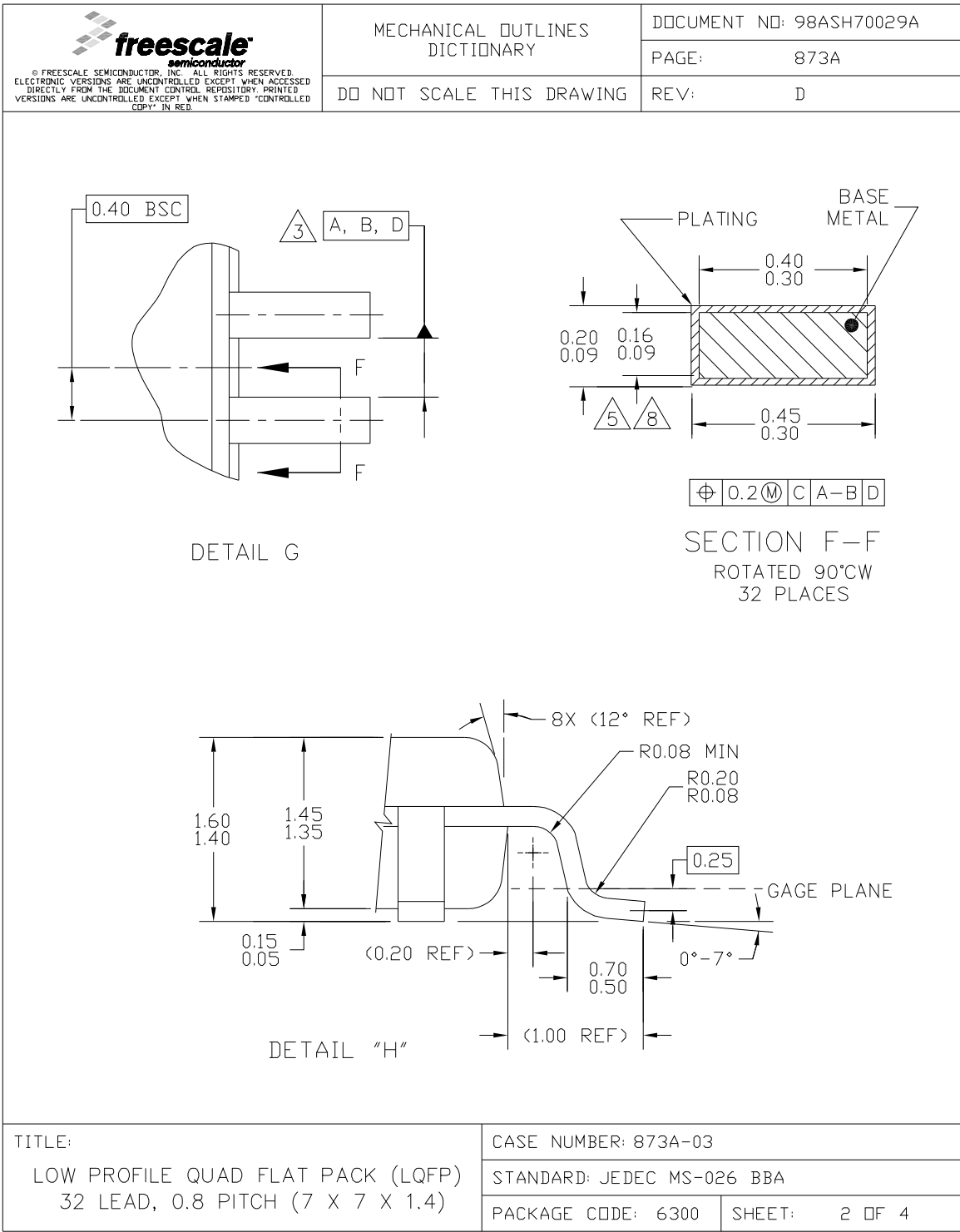
| | | | | |
|---|---|---------------|--------------------------|------|
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| | DO NOT SCALE THIS DRAWING | | PAGE: | 751F |
| | | | REV: | G |
| | | | | |
| TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE | | | CASE NUMBER: 751F-05 | |
| | | | STANDARD: MS-013AE | |
| PACKAGE CODE: 2009 | | SHEET: 2 OF 4 | | |

| | | | |
|--|--|--------------------------|---------------|
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| | | PAGE: | 751F |
| | DO NOT SCALE THIS DRAWING | REV: | G |
| <p>NOTES:</p> <ol style="list-style-type: none"> 1. DIMENSIONS ARE IN MILLIMETERS. 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. 3. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE. 5. 751F-01 THRU -04 OBSOLETE. NEW STANDARD: 751F-05 6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION. | | | |
| <p>TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE</p> | | CASE NUMBER: 751F-05 | |
| | | STANDARD: MS-013AE | |
| | | PACKAGE CODE: 2009 | SHEET: 3 OF 4 |

Figure 38. 56F8006/56F8002 28-Pin SOIC Mechanical Information

10.2 32-pin LQFP

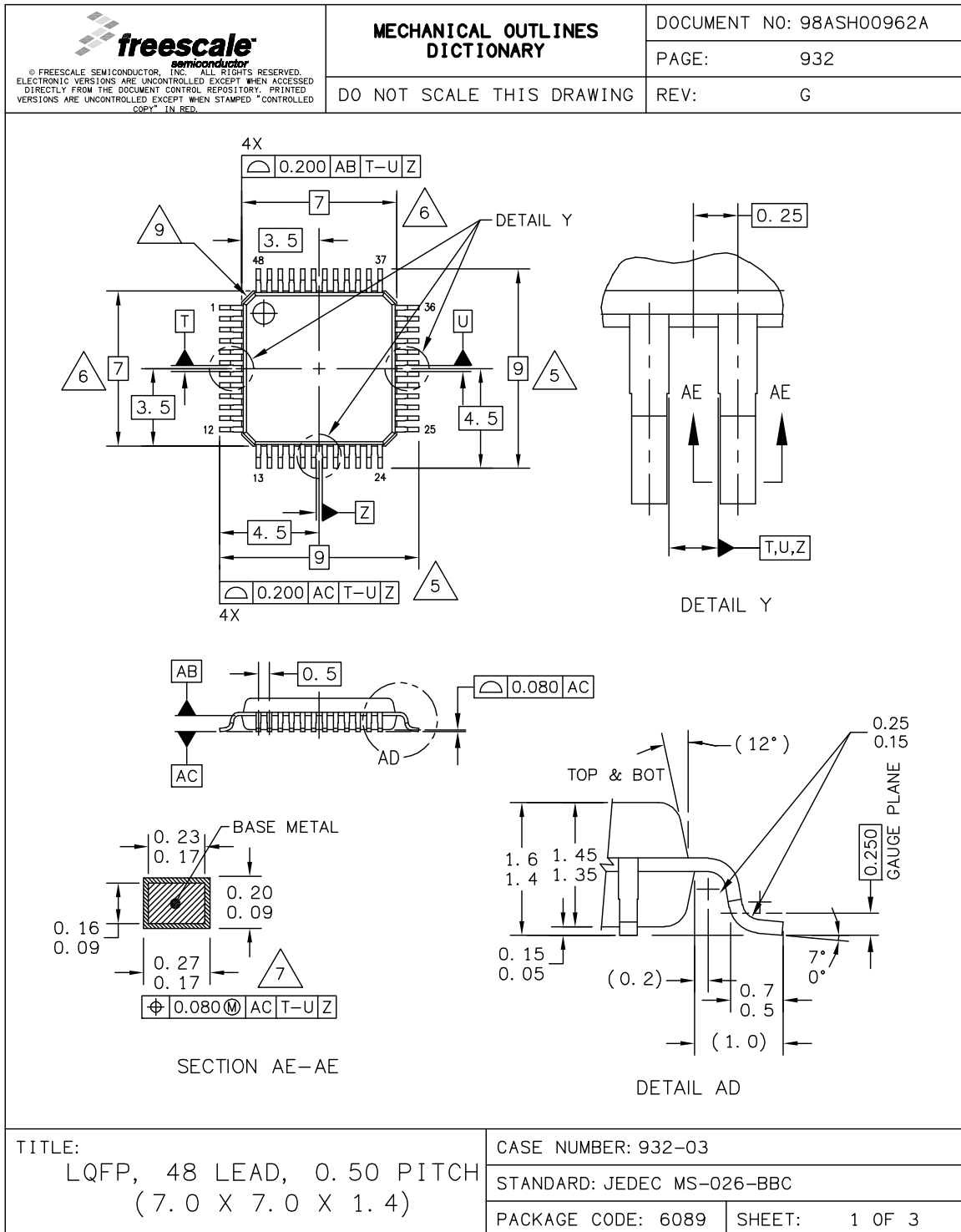




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| | DO NOT SCALE THIS DRAWING | PAGE: 873A REV: D |
| <p>NOTES:</p> <ol style="list-style-type: none"> 1. DIMENSIONS ARE IN MILLIMETERS. 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5-1994. 3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H. 4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C. 5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM. 6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH. 7. EXACT SHAPE OF EACH CORNER IS OPTIONAL. 8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP. | | |
| TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4) | | CASE NUMBER: 873A-03 STANDARD: JEDEC MS-026 BBA PACKAGE CODE: 6300 SHEET: 3 OF 4 |

Figure 39. 56F8006/56F8002 32-Pin LQFP Mechanical Information

10.3 48-pin LQFP

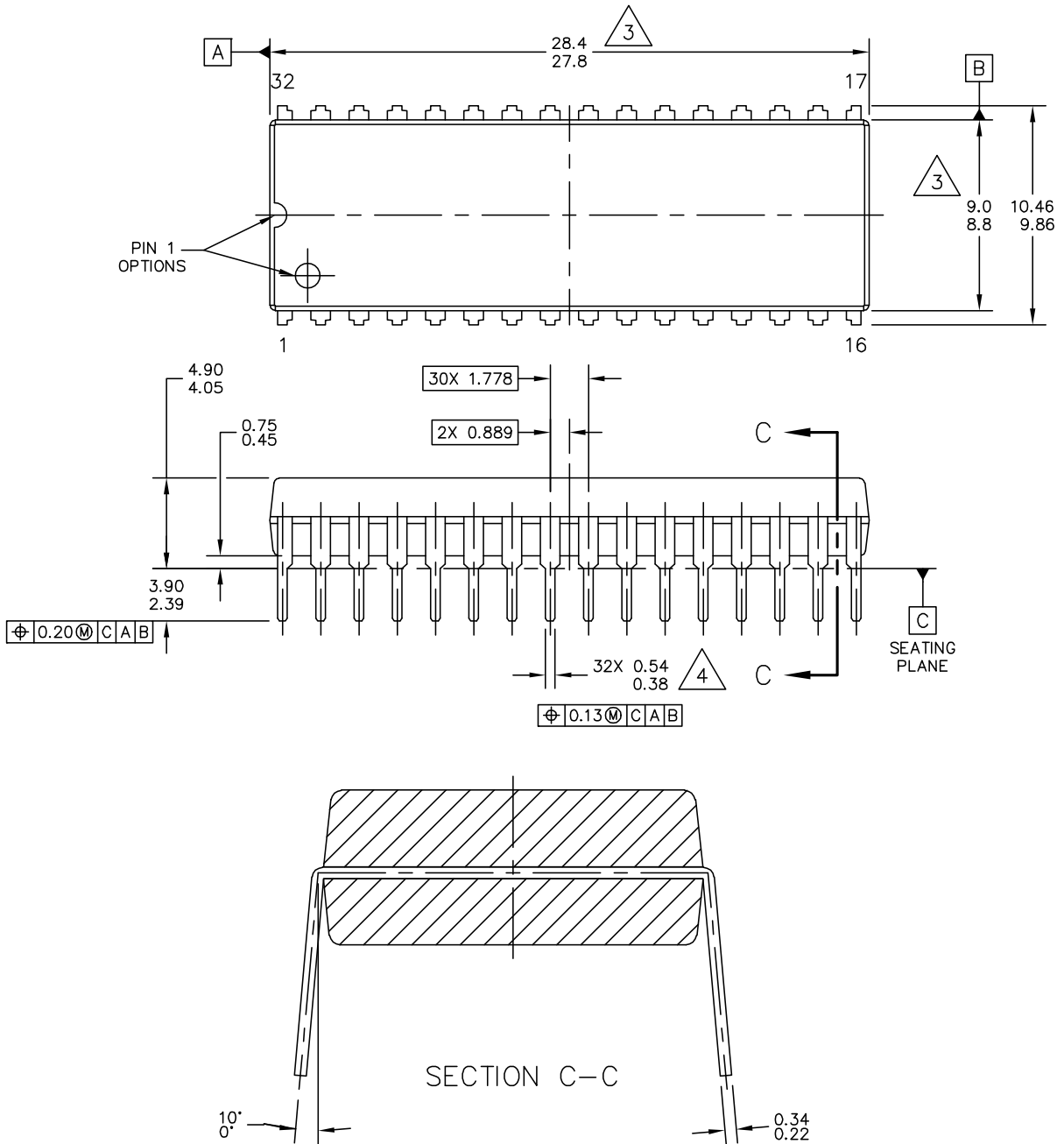


MC56F8006/MC56F8002 Digital Signal Controller, Rev. 4

| | | | |
|---|--|----------------------------|---------------|
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| | | PAGE: | 932 |
| DO NOT SCALE THIS DRAWING | | REV: | G |
| <p>NOTES:</p> <ol style="list-style-type: none"> 1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE. 4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB. 5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC. 6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB. 7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350. 8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076. 9. EXACT SHAPE OF EACH CORNER IS OPTIONAL. | | | |
| TITLE: | | CASE NUMBER: 932-03 | |
| LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4) | | STANDARD: JEDEC MS-026-BBC | |
| | | PACKAGE CODE: 6089 | SHEET: 2 OF 3 |

Figure 40. 56F8006/56F8002 48-Pin LQFP Mechanical Information

10.4 32-Pin PSDIP



| | | | |
|---|---------------------------|----------------------------|--|
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| TITLE: 32 LEAD PDIP | DOCUMENT NO: 98ASA99330D | REV: A | |
| | CASE NUMBER: 1376-02 | 25 APR 2005 | |
| | STANDARD: NON-JEDEC | | |

Package Mechanical Outline Drawings

NOTES:

1. ALL DIMENSION ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14. 5-1994.



DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.



DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.

| | | | |
|---|---------------------------|----------------------------|--|
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| TITLE: 32 LEAD PDIP | DOCUMENT NO: 98ASA99330D | REV: A | |
| | CASE NUMBER: 1376-02 | 25 APR 2005 | |
| | STANDARD: NON-JEDEC | | |

Figure 41. 56F8006/56F8002 32-Pin PSDIP Mechanical Information

11 Revision History

Table 41 lists major changes between versions of the *MC56F8006* document.

Table 41. Changes Between Revisions 2 and 3

| Location | Description |
|---|--|
| Introduction on page 1 | Added part marking for devices covered by this document |
| Section 6.7, "PWM, PDB, PGA, and ADC Connections," on page 38 | Updated routing details for ANB24 and ANB25 |
| Table 12 on page 42 | Removed row about open drain mode (GPIO supports only push-pull mode) |
| Table 21 on page 47 | Updated specifications for low-voltage detection threshold (high and low range) and low-voltage warning threshold |
| Table 22 on page 51 | Updated all Supply Current Consumption specifications |
| Table 26 and Figure 22 on page 55 | Updated ROOSC variation over temperature specifications (both ranges) |
| Table 31 on page 62 | Removed I ² C fast mode specifications and footnote about setup time if the TX FIFO is empty (fast mode and FIFO not supported) |
| Appendix B on page 86 | Added note explaining ADC and GPIO naming conventions |
| Table 44 on page 86 | For I2C_SMB_CSR, clarified that bits 7 and 6 are reserved |

Table 42. Changes Between Revisions 3 and 4

| Location | Description |
|----------------------|---|
| Throughout document. | Added information for 32-pin PSDIP device and devices with temperature range from -40 °C to + 125 °C. |

Appendix A Interrupt Vector Table

Table 43 provides the 56F8006/56F8002's reset and interrupt priority structure, including on-chip peripherals. The table is organized with higher-priority vectors at the top and lower-priority interrupts lower in the table. As indicated, the priority of an interrupt can be assigned to different levels, allowing some control over interrupt priorities. All level 3 interrupts are serviced before level 2 and so on. For a selected priority level, the lowest vector number has the highest priority.

The location of the vector table is determined by the vector base address (VBA). Please see the *MC56F8006 Peripheral Reference Manual* for detail.

By default, the chip reset address and COP reset address correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Table 43. Interrupt Vector Table Contents¹

| Peripheral | Vector Number | User Encoding | Priority Level | Vector Base Address + | Interrupt Function |
|------------------|---------------|---------------|----------------|-----------------------|---|
| Core | | | | P:0x00 | Reserved for Reset Overlay ² |
| Core | | | | P:0x02 | Reserved for COP Reset Overlay |
| Core | 2 | N/A | 3 | P:0x04 | Illegal Instruction |
| Core | 3 | N/A | 3 | P:0x06 | HW Stack Overflow |
| Core | 4 | N/A | 3 | P:0x08 | Misaligned Long Word Access |
| Core | 5 | N/A | 3 | P:0x0A | EOnCE Step Counter |
| Core | 6 | N/A | 3 | P:0x0C | EOnCE Breakpoint Unit |
| Core | 7 | N/A | 3 | P:0x0E | EOnCE Trace Buffer |
| Core | 9 | N/A | 3 | P:0x10 | EOnCE Transmit Register Empty |
| Core | 9 | N/A | 3 | P:0x12 | EOnCE Receive Register Full |
| PMC | 10 | 0x0A | 0 | P:0x14 | Low-Voltage Detector |
| PLL | 11 | 0x0B | 0 | P:0x16 | Phase-Locked Loop Loss of Locks and Loss of Clock |
| ADCA | 12 | 0x0C | 0 | P:0x18 | ADCA Conversion Complete |
| ADCB | 13 | 0x0D | 0 | P:0x1A | ADCB Conversion Complete |
| PWM | 14 | 0x0E | 0 | P:0x1C | Reload PWM and/or PWM Faults |
| CMP0 | 15 | 0x0F | 0 | P:0x1E | Comparator 0 Rising/Falling Flag |
| CMP1 | 16 | 0x10 | 0 | P:0x20 | Comparator 1 Rising/Falling Flag |
| CMP2 | 17 | 0x11 | 0 | P:0x22 | Comparator 2 Rising/Falling Flag |
| FM | 18 | 0x12 | 0 | P:0x24 | Flash Memory Access Status |
| SPI | 19 | 0x13 | 0 | P:0x26 | SPI Receiver Full |
| SPI | 20 | 0x14 | 0 | P:0x28 | SPI Transmitter Empty |
| SCI | 21 | 0x15 | 0 | P:0x2A | SCI Transmitter Empty/Idle |
| SCI | 22 | 0x16 | 0 | P:0x2C | SCI Receiver Full/Overrun/Errors |
| I ² C | 23 | 0x17 | 0 | P:0x2E | I ² C Interrupt |
| PIT | 24 | 0x18 | 0 | P:0x30 | Interval Timer Interrupt |
| TMR0 | 25 | 0x19 | 0 | P:0x32 | Dual Timer, Channel 0 Interrupt |
| TMR1 | 26 | 0x1A | 0 | P:0x34 | Dual Timer, Channel 1 Interrupt |
| GPIOA | 27 | 0x1B | 0 | P:0x36 | GPIOA Interrupt |
| GPIOB | 28 | 0x1C | 0 | P:0x38 | GPIOB Interrupt |
| GPIOC | 29 | 0x1D | 0 | P:0x3A | GPIOC Interrupt |
| GIPOD | 30 | 0x1E | 0 | P:0x3C | GIPOD Interrupt |
| GPIOE | 29 | 0x1F | 0 | P:0x3E | GPIOE Interrupt |
| GPIOF | 30 | 0x20 | 0 | P:0x40 | GPIOF Interrupt |
| RTC | 33 | 0x21 | 0 | P:0x42 | Real Time Clock |

Table 43. Interrupt Vector Table Contents¹ (continued)

| Peripheral | Vector Number | User Encoding | Priority Level | Vector Base Address + | Interrupt Function |
|--------------------|---------------|---------------|----------------|-----------------------|--|
| Reserved | 34- 39 | 0x22-0x27 | 0 | P:0x44 - P:0x4E | Reserved |
| core | 40 | N/A | 0 | P:0x50 | SW Interrupt 0 |
| core | 41 | N/A | 1 | P:0x52 | SW Interrupt 1 |
| core | 42 | N/A | 2 | P:0x54 | SW Interrupt 2 |
| core | 43 | N/A | 3 | P:0x56 | SW Interrupt 3 |
| SWILP | 44 | N/A | -1 | P:0x58 | SW Interrupt Low Priority |
| USER1 | 45 | N/A | 1 | P:0x5A | User Programmable Priority Level 1 Interrupt |
| USER2 | 46 | N/A | 1 | P:0x5C | User Programmable Priority Level 1 Interrupt |
| USER3 | 47 | N/A | 1 | P:0x5E | User Programmable Priority Level 1 Interrupt |
| USER4 | 48 | N/A | 2 | P:0x60 | User Programmable Priority Level 2 Interrupt |
| USER5 | 49 | N/A | 2 | P:0x62 | User Programmable Priority Level 2 Interrupt |
| USER6 ³ | 50 | N/A | 2 | P:0x64 | User Programmable Priority Level 2 Interrupt |

¹ Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.

² If the VBA is set to the reset value, the first two locations of the vector table overlay the chip reset addresses because the reset address would match the base of this vector table.

³ USER6 vector can be defined as a fast interrupt if the instruction located in this vector location is not a JSR or BSR instruction. Please see section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for detail.

Appendix B

Peripheral Register Memory Map and Reset Value

NOTE

In Table 44, ADC0 stands for ADCA, ADC1 stands for ADCB, and GPIO_n is the same as GPIO_n (for example, GPIOA_PUR is the same as GPIO_A_PUR).

Table 44. Detailed Peripheral Memory Map

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | |
|--------------------|-------------------|---------|-------------|-------------------|-------|-----|-------|-----|-------|-----|-------|--------------|------|------|--------|-------|---------|-----|-------|--|
| 00 | 0000 | TMR0 | TMR0_COMP1 | COMPARISON_1 | | | | | | | | | | | | | | | | |
| 01 | 0000 | TMR0 | TMR0_COMP2 | COMPARISON_2 | | | | | | | | | | | | | | | | |
| 02 | 0000 | TMR0 | TMR0_CAPT | CAPTURE | | | | | | | | | | | | | | | | |
| 03 | 0000 | TMR0 | TMR0_LOAD | LOAD | | | | | | | | | | | | | | | | |
| 04 | 0000 | TMR0 | TMR0_HOLD | HOLD | | | | | | | | | | | | | | | | |
| 05 | 0000 | TMR0 | TMR0_CNTR | COUNTER | | | | | | | | | | | | | | | | |
| 06 | 0000 | TMR0 | TMR0_CTRL | CM | | | PCS | | | | | SCS | | ONCE | LENGTH | DIR | Co_INIT | OM | | |
| 07 | 0000 | TMR0 | TMR0_SCTRL | TCF | TCFIE | TOF | TOFIE | IEF | IEFIE | IPS | INPUT | CAPTURE_MODE | MSTR | EEOF | VAL | FORCE | OPS | OEN | | |
| 08 | 0000 | TMR0 | TMR0_CMPLD1 | COMPARATOR_LOAD_1 | | | | | | | | | | | | | | | | |
| 09 | 0000 | TMR0 | TMR0_CMPLD2 | COMPARATOR_LOAD_2 | | | | | | | | | | | | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | |
|--------------------|-------------------|---------|-------------|-------------------|-------|-------|----------|-----|----------|-----|-------|--------------|--------|--------|------|--------|-------|-----|-------|--|
| 0A | 0000 | TMR0 | TMR0_CSCTRL | DBG_EN | | FAULT | ALT_LOAD | 0 | 0 | 0 | 0 | TCF2EN | TCF1EN | TCF2 | TCF1 | CL2 | | CL1 | | |
| 0B | 0000 | TMR0 | TMR0_FILT | 0 | 0 | 0 | 0 | 0 | FILT_CNT | | | FILT_PER | | | | | | | | |
| 0C–0E | — | TMR0 | Reserved | RESERVED | | | | | | | | | | | | | | | | |
| 0F | 000F | TMR0 | TMR_ENBL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ENBL | | | | |
| 10 | 0000 | TMR1 | TMR1_COMP1 | COMPARISON_1 | | | | | | | | | | | | | | | | |
| 11 | 0000 | TMR1 | TMR1_COMP2 | COMPARISON_2 | | | | | | | | | | | | | | | | |
| 12 | 0000 | TMR1 | TMR1_CAPT | CAPTURE | | | | | | | | | | | | | | | | |
| 13 | 0000 | TMR1 | TMR1_LOAD | LOAD | | | | | | | | | | | | | | | | |
| 14 | 0000 | TMR1 | TMR1_HOLD | HOLD | | | | | | | | | | | | | | | | |
| 15 | 0000 | TMR1 | TMR1_CNTR | COUNTER | | | | | | | | | | | | | | | | |
| 16 | 0000 | TMR1 | TMR1_CTRL | CM | | | PCS | | | | SCS | | ONCE | LENGTH | DIR | COINIT | OM | | | |
| 17 | 0000 | TMR1 | TMR1_SCTRL | TCF | TCFIE | TOF | TOFIE | IEF | IEFIE | IPS | INPUT | CAPTURE_MODE | | MSTR | EEOF | VAL | FORCE | OPS | OEN | |
| 18 | 0000 | TMR1 | TMR1_CMPLD1 | COMPARATOR_LOAD_1 | | | | | | | | | | | | | | | | |
| 19 | 0000 | TMR1 | TMR1_CMPLD2 | COMPARATOR_LOAD_2 | | | | | | | | | | | | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|-------------|----------|--------|---------|----------|---------|----------|---------|---------|----------|--------|--------|--------|-------|--------|------|--------|
| 1A | 0000 | TMR1 | TMR1_CSCTRL | DBG_EN | | FAULT | ALT_LOAD | 0 | 0 | 0 | 0 | TCF2EN | TCF1EN | TCF2 | TCF1 | CL2 | | CL1 | |
| 1B | 0000 | TMR1 | TMR1_FILT | 0 | 0 | 0 | 0 | 0 | FILT_CNT | | | FILT_PER | | | | | | | |
| 1C-1F | — | TMR1 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 20 | 0000 | PWM | PWM_CTRL | LDFQ | | | | HALF | IPOL2 | IPOL1 | IPOL0 | PRSC | | PWMRIE | PWMF | ISENS | | LDOK | PWMEN |
| 21 | 0000 | PWM | PWM_FCTRL | 0 | 0 | 0 | 0 | FPOL3 | FPOL2 | FPOL1 | FPOL0 | FIE3 | FMODE3 | FIE2 | FMODE2 | FIE1 | FMODE1 | FIE0 | FMODE0 |
| 22 | 0000 | PWM | PWM_FLTACK | FPIN3 | FFLAG3 | FPIN2 | FFLAG2 | FPIN1 | FFLAG1 | FPIN0 | FFLAG0 | | FTACK3 | | FTACK2 | | FTACK1 | | FTACK0 |
| 23 | 0000 | PWM | PWM_OUT | PAD_EN | 0 | OUTCTL5 | OUTCTL4 | OUTCTL3 | OUTCTL2 | OUTCTL1 | OUTCTL0 | 0 | 0 | OUT5 | OUT4 | OUT3 | OUT2 | OUT1 | OUT0 |
| 24 | 0000 | PWM | PWM_CNTR | 0 | CR | | | | | | | | | | | | | | |
| 25 | 0000 | PWM | PWM_CMOD | 0 | PWMCM | | | | | | | | | | | | | | |
| 26 | 0000 | PWM | PWM_VAL0 | PMVAL | | | | | | | | | | | | | | | |
| 27 | 0000 | PWM | PWM_VAL1 | PMVAL | | | | | | | | | | | | | | | |
| 28 | 0000 | PWM | PWM_VAL2 | PMVAL | | | | | | | | | | | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|------------|-------------|--------|---------|-------|--------|----------|----------|----------|--------------|----------|----------|----------|---------|---------|---------|-------|
| 29 | 0000 | PWM | PWM_VAL3 | PMVAL | | | | | | | | | | | | | | | |
| 2A | 0000 | PWM | PWM_VAL4 | PMVAL | | | | | | | | | | | | | | | |
| 2B | 0000 | PWM | PWM_VAL5 | PMVAL | | | | | | | | | | | | | | | |
| 2C | 0FFF | PWM | PWM_DTIM0 | 0 | 0 | 0 | 0 | PWMDT0 | | | | | | | | | | | |
| 2D | 0FFF | PWM | PWM_DTIM1 | 0 | 0 | 0 | 0 | PWMDT1 | | | | | | | | | | | |
| 2E | FFFF | PWM | PWM_DMAP1 | DISMAP_15_0 | | | | | | | | | | | | | | | |
| 2F | 00FF | PWM | PWM_DMAP2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DISMAP_23_16 | | | | | | | |
| 30 | 0000 | PWM | PWM_CNFG | 0 | DBG_EN | WAIT_EN | EDG | 0 | TOPNEG45 | TOPNEG23 | TOPNEG01 | 0 | BOTNEG45 | BOTNEG23 | BOTNEG01 | INDEP45 | INDEP23 | INDEP01 | WP |
| 31 | 0000 | PWM | PWM_CCTRL | ENHA | nBX | MSK5 | MSK4 | MSK3 | MSK2 | MSK1 | MSK0 | 0 | 0 | VLMODE | | 0 | SWP45 | SWP23 | SWP01 |
| 32 | 00-U ¹ | PWM | PWM_PORT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PORT | | | | | | |
| 33 | 0000 | PWM | PWM_ICCTRL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PEC2 | PEC1 | PEC0 | ICC2 | ICC1 | ICC0 |
| 34 | 0000 | PWM | PWM_SCTRL | 0 | 0 | CINV5 | CINV4 | CINV3 | CINV2 | CINV1 | CINV0 | 0 | SRC2 | | 0 | SRC1 | | 0 | SRC0 |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|--------------|-------------|-------------|---------------------|-----|----|-----------|---|---|----------------|------|------|-------|------|--------|---|-------|
| 35 | 0000 | PWM | PWM_SYNC | SYNC_OUT_EN | SYNC_WINDOW | | | | | | | | | | | | | | |
| 36 | 0000 | PWM | PWM_FFILT0 | GSTR0 | 0 | 0 | 0 | 0 | FILT0_CNT | | | FILT0_PER | | | | | | | |
| 37 | 0000 | PWM | PWM_FFILT1 | GSTR1 | 0 | 0 | 0 | 0 | FILT1_CNT | | | FILT1_PER | | | | | | | |
| 38 | 0000 | PWM | PWM_FFILT2 | GSTR2 | 0 | 0 | 0 | 0 | FILT2_CNT | | | FILT2_PER | | | | | | | |
| 39 | 0000 | PWM | PWM_FFILT3 | GSTR3 | 0 | 0 | 0 | 0 | FILT3_CNT | | | FILT3_PER | | | | | | | |
| 3B–3F | — | PWM | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 40 | 0000 | INTC | INTC_ICSR | INT | IPIC | | VAB | | | | | INT_DIS | ERRF | ETRE | TRBUF | BKPT | STPCNT | | |
| 41 | 0000 | INTC | INTC_VBA | 0 | 0 | VECTOR_BASE_ADDRESS | | | | | | | | | | | | | |
| 42 | 0000 | INTC | INTC_IAR0 | 0 | 0 | USER2 | | | | 0 | 0 | USER1 | | | | | | | |
| 43 | 0000 | INTC | INTC_IAR1 | 0 | 0 | USER4 | | | | 0 | 0 | USER3 | | | | | | | |
| 44 | 0000 | INTC | INTC_IAR2 | 0 | 0 | USER6 | | | | 0 | 0 | USER5 | | | | | | | |
| 45–5F | — | INTC | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 60 | 001F | ADC0 | ADC0_ADCSC1A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CO CO CO | AIEN | ADCO | ADCH | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|--------------|----------|-------|-------|------|------|------|------|------|-------|-------|------|--------|------|-----|--------|-------|
| 61 | 0000 | ADC0 | ADC0_ADCSC2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ADACT | ADTRG | 0 | 0 | 0 | ECC | REFSEL | |
| 62–65 | — | ADC0 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 66 | 0000 | ADC0 | ADC0_ADCCFG | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ADLPC | ADIV | | ADLSMP | MODE | | ADICLK | |
| 67–69 | — | ADC0 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 6A | 001F | ADC0 | ADC0_ADCSC1B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | COCO | AIEN | ADCO | ADCH | | | | |
| 6B | 0000 | ADC0 | ADC0_ADCRA | 0 | ADR11 | ADR10 | ADR9 | ADR8 | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 | 0 | 0 | 0 |
| 6C | 0000 | ADC0 | ADC0_ADCRB | 0 | ADR11 | ADR10 | ADR9 | ADR8 | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 | 0 | 0 | 0 |
| 6D–6F | — | ADC0 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 80 | 001F | ADC1 | ADC1_ADCSC1A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | COCO | AIEN | ADCO | ADCH | | | | |
| 81 | 0000 | ADC1 | ADC1_ADCSC2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ADACT | ADTRG | 0 | 0 | 0 | ECC | REFSEL | |
| 82–85 | — | ADC1 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 86 | 0000 | ADC1 | ADC1_ADCCFG | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ADLPC | ADIV | | ADLSMP | MODE | | ADICLK | |
| 87–89 | — | ADC1 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 8A | 001F | ADC1 | ADC1_ADCSC1B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | COCO | AIEN | ADCO | ADCH | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|------------|----------|-------|-------|------|------|------|------|------|-------|---------|--------|------------|------|-----|---------|--------|
| 8B | 0000 | ADC1 | ADC1_ADCRA | 0 | ADR11 | ADR10 | ADR9 | ADR8 | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 | 0 | 0 | 0 |
| 8C | 0000 | ADC1 | ADC1_ADCRB | 0 | ADR11 | ADR10 | ADR9 | ADR8 | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 | 0 | 0 | 0 |
| 8D–8F | — | ADC1 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| A0 | 0000 | PGA0 | PGA0_CNTL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TM | GAINSEL | | | | LP | EN | |
| A1 | 0002 | PGA0 | PGA0_CNTL1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PPDIS | PARMODE | 0 | CALMODE | | CPD | | |
| A2 | 000E | PGA0 | PGA0_CNTL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SWTRIG | NUM_CLK_GS | | | ADIV | |
| A3 | 0000 | PGA0 | PGA0_STS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RUNNING | STCOMP |
| A4–BF | — | PGA0 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| C0 | 0000 | PGA1 | PGA1_CNTL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TM | GAINSEL | | | | LP | EN | |
| C1 | 0002 | PGA1 | PGA1_CNTL1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PPDIS | PARMODE | 0 | CALMODE | | CPD | | |
| C2 | 000E | PGA1 | PGA1_CNTL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SWTRIG | NUM_CLK_GS | | | ADIV | |



Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|-------------|----------|-------|------|-------|--------|----------|---------|-----------------------|---------|----------|----------|-------|----------|------|----------|--------|
| C3 | 0000 | PGA1 | PGA1_STS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RUNNING | STCOMP |
| C4–DF | — | PGA1 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| E0 | 0200 | SCI | SCI_RATE | SBR | | | | | | | | | | | | | | FRAC_SBR | |
| E1 | 0000 | SCI | SCI_CTRL1 | LOOP | SWAI | RSRC | M | WAKE | POL | PE | PT | TEIE | TIIE | RFIE | REIE | TE | RE | RWU | SBK |
| E2 | 0000 | SCI | SCI_CTRL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LIN_MODE | 0 | 0 | 0 |
| E3 | C000 | SCI | SCI_STAT | TDRE | TIDLE | RDRF | RIDLE | OR | NF | FE | PF | 0 | 0 | 0 | 0 | LSE | 0 | 0 | RAF |
| E4 | 0000 | SCI | SCI_DATA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RECEIVE_TRANSMIT_DATA | | | | | | | | |
| E5–FF | — | SCI | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 00 | 6141 | SPI | SPI_SCTRL | SPR | | | DSO | ERRIE | MODFEN | SPRIE | SPMSTR | CPOL | CPHA | SPE | SPTIE | SPRF | OVRF | MODF | SPTE |
| 01 | 000F | SPI | SPI_DSCTRL | WOM | 0 | 0 | BD2X | SSB_IN | SSB_DATA | SSB_ODM | SSB_AUTO | SSB_DDR | SSB_STRB | SSB_OVER | SPR3 | DS | | | |
| 02 | 0000 | SPI | SPI_DRCV | R15 | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |
| 03 | 0000 | SPI | SPI_DXMIT | T15 | T14 | T13 | T12 | T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
| 04–1F | — | SPI | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 20 | 0000 | I2C | I2C_ADDR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | 0 |
| 21 | 0000 | I2C | I2C_FREQDIV | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MULT | | ICR | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|-------------|---------------|----|----|----|----|----|-----|---|----------|----------|---------|--------|--------|--------|-------|-------|
| 22 | 0000 | I2C | I2C_CR1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IICEN | IICIE | MST | TX | TXAK | RSTA | 0 | 0 |
| 23 | 0080 | I2C | I2C_SR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TCF | IAAS | BUSY | ARBL | 0 | SRW | IICIF | RXAK |
| 24 | 0000 | I2C | I2C_DATA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DATA | | | | | | | |
| 25 | 0000 | I2C | I2C_CR2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GCAEN | ADEXT | 0 | 0 | 0 | AD10 | AD9 | AD8 |
| 26 | 0000 | I2C | I2C_SMB_CSR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RESERVED | RESERVED | SIICAEN | TCKSEL | SLTF | SHTF | 0 | 0 |
| 27 | 0000 | I2C | I2C_ADDR2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SAD7 | SAD6 | SAD5 | SAD4 | SAD3 | SAD2 | SAD1 | 0 |
| 28 | 0000 | I2C | I2C_SLT1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSLT15 | SSLT14 | SSLT13 | SSLT12 | SSLT11 | SSLT10 | SSLT9 | SSLT8 |
| 29 | 0000 | I2C | I2C_SLT2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSLT7 | SSLT6 | SSLT5 | SSLT4 | SSLT3 | SSLT2 | SSLT1 | SSLT0 |
| 30–3F | — | I2C | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 40 | 0302 | COP | COP_CTRL | 0 | 0 | 0 | 0 | 0 | 0 | PSS | 0 | CLKSEL | CLOREN | CSEN | CWEN | CEN | CWP | | |
| 41 | FFFF | COP | COP_TOUT | TIMEOUT | | | | | | | | | | | | | | | |
| 42 | FFFF | COP | COP_CNTR | COUNT_SERVICE | | | | | | | | | | | | | | | |
| 43–5F | — | COP | Reserved | RESERVED | | | | | | | | | | | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | |
|--------------------|-------------------|---------|--------------|----------|---------------|--------|----------|-------|---------|------|---|-------|------------|-------|--------|-------|----------|------|-------|---|
| 60 | 0011 | OCCS | OCCS_CTRL | PLLIE1 | | PLLIE0 | | LOCIE | 0 | 0 | 0 | LCKON | 0 | 0 | PLLPD | 0 | PRECS | ZSRC | | |
| 61 | 2000 | OCCS | OCCS_DIVBY | LORTP | | | | COD | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 62 | 0015 | OCCS | OCCS_STAT | LOLI1 | LOLIO | LOCI | 0 | 0 | 0 | 0 | 0 | 0 | LCK1 | LCK0 | PLLPDN | 0 | COSC_RDY | ZSRC | | |
| 64 | 1611 | OCCS | OCCS_OCTRL | ROPD | ROSB | COHL | CLK_MODE | RANGE | EXT_SEL | TRIM | | | | | | | | | | |
| 65 | 0000 | OCCS | OCCS_CLKCHKR | CHK_ENA | REFERENCE_CNT | | | | | | | | | | | | | | | |
| 66 | 0000 | OCCS | OCCS_CLKCHKT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TARGET_CNT | | | | | | | |
| 67 | 0000 | OCCS | OCCS_PROT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FRQEP | OSCEP | PLLEP | | | | |
| 68–7F | — | OCCS | Reserved | RESERVED | | | | | | | | | | | | | | | | |
| 80 | 00FF | GPIOA | GPIOA_PUR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PU | | | | | | | | |
| 81 | 0000 | GPIOA | GPIOA_DR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D | | | | | | | | |
| 82 | 0000 | GPIOA | GPIOA_DDR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DD | | | | | | | | |
| 83 | 0080 | GPIOA | GPIOA_PER | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PE | | | | | | | | |
| 84 | — | GPIOA | Reserved | RESERVED | | | | | | | | | | | | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|---------------|----------|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|-------|
| 85 | 0000 | GPIOA | GPIOA_IENR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IEN | | | | | | | |
| 86 | 0000 | GPIOA | GPIOA_IPOLR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IPOL | | | | | | | |
| 87 | 0000 | GPIOA | GPIOA_IPR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IP | | | | | | | |
| 88 | 0000 | GPIOA | GPIOA_IESR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IES | | | | | | | |
| 89 | — | GPIOA | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 8A | 0000 | GPIOA | GPIOA_RAWDATA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RAWDATA | | | | | | | |
| 8B | 0000 | GPIOA | GPIOA_DRIVE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DRIVE | | | | | | | |
| 8C | 00FF | GPIOA | GPIOA_IFE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IFE | | | | | | | |
| 8D | 0000 | GPIOA | GPIOA_SLEW | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLEW | | | | | | | |
| 8E–9F | — | GPIOA | Reserved | RESERVED | | | | | | | | | | | | | | | |
| A0 | 00FF | GPIOB | GPIOB_PUR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PUR | | | | | | | |
| A1 | 0000 | GPIOB | GPIOB_DR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DR | | | | | | | |
| A2 | 0000 | GPIOB | GPIOB_DDR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDR | | | | | | | |
| A3 | 0080 | GPIOB | GPIOB_PER | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PER | | | | | | | |
| A4 | — | GPIOB | Reserved | RESERVED | | | | | | | | | | | | | | | |
| A5 | 0000 | GPIOB | GPIOB_IENR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IENR | | | | | | | |
| A6 | 0000 | GPIOB | GPIOB_IPOLR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IPOLR | | | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|---------------|----------|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|-------|
| A7 | 0000 | GPIOB | GPIOB_IPR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IPR | | | | | | | |
| A8 | 0000 | GPIOB | GPIOB_IESR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IESR | | | | | | | |
| A9 | — | GPIOB | Reserved | RESERVED | | | | | | | | | | | | | | | |
| AA | 0000 | GPIOB | GPIOB_RAWDATA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RAWDATA | | | | | | | |
| AB | 0000 | GPIOB | GPIOB_DRIVE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DRIVE | | | | | | | |
| AC | 00FF | GPIOB | GPIOB_IFE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IFE | | | | | | | |
| AD | 0000 | GPIOB | GPIOB_SLEW | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLEW | | | | | | | |
| AE–BF | — | GPIOB | Reserved | RESERVED | | | | | | | | | | | | | | | |
| C0 | 00FF | GPIOC | GPIOC_PUR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PUR | | | | | | | |
| C1 | 0000 | GPIOC | GPIOC_DR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DR | | | | | | | |
| C2 | 0000 | GPIOC | GPIOC_DDR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDR | | | | | | | |
| C3 | 0080 | GPIOC | GPIOC_PER | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PER | | | | | | | |
| C4 | — | GPIOC | Reserved | RESERVED | | | | | | | | | | | | | | | |
| C5 | 0000 | GPIOC | GPIOC_IENR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IENR | | | | | | | |
| C6 | 0000 | GPIOC | GPIOC_IPOLR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IPOLR | | | | | | | |
| C7 | 0000 | GPIOC | GPIOC_IPR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IPR | | | | | | | |
| C8 | 0000 | GPIOC | GPIOC_IESR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IESR | | | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|---------------|----------|----|----|----|----|----|---|---|---------|---|---|---|---------|---|---|-------|
| C9 | — | GPIOC | Reserved | RESERVED | | | | | | | | | | | | | | | |
| CA | 0000 | GPIOC | GPIOC_RAWDATA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RAWDATA | | | | | | | |
| CB | 0000 | GPIOC | GPIOC_DRIVE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DRIVE | | | | | | | |
| CC | 00FF | GPIOC | GPIOC_IFE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IFE | | | | | | | |
| CD | 0000 | GPIOC | GPIOC_SLEW | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLEW | | | | | | | |
| CE-DF | — | GPIOC | Reserved | RESERVED | | | | | | | | | | | | | | | |
| E0 | 00FF | GPIOD | GPIOD_PUR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PUR | | | |
| E1 | 0000 | GPIOD | GPIOD_DR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DR | | | |
| E2 | 0000 | GPIOD | GPIOD_DDR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDR | | | |
| E3 | 0080 | GPIOD | GPIOD_PER | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PER | | | |
| E4 | — | GPIOD | Reserved | RESERVED | | | | | | | | | | | | | | | |
| E5 | 0000 | GPIOD | GPIOD_IENR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IENR | | | |
| E6 | 0000 | GPIOD | GPIOD_IPOLR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IPOLR | | | |
| E7 | 0000 | GPIOD | GPIOD_IPR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IPR | | | |
| E8 | 0000 | GPIOD | GPIOD_IESR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IESR | | | |
| E9 | — | GPIOD | Reserved | RESERVED | | | | | | | | | | | | | | | |
| EA | 0000 | GPIOD | GPIOD_RAWDATA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RAWDATA | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|---------------|----------|----|----|----|----|----|---|---|---------|---|---|---|-------|---|---|-------|
| EB | 0000 | GPIOD | GPIOD_DRIVE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DRIVE | | | |
| EC | 00FF | GPIOD | GPIOD_IFE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IFE | | | |
| ED | 0000 | GPIOD | GPIOD_SLEW | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLEW | | | |
| EE-9F | — | GPIOD | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 00 | 00FF | GPIOE | GPIOE_PUR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PUR | | | | | | | |
| 01 | 0000 | GPIOE | GPIOE_DR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DR | | | | | | | |
| 02 | 0000 | GPIOE | GPIOE_DDR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDR | | | | | | | |
| 03 | 0080 | GPIOE | GPIOE_PER | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PER | | | | | | | |
| 04 | — | GPIOE | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 05 | 0000 | GPIOE | GPIOE_IENR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IENR | | | | | | | |
| 06 | 0000 | GPIOE | GPIOE_IPOLR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IPOLR | | | | | | | |
| 07 | 0000 | GPIOE | GPIOE_IPR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IPR | | | | | | | |
| 08 | 0000 | GPIOE | GPIOE_IESR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IESR | | | | | | | |
| 09 | — | GPIOE | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 0A | 0000 | GPIOE | GPIOE_RAWDATA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RAWDATA | | | | | | | |
| 0B | 0000 | GPIOE | GPIOE_DRIVE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DRIVE | | | | | | | |
| 0C | 00FF | GPIOE | GPIOE_IFE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IFE | | | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|---------------|----------|----|----|----|----|----|---|---|------|---|---|---|---------|---|---|-------|
| 0D | 0000 | GPIOE | GPIOE_SLEW | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLEW | | | | | | | |
| 0E–1F | — | GPIOE | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 20 | 00FF | GPIOF | GPIOF_PUR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PUR | | | |
| 21 | 0000 | GPIOF | GPIOF_DR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DR | | | |
| 22 | 0000 | GPIOF | GPIOF_DDR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDR | | | |
| 23 | 0080 | GPIOF | GPIOF_PER | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PER | | | |
| 24 | — | GPIOF | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 25 | 0000 | GPIOF | GPIOF_IENR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IENR | | | |
| 26 | 0000 | GPIOF | GPIOF_IPOLR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IPOLR | | | |
| 27 | 0000 | GPIOF | GPIOF_IPR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IPR | | | |
| 28 | 0000 | GPIOF | GPIOF_IESR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IESR | | | |
| 29 | — | GPIOF | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 2A | 0000 | GPIOF | GPIOF_RAWDATA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RAWDATA | | | |
| 2B | 0000 | GPIOF | GPIOF_DRIVE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DRIVE | | | |
| 2C | 00FF | GPIOF | GPIOF_IFE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IFE | | | |
| 2D | 0000 | GPIOF | GPIOF_SLEW | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLEW | | | |
| 2E–3F | — | GPIOF | Reserved | RESERVED | | | | | | | | | | | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|------------|------------|------|---------|--------|------|----------|------|--------|--------|-----|---------|----------|--------------|--------|--------------|-------|
| 40 | 0000 | SIM | SIM_CTRL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ONCEEBL | SW_RST | STOP_DISABLE | | WAIT_DISABLE | |
| 41 | 0001 | SIM | SIM_RSTAT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SWR | COP_CPU | COP_LOR | EXTR | LVDR | PPD | POR |
| 42 | 01F2 | SIM | SIM_MSHID | SIM_MSH_ID | | | | | | | | | | | | | | | |
| 43 | 601D | SIM | SIM_LSHID | SIM_LSH_ID | | | | | | | | | | | | | | | |
| 45 | 2020 | SIM | SIM_CLKOUT | 0 | 0 | CLKDIS1 | 0 | 0 | CLKOSEL1 | | | 0 | 0 | CLKDIS0 | CLKOSEL0 | | | | |
| 46 | 0000 | SIM | SIM_PCR | TMR_CR | 0 | PWM_CR | SCI_CR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 47 | 0000 | SIM | SIM_PCE | CMP2 | CMP1 | CMP0 | ADC1 | ADC0 | PGA1 | PGA0 | I2C | SCI | SPI | PWM | COP | PDB | PIT | TA1 | TA0 |
| 48 | 0000 | SIM | SIM_SDR | CMP2 | CMP1 | CMP0 | ADC1 | ADC0 | PGA1 | PGA0 | I2C | SCI | SPI | PWM | COP | PDB | PIT | TA1 | TA0 |
| 49 | F000 | SIM | SIM_ISAL | ADDR_15_6 | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 |
| 4A | 0000 | SIM | SIM_PROT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PCEP | | GIPSP | |
| 4B | 0000 | SIM | SIM_GPSA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GPS_A6 | | | GPS_A5 | | GPS_A4 | | GPS_A3 | |
| 4C | 0000 | SIM | SIM_GPSB0 | GPS_B5 | | GPS_B4 | | | GPS_B3 | | | GPS_B2 | | 0 | GPS_B1 | | GPS_B0 | | |
| 4D | 0000 | SIM | SIM_GPSB1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GPS_B7 | | GPS_B6 | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|----------|----------|-----------|------|------|------------|------------|------------|-----------|----------|------------|-----------|--------|--------|-----------|--------|--------|
| 4E | 0000 | SIM | SIM_GPSC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GPS_C6 | GPS_C0 |
| 4F | 0000 | SIM | SIM_GPSD | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GPS_D3 | | GPS_D2 | | GPS_D1 | | GPS_D0 | | |
| 50 | 0000 | SIM | SIM_IPS0 | 0 | 0 | 0 | 0 | IPS_FAULT3 | IPS_FAULT2 | IPS_FAULT1 | IPS_PSRC2 | | | IPS_PSRC1 | | | IPS_PSRC0 | | |
| 51 | 0000 | SIM | SIM_IPS1 | 0 | IPS_C2_WS | | | IPS_C1_WS | | | IPS_C0_WS | | | IPS_T1 | | IPS_T0 | | | |
| 52–5F | — | SIM | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 60 | 0208 | PMC | PMC_SCR | OORF | LVDF | PPDF | PORF | OORIE | LVDIE | LVDRE | PPDE | LPR | LPRS | LPWUI | BGBE | LVDE | LVLS | PROT | |
| 61 | 00– ² | PMC | PMC_CR2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LPO_EN | LPO_TRIM | | | TRIM | | | | |
| 7F | — | PMC | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 80 | 0000 | CMP0 | CMP0_CR0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FILTER_CNT | | | PMC | | MMC | |
| 81 | 0000 | CMP0 | CMP0_CR1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SE | WE | 0 | P.MODE | INV | COS | OPE | EN |
| 82 | 0000 | CMP0 | CMP0_FPR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FILT_PER | | | | | | | |
| 83 | 0000 | CMP0 | CMP0_SCR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IER | IEF | CFR | CFF | COUT |
| 84–9F | — | CMP0 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| A0 | 0000 | CMP1 | CMP1_CR0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FILTER_CNT | | | PMC | | MMC | |



Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|------------|---------------|----|----|----|-----|----|---|-----|----------|------------|--------|---------|-----|-----|------|--------|
| A1 | 0000 | CMP1 | CMP1_CR1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SE | WE | 0 | PMODE | INV | COS | OPE | EN |
| A2 | 0000 | CMP1 | CMP1_FPR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FILT_PER | | | | | | | |
| A3 | 0000 | CMP1 | CMP1_SCR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IER | IEF | CFR | CFF | COUT |
| A4–BF | — | CMP1 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| C0 | 0000 | CMP2 | CMP2_CR0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FILTER_CNT | | | PMC | | MMC | |
| C1 | 0000 | CMP2 | CMP2_CR1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SE | WE | 0 | PMODE | INV | COS | OPE | EN |
| C2 | 0000 | CMP2 | CMP2_FPR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FILT_PER | | | | | | | |
| C3 | 0000 | CMP2 | CMP2_SCR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IER | IEF | CFR | CFF | COUT |
| C4–DF | — | CMP2 | Reserved | RESERVED | | | | | | | | | | | | | | | |
| E0 | 0000 | PIT | PIT_CTRL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PRESCALER | | | | PRF | PRIE | CNT_EN |
| E1 | 0000 | PIT | PIT_MOD | MODULO_VALUE | | | | | | | | | | | | | | | |
| E2 | 0000 | PIT | PIT_CNTR | COUNTER_VALUE | | | | | | | | | | | | | | | |
| E3–FF | — | PIT | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 00 | 0000 | PDB | PDB_SCR | PRESCALER | | | 0 | AOS | | 0 | BOS | | CONT | SWTRIG | TRIGSEL | | | ENA | ENB |
| 01 | 0000 | PDB | PDB_DELAYA | DELAYA | | | | | | | | | | | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|------------|----------|---------|----|----|----|------|---|--------|-------|--------|--------|--------|---|-------|------|-------|
| 02 | 0000 | PDB | PDB_DELAYB | DELAYB | | | | | | | | | | | | | | | |
| 03 | FFFF | PDB | PDB_MOD | MOD | | | | | | | | | | | | | | | |
| 04 | FFFF | PDB | PDB_COUNT | COUNT | | | | | | | | | | | | | | | |
| 05–1F | — | PDB | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 20 | 0000 | RTC | RTC_SC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RTIF | RTCLKS | RTIE | RTCPS | | | | |
| 21 | 0000 | RTC | RTC_CNT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RTCCNT | | | | | | | | |
| 22 | 0000 | RTC | RTC_MOD | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RTCMOD | | | | | | | | |
| 23–FF | — | RTC | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 00 | 0000 | HFM | FM_CLKDIV | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DIVLD | PRDIV8 | DIV | | | | | |
| 01 | 0000 | HFM | FM_CNFG | 0 | 0 | 0 | 0 | 0 | LOCK | 0 | AEIE | CBEIE | CCIE | KEYACC | 0 | 0 | 0 | LBTS | BTS |
| 03 | -000 ³ | HFM | FM_SECHI | KEYEN | SECSTAT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 04 | 0000 | HFM | FM_SECLO | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SEC | |
| 06–0F | — | HFM | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 10 | FFFF ⁶ | HFM | FM_PROT | PROTECT | | | | | | | | | | | | | | | |
| 11 | — | HFM | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 13 | 00C0 | HFM | FM_USTAT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CBEIF | CCIF | PVIOL | ACCERR | 0 | BLANK | 0 | 0 |
| 14 | 0000 | HFM | FM_CMD | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CMD | | | | | | |

Table 44. Detailed Peripheral Memory Map (continued)

| Offset Addr. (Hex) | Reset Value (Hex) | Periph. | Register | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------------------|-------------------|---------|-----------|--------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| 17 | — | HFM | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 18 | 0000 | HFM | FM_DATA | FMDATA | | | | | | | | | | | | | | | |
| 19 | — | HFM | Reserved | RESERVED | | | | | | | | | | | | | | | |
| 1A | FFFF ⁴ | HFM | FM_OPT0 | IFR_OPT0 | | | | | | | | | | | | | | | |
| 1B | FFFF ⁵ | HFM | FM_OPT1 | IFR_OPT1 | | | | | | | | | | | | | | | |
| 1D | FFFF ⁶ | HFM | FM_TSTSIG | TST_AREA_SIG | | | | | | | | | | | | | | | |
| 1E–3F | — | HFM | Reserved | RESERVED | | | | | | | | | | | | | | | |

- ¹ The binary reset value of this register is 0000 0000 0UUU UUUU, where U represents an undefined value. Spaces have been added to the value for clarity.
- ² The binary reset value of this register is 0000 0000 111NC NC NC NC NC. Spaces have been added to the value for clarity.
- ³ The binary reset value of this register is FS00 0000 0000 0000, where F indicates that the reset state is loaded from the flash array during reset, and where S indicates that the reset state is determined by the security state of the module. Spaces have been added to the value for clarity.
- ⁴ The reset state is loaded from the flash array during reset.
- ⁵ The reset state is loaded from the flash array during reset.
- ⁶ The reset state is loaded from the flash array during reset.

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Document Number: MC56F8006

Rev. 4

06/2011