

# 0.4 A Dual H-Bridge Motor Driver IC

The 17C724 is a SMARTMOS compact monolithic dual channel H-Bridge power IC, ideal for portable electronic applications containing bipolar stepper motors or brush DC motors such as those used in camera lenses and shutters.

The 17C724 can operate efficiently with supply voltages from 2.7 V to 5.5 V and can provide continuous motor drive currents of 0.4 A with low  $R_{DS(on)}$  of 1.0  $\Omega$ . It is easily interfaced to low cost MCUs via parallel 3.0 V or 5.0 V compatible logic and has built-in shoot-through current protection circuit and undervoltage detector to avoid malfunction.

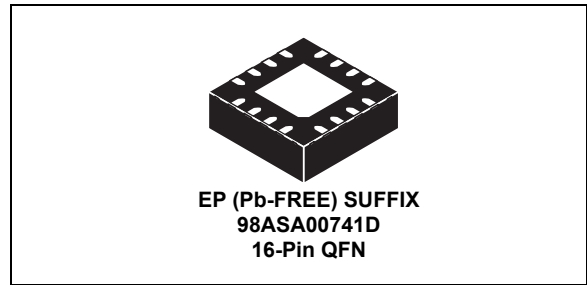
The 17C724 has four output control modes: forward, reverse, brake, and tri-state (high-impedance). The H-Bridge outputs are designed to be independently PWMed at up to 200 kHz for speed/torque and current control.

### Features

- Manufactured in SMOS7 process technology
- Built-in 2-channel H-Bridge driver
- Provides 4 driving modes (forward, reverse, brake, high-impedance)
- Direct interface to MCU
- Low ON-Resistance,  $R_{DS(on)} = 1.0 \Omega$  (typical)
- Dual channel parallel drive,  $R_{DS(on)} = 0.5 \Omega$  (typical)
- Output current driver is 400 mA (continuous)
- Low power consumption
- Built-in shoot-through current prevention circuit
- Built-in low voltage shutdown circuit
- PWM control frequency 200 kHz (max)
- Very compact size, comes in 16-pin QFN Package (3x3 mm pin Pitch: 0.5 mm)

**17C724**

**MOTOR DRIVER**



| ORDERING INFORMATION                            |                                     |         |
|---|-------------------------------------|---------|
| Device<br>(For Tape and Reel, add an R2 Suffix) | Temperature Range (T <sub>A</sub> ) | Package |
| MPC17C724EP                                     | -20 °C to 85 °C                     | 16 QFN  |

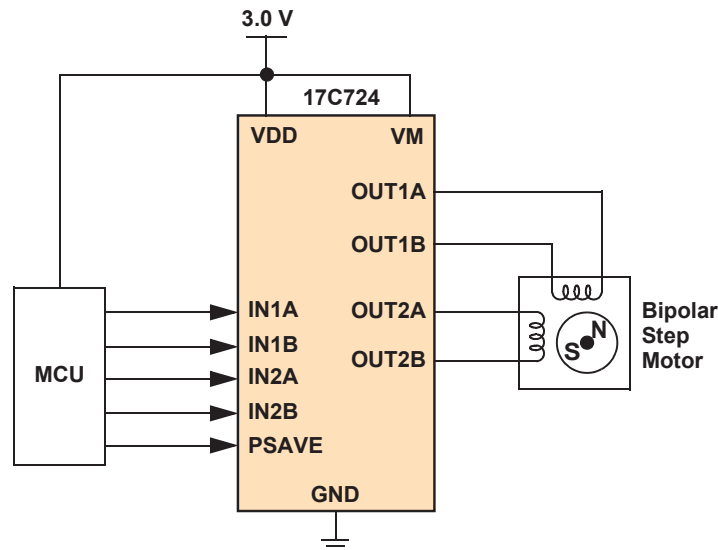


Figure 1. 17C724 Simplified Application Diagram

### INTERNAL BLOCK DIAGRAM

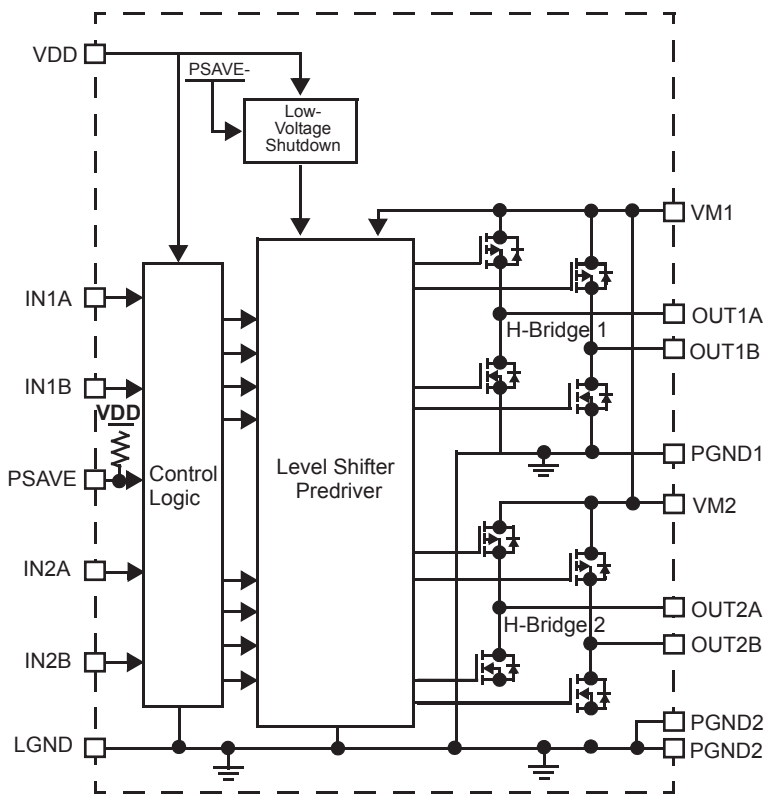
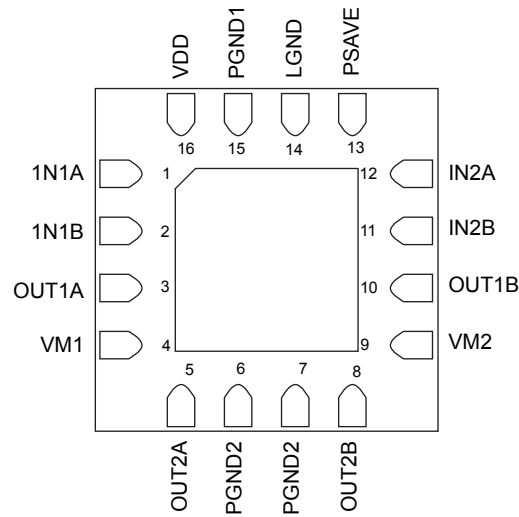


Figure 2. 17C724 Simplified Internal Block Diagram

## PIN CONNECTIONS

### Transparent Top View of Package



**Figure 3. 17C724 Pin Connections**

**Table 1. 17C724 Pin Definitions**

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 8](#).

| Pin Number | Pin Name | Pin Function | Formal Name                 | Definition  |
|------------|----------|--------------|-----------------------------|---|
| 1          | IN1A     | Logic        | Logic Input Control 1A      | Logic input control of OUT1A (refer to <a href="#">Table 5. Truth Table</a> , page <a href="#">Z</a> ). |
| 2          | IN1B     | Logic        | Logic Input Control 1B      | Logic input control of OUT1B (refer to <a href="#">Table 5. Truth Table</a> , page <a href="#">Z</a> ). |
| 3          | OUT1A    | Output       | H-Bridge Output 1A          | Output A of H-Bridge channel 1.   |
| 4          | VM1      | Power        | Motor Driver Power Supply 1 | Positive power source connection for H-Bridge 1 (Motor Driver Power Supply) <sup>(1)</sup> .            |
| 5          | OUT2A    | Output       | H-Bridge Output 2A          | Output A of H-Bridge channel 2.   |
| 6, 7       | PGND2    | Ground       | Power Ground 2              | High-current power ground 2 <sup>(2)</sup> .  |
| 8          | OUT2B    | Output       | H-Bridge Output 2B          | Output B of H-Bridge channel 2.   |
| 9          | VM2      | Power        | Motor Driver Power Supply 2 | Positive power source connection for H-Bridge 2 (Motor Driver Power Supply) <sup>(1)</sup> .            |
| 10         | OUT1B    | Output       | H-Bridge Output 1B          | Output B of H-Bridge channel 1.   |
| 11         | IN2B     | Input        | Logic Input Control 2B      | Logic input control of OUT2B (refer to <a href="#">Table 5. Truth Table</a> , page <a href="#">Z</a> ). |
| 12         | IN2A     | Input        | Logic Input Control 2A      | Logic input control of OUT2A (refer to <a href="#">Table 5. Truth Table</a> , page <a href="#">Z</a> ). |
| 13         | PSAVE    | Input        | Input Enable Control        | Logic input enable control of H-Bridges to save power.  |
| 14         | LGND     | Ground       | Logic Ground                | Low-current logic signal ground <sup>(2)</sup> .  |
| 15         | PGND1    | Ground       | Power Ground 1              | High-current power ground 1 <sup>(2)</sup> .  |
| 16         | VDD      | Logic        | Logic Circuit Power Supply  | Positive power source connection for logic circuit.   |

**Notes**

- VM1 and VM2 are internally connected.
- LGND, PGND1, and PGND2 are internally connected.

## MAXIMUM RATINGS

**Table 2. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings   | Symbol                              | Value                      | Unit |
|---|-------------------------------------|----------------------------|------|
| <b>ELECTRICAL RATINGS</b>   |                                     |                            |      |
| Power Supply Voltage (Motor Driver)<br>Normal Operation (Steady-State)<br>Transient Conditions <sup>(3)</sup>                           | $V_{M(SS)}$<br>$V_{M(PK)}$          | -0.3 to 6.0<br>-0.3 to 6.5 | V    |
| Logic Supply Voltage  | $V_{DD}$                            | 6.0                        | V    |
| Input Pin Voltage   | $V_{IN}$                            | -0.3 to $V_{DD} + 0.3$     | V    |
| Driver Output Current (Continuous) <sup>(4)</sup>   | $I_O$                               | 400                        | mA   |
| Driver Output Current (Peak) <sup>(5)</sup>   | $I_{OPK}$                           | 800                        | mA   |
| ESD Voltage <sup>(6)</sup><br>Human Body Model<br>Machine Model   | $V_{ESD1}$<br>$V_{ESD2}$            | $\pm 2000$<br>$\pm 200$    | V    |
| <b>TEMPERATURE RATINGS</b>  |                                     |                            |      |
| Storage Temperature   | $T_{STG}$                           | -40 to 150                 | °C   |
| Operating Temperature<br>Ambient  | $T_A$                               | -20 to 85                  | °C   |
| Operating Junction Temperature  | $T_J$                               | 150 maximum                | °C   |
| Thermal Resistance (Junction-to-Ambient)<br>Single-Layer PCB Mounting <sup>(9)</sup><br>Multi-Layer PCB (2S2P) Mounting <sup>(10)</sup> | $R_{\theta JA}$<br>$R_{\theta JMA}$ | 169<br>47                  | °C/W |
| Pin Soldering Temperature <sup>(7)</sup> , <sup>(8)</sup>   | $T_{PPRT}$                          | Note 8                     | °C   |

**Notes**

- Transient condition within 500 ms.
- Continuous output current must not be exceeded and at operating junction temperature below 150 °C.
- Peak time is for 10 ms pulse width at 200 ms intervals.
- ESD testing is performed in accordance with the Human Body Model ( $C_{ZAP}=100$  pF,  $R_{ZAP}=1500$   $\Omega$ ), **and** the Machine Model ( $C_{ZAP}=200$  pF,  $R_{ZAP}=0$   $\Omega$ ).
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxx enter 33xxx), and review parametrics.
- For cases using SEMI G38-87, JEDEC JESD51-2, JESD51-3, JESD51-5, single layer PCB mounting without thermal vias.
- For cases using SEMI JEDEC JESD51-6, JESD51-5, JESD51-7, 2S2P PCB mounting with 4 thermal vias.

## STATIC ELECTRICAL CHARACTERISTICS

**Table 3. Static Electrical Characteristics**

Characteristics noted under conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = V_M = 3.0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions unless otherwise noted.

| Characteristic   | Symbol        | Min          | Typ | Max          | Unit          |
|--|---------------|--------------|-----|--------------|---------------|
| <b>POWER INPUT (VDD, PSAVE)</b>                        |               |              |     |              |               |
| Supply Voltage Range                                   |               |              |     |              | V             |
| Motor Driver Supply Voltage                            | $V_M$         | 2.7          | 3.0 | 5.5          |               |
| Logic Supply Voltage                                   | $V_{DD}$      | 2.7          | 3.0 | 5.5          |               |
| Standby Power Supply Current <sup>(11)</sup>           |               |              |     |              | $\mu\text{A}$ |
| $V_M = 3.0\text{ V}$                                   | $I_{VMSTBY}$  | –            | –   | 1.0          |               |
| $V_{DD} = 3.0\text{ V}$                                | $I_{VDDSTBY}$ | –            | –   | 1.0          |               |
| Operating Power Supply Current <sup>(12)</sup>         |               |              |     |              | $\mu\text{A}$ |
| $V_{DD} = 3.0\text{ V}$                                | $I_C$         | –            | 40  | 100          |               |
| Logic Input Function                                   |               |              |     |              |               |
| High-Level Input Voltage                               | $V_{IH}$      | $V_{DD} 0.7$ | –   | –            | V             |
| Low-Level Input Voltage                                | $V_{IL}$      | –            | –   | $V_{DD} 0.3$ | V             |
| High-Level Input Current                               | $I_{IH}$      | –            | –   | 1.0          | $\mu\text{A}$ |
| Low-Level Input Current                                | $I_{IL}$      | -1.0         | –   | –            | $\mu\text{A}$ |
| PSAVE Pin Low Level Input Current <sup>(13)</sup>      | $I_{IL}$      | –            | -30 | -60          | $\mu\text{A}$ |
| Driver Output ON Resistance <sup>(14)</sup>            | $R_{DS(ON)}$  | –            | 1.0 | 1.5          | $\Omega$      |
| Low Voltage Shutdown Detection Voltage <sup>(15)</sup> | $V_{DDEET}$   | 1.5          | 2.0 | 2.5          | V             |

**Notes**

- Power SAVE mode.
- $I_C$  is the sum of the current of  $V_{DD}$  monitor block “Low Voltage Detection Module” and the PSAVE pull-up resistor at  $f_{IN} = 200\text{ kHz}$ .
- $V_{DD} = 3.0\text{ V}$ .
- $R_{SOURCE} + R_{SINK}$  at  $I_O = 375\text{ mA}$ .
- Detection voltage is defined as when the output becomes high impedance after  $V_{DD}$  voltage falls and when  $V_M = 5.5\text{ V}$ .

## DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 4. Dynamic Electrical Characteristics**

Characteristics noted under conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = V_M = 3.0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions unless otherwise noted.

| Characteristic                                | Symbol       | Min | Typ  | Max         | Unit          |
|---|--------------|-----|------|-------------|---------------|
| <b>INPUT</b>                                  |              |     |      |             |               |
| Pulse Input Frequency                         | $f_{IN}$     | –   | –    | 200         | kHz           |
| Input Pulse Rise Time <sup>(16)</sup>         | $t_R$        | –   | –    | 1.0<br>(17) | $\mu\text{s}$ |
| Input Pulse Fall Time <sup>(18)</sup>         | $t_F$        | –   | –    | 1.0<br>(17) | $\mu\text{s}$ |
| <b>OUTPUT</b>                                 |              |     |      |             |               |
| Output Propagation Delay Time <sup>(19)</sup> |              |     |      |             | $\mu\text{s}$ |
| Turn-ON Time                                  | $t_{PLH}$    | –   | 0.2  | 0.5         |               |
| Turn-OFF Time                                 | $t_{PHL}$    | –   | 0.1  | 0.5         |               |
| Low-Voltage Detection Time                    | $t_{VDDDET}$ | –   | 0.02 | 1.0         | ms            |

**Notes**

16. Time is defined between 10% and 90%.
17. That is, the input waveform slope must be steeper than this.
18. Time is defined between 90% and 10%.
19.  $R_L = 6.8\ \Omega$ . Slew time, rise time, and fall times are between 10% and 90% of output low and high levels with respect to the 50% level of the input.

## TIMING DIAGRAMS

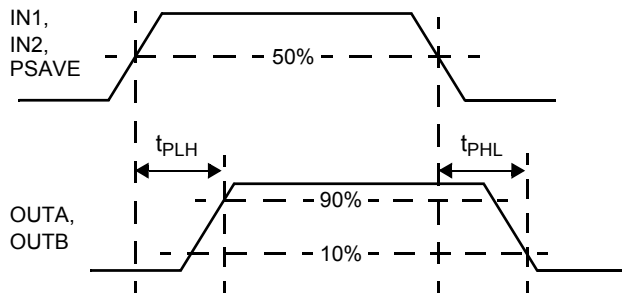
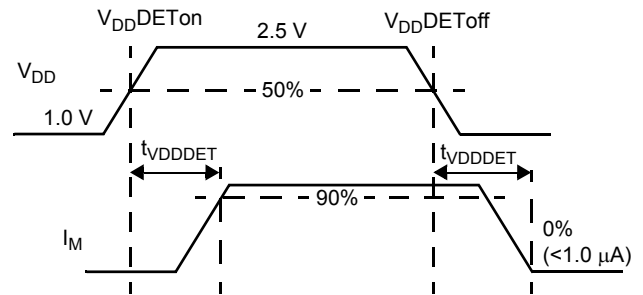

 Figure 4.  $t_{PLH}$  and  $t_{PHL}$  Timing


Figure 5. Low-Voltage Detection Timing

Table 5. Truth Table

| INPUT                 |              |              | OUTPUT         |                | $V_{DDDET}^{(21)}$ |
|-----------------------|--------------|--------------|----------------|----------------|--------------------|
| PSAVE <sup>(19)</sup> | IN1A<br>IN2A | IN1B<br>IN2B | OUT1A<br>OUT2A | OUT1B<br>OUT2B |                    |
| L                     | L            | L            | L              | L              | Enabled            |
| L                     | H            | L            | H              | L              | Enabled            |
| L                     | L            | H            | L              | H              | Enabled            |
| L                     | H            | H            | Z              | Z              | Enabled            |
| H                     | X            | X            | Z              | Z              | Disabled           |

H : High  
 L : Low  
 Z : High-impedance  
 X : Don't care

## Notes

20. Pin 13 (PSAVE) is pulled up by an internal resistor.
21. When  $V_{DD}$  is lower than  $V_{DDDET}$  while  $V_M$  is applied, output becomes "Z" (high-impedance); however, when PSAVE = "H", the low voltage shutdown detection circuit is disabled.

## FUNCTIONAL DESCRIPTION

### INTRODUCTION

The 17C724 is a monolithic dual H-Bridge that is ideal in portable electronic applications to control bipolar step motors and brush DC motors, such as those used in camera lens and shutters. The 17C724 can operate efficiently with supply voltages as low as 2.7 V to as high as 5.5 V, and provide continuous motor drive currents of 0.4 A while handling peak currents up to 0.8 A. It is easily interfaced to low cost MCUs via parallel 3.0 V or 5.0 V compatible logic. The device can be pulse width modulated (PWM'ed) at up to 200 kHz.

The 17C724 can drive two motors simultaneously (see [Figure 6](#)), or it can drive one bipolar step motor as shown in the simplified application diagram on [page 1](#). Dual channel

parallel drive is also possible if higher current drive is desired (0.8 A). Two-motor operation is accomplished by hooking one motor between OUT1A and OUT1B, and the other motor between OUT2A and OUT2B.

This IC has a built-in shoot-through current protection circuit and undervoltage detector to avoid malfunction. It also allows for power-conserving Sleep mode by the setting of the PSAVE pin (refer to [Table 5, Truth Table, page 7](#)).

The device features four operating modes: forward, reverse, brake, and tri-stated (high-impedance).

### FUNCTIONAL PIN DESCRIPTION

#### LOGIC CIRCUIT POWER SUPPLY (VDD)

The VDD pin carries the power source connection to the control (logic) circuit, and its input range is between 2.7 V to 5.5 V (3.0 V and 5.0 V compatible). V<sub>DD</sub> has an undervoltage threshold. If the supply voltage to V<sub>DD</sub> drops below 2.0 V (typical), then all the output of H-Bridges (OUT1A, OUT1B, OUT2A, OUT2B) will become open (high impedance = Z). When the supply voltage returns to a level that is above the threshold voltage the H-Bridge outputs automatically resume normal operation according to the established condition of the input pins.

#### LOGIC INPUT CONTROL (IN1A, IN1B, IN2A, AND IN2B)

These logic input pins control each H-Bridge output. For example, IN1A logic HIGH = OUT1A HIGH; likewise, IN1B logic HIGH = OUT1B HIGH. If both A and B inputs are HIGH, then both A and B outputs are Z (refer to [Table 5, Truth Table, page 7](#)).

#### INPUT ENABLE CONTROL (PSAVE)

The PSAVE input controls the functioning of the power output stages (the H-Bridges). When it is set logic LOW, the output stages are enabled and the H-Bridges function normally. When it is set logic HIGH, the output stages are

disabled and all the outputs are opened (high impedance). In this mode, the built-in low voltage detection circuit is disabled.

#### H-BRIDGE OUTPUT (OUT1A, OUT1B, OUT2A, AND OUT2B)

These pins are the outputs of the power MOSFET H-Bridges. OUT1 is from H-Bridge Channel 1, and OUT2 from H-Bridge Channel 2. These pins will typically connect to an external load (step motor or brush DC motors).

#### MOTOR DRIVER POWER SUPPLY (VM1 AND VM2)

VM1 and VM2 carries the main supply voltage and current into the power sections (the H-Bridges) of the IC. Both of these pins are connected internally but they must be connected together on the printed circuit board with as short as possible traces. The input range is 2.7 V to 5.5 V.

#### POWER GROUND (PGND1 AND PGND2)

These two are the power ground pins that connect to the power ground of the H-Bridges. The power grounds are for higher current handling capability from loads and they must be connected together on the PCB.

#### LOGIC GROUND (LGND)

LGND is the logic ground pin and its current handling level is lower than the PGND.



## TYPICAL APPLICATIONS

Figure 6 shows a typical application for the 17C724.

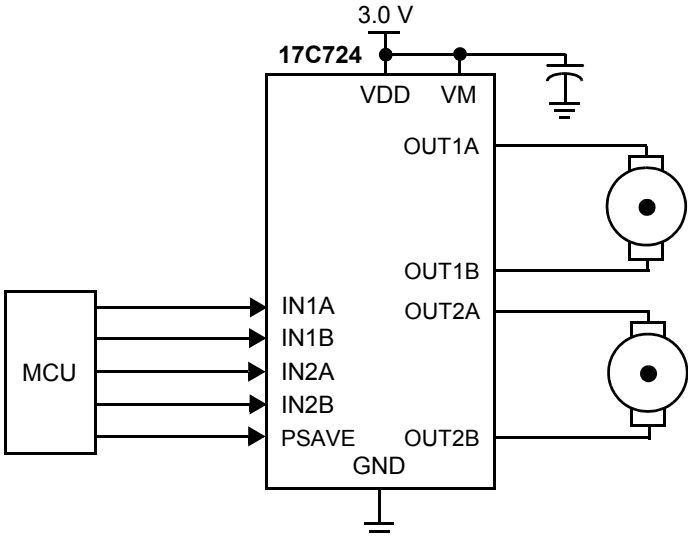


Figure 6. 17C724 Typical Application Diagram

### CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a zener or capacitor at the supply pin (VM) (see Figure 7).

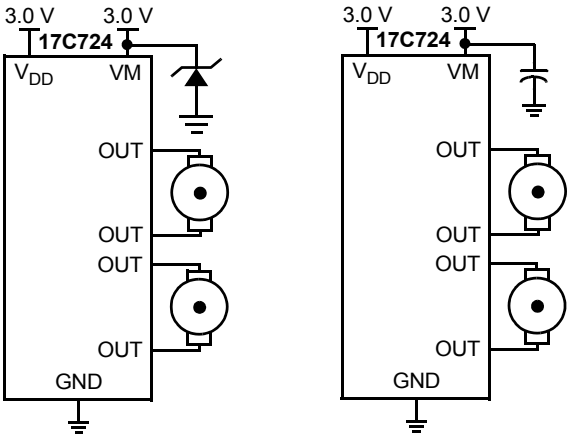


Figure 7. CEMF Snubbing Techniques

### PCB LAYOUT

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground pins to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distance.

### APPLICATION NOTES

Although VM1 and VM2 are connected internally, they must be connected externally to attain sufficient power distribution.

Take precautions to guard against electrostatic discharge when handling the device, especially when mounting and demounting the device to a PCB.

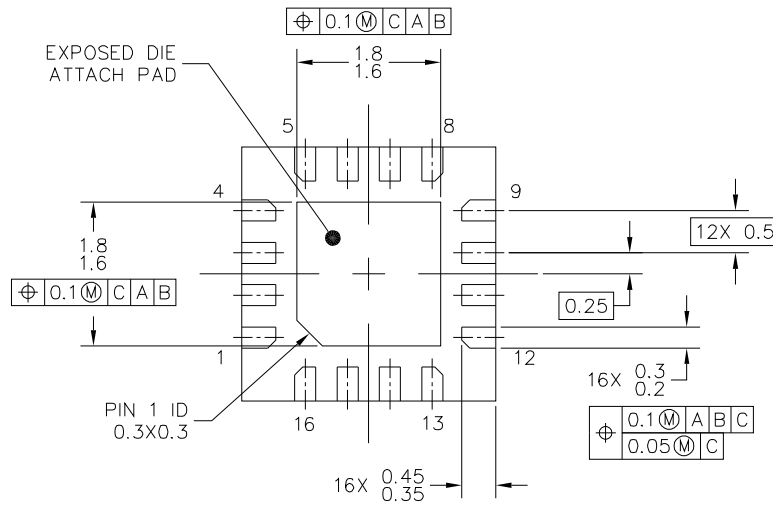
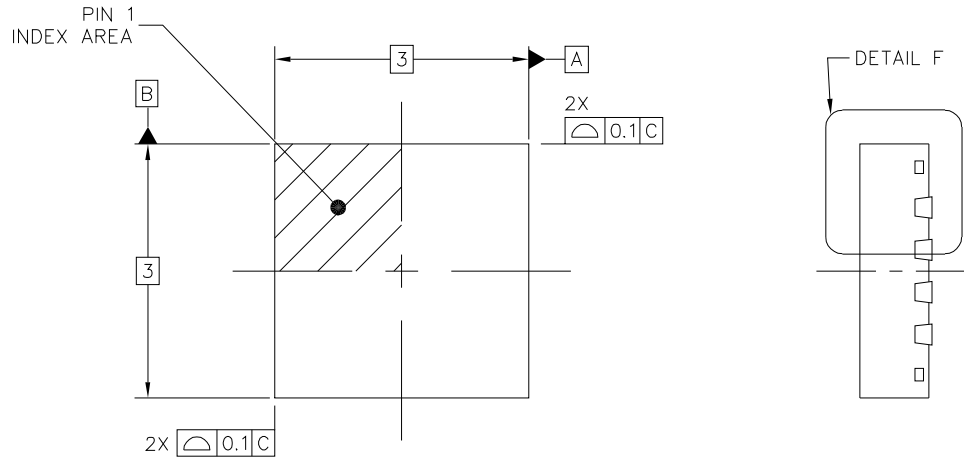
## PACKAGING

### PACKAGE DIMENSIONS

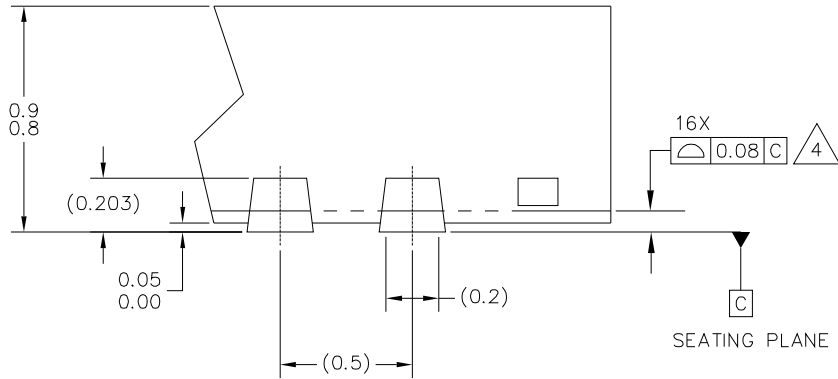
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to [www.freescale.com](http://www.freescale.com) and perform a keyword search for the drawing's document number.

**Table 6.**

| Package    | Suffix | Package Outline Drawing Number |
|------------|--------|--------------------------------|
| 16-PIN QFN | EP     | 98ASA00741D                    |




|  |                          |                            |
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DETAIL F  
VIEW ROTATED 90°CW

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4.  COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

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|  |                    | STANDARD: NON-JEDEC        |        |
|  |                    | 16 MAY 2014                |        |

## REVISION HISTORY

| REVISION | DATE    | DESCRIPTION OF CHANGES  |
|----------|---------|---|
| 2.0      | 2005    | <ul style="list-style-type: none"> <li>• Initial Release</li> </ul>   |
|          | 12/2013 | <ul style="list-style-type: none"> <li>• No technical changes</li> <li>• Revised back page</li> <li>• Updated document properties</li> </ul>  |
| 3.0      | 9/2014  | <ul style="list-style-type: none"> <li>• Updated the case outline as per Cu wire PCN 16443.</li> <li>• The change of package case outline is required to support the new assembly process.</li> </ul> |



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