NXP Semiconductors
User's Guide

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Freedom Board for Kinetis K28F (FRDM-K28F)

1. Introduction

The Freedom development platform is a set of software and hardware tools for evaluation and development. It is ideal for rapid prototyping of MCU-based applications. The Freedom K28 board (FRDM-K28F) is a simple yet sophisticated design featuring the Kinetis K series MCU built upon the ARM® Cortex®-M4 core which features a Floating-Point Unit (FPU).

FRDM-K28F can be used to evaluate the K27 and K28 Kinetis K series MCUs. The FRDM-K28F board features the MK28FN2M0VMI15 MCU which features a maximum operating frequency of 150 MHz, 2 MB flash, 1 MB RAM, high-speed and full-speed USB controller with available crystal-less operation, SDRAM controller, secure digital host controller, QuadSPI controller, and analog and digital peripherals. The FRDM-K28F hardware is form-factor compatible with the Arduino™ R3 pin layout, providing a broad range of expansion board options. The on-board interface includes a 6-axis digital accelerometer and magnetometer, RGB LED, FlexIO socket, SD card interface, mobile SDRAM memory, and external serial flash memory.

Contents

FRDM-K28F features OpenSDA v2.2, the open-source hardware embedded serial and debug adapter running an open-source bootloader. This circuit offers several options for serial communication, flash programming, and run-control debugging. OpenSDA v2.2 is an mbed™ HDK-compatible debug interface pre-loaded with the open-source DAP link interface firmware for rapid prototyping and product development with focus on the connected Internet of Things (IoT) devices.

2. FRDM-K28F hardware overview

The features of the FRDM-K28F board are:

- Kinetis MK28FN2M0VMI15 MCU (ARM Cortex-M4 at150 MHz, 1 MB SRAM, 2 MB flash, HS and FS USB, 169 MAPBGA package).
- Kinetis K20 MCU (K20DX128VFM5) based OpenSDA circuit.
- Dual-role high-speed and full-speed USB interface with the micro-B USB connector via the high-speed switch.
- One 256 Mbit (32 MB) on-board QuadSPI memory at 1.8 V.
- One 128 Mbit (16 MB) on-board mobile SDRAM memory at 3.3 V.
- Multiple independent voltage domains: VDD_CORE, VDD, VBAT, and VDDIO_E.
- FlexIO socket which enables you to connect an optional TFT Proto 5” CAPACITIVE from MikroElektronika (5” display board with capacitive touch).
- Easy access to the MCU input/output through Arduino R3-compatible I/O connectors to connect external add-on boards.
- Flexible power supply option—OpenSDA v2.2 USB, Kinetis K28 USB, or an external source.
- FXOS8700CQ—6-axis sensor with accelerometer and magnetometer.
- RGB LED.
- Two mechanical push-buttons for user input and one for the reset.
- Programmable OpenSDA v2.2 debug circuit supporting the DAP-Link interface software which provides:
  - Mass-Storage Device (MSD) flash programming interface.
  - CMSIS-DAP debug interface over a driverless USB HID connection providing run-control debugging and compatibility with the IDE tools.
  - Virtual serial port interface.
  - Open-source CMSIS-DAP software project.

Figure 1 shows the block diagram of the FRDM-K28F board. The primary components and their placement on the hardware assembly are shown in Figure 2.

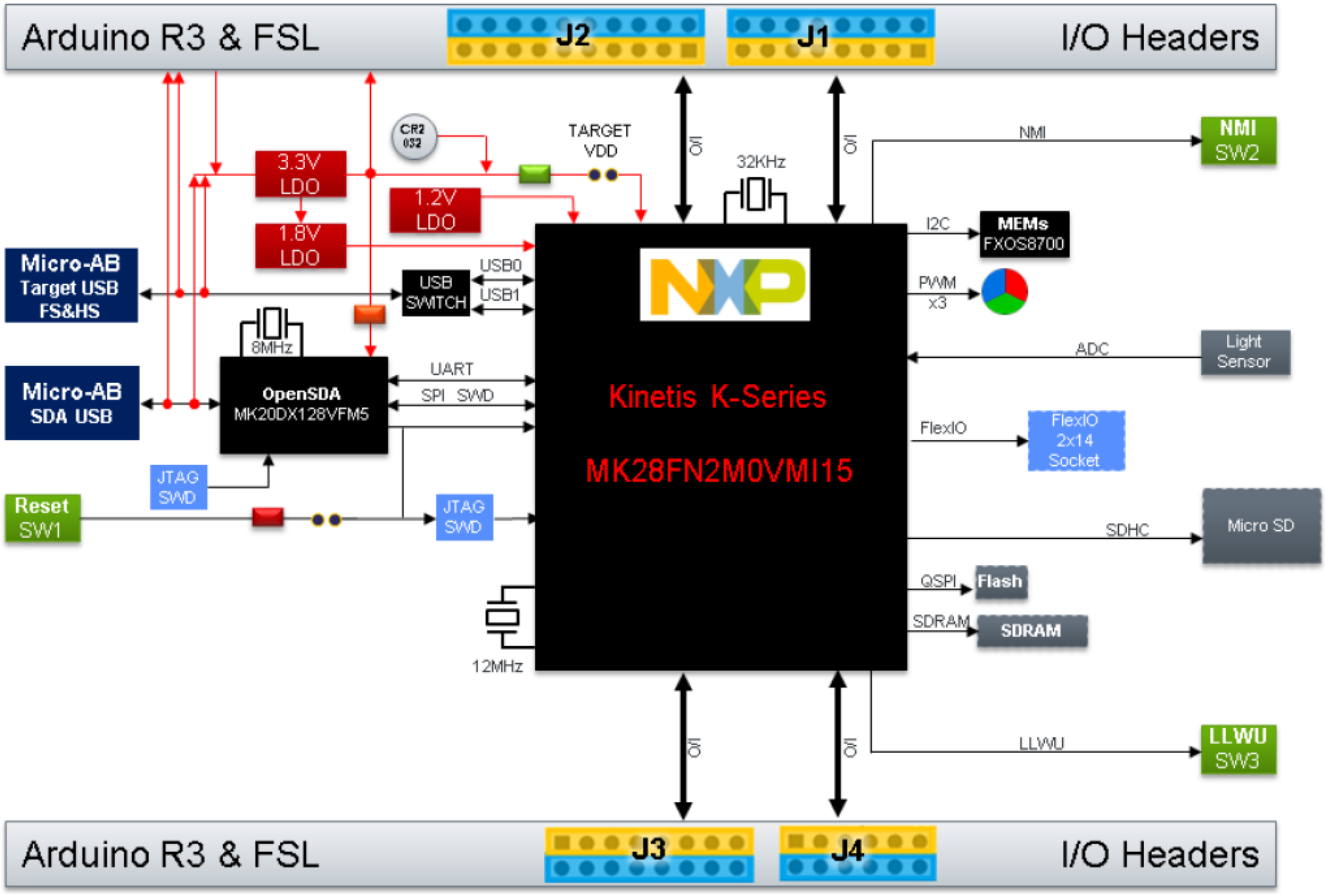

Figure 1. FRDM-K28F block diagram

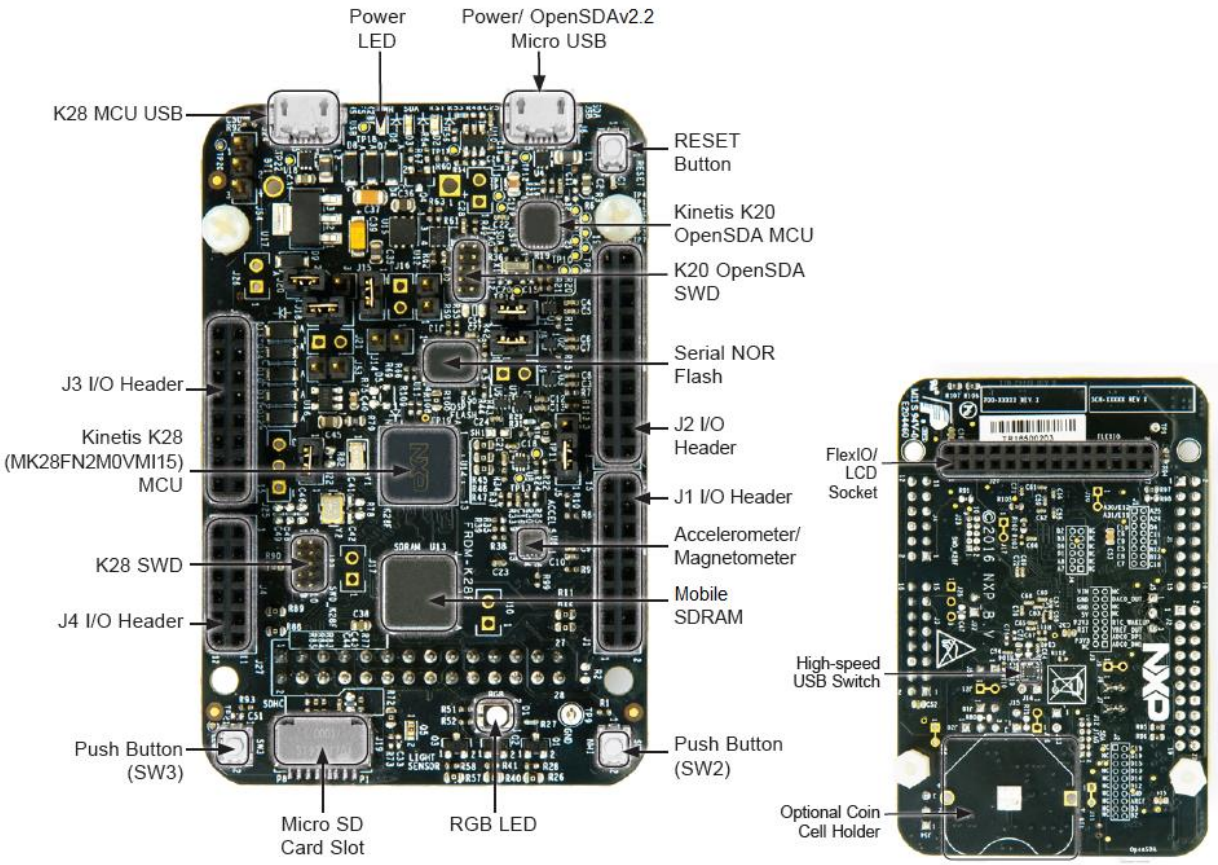

Figure 2. FRDM-K28F primary component placement

3. FRDM-K28F hardware description

3.1. Power supply

There are multiple power supply options on the FRDM-K28F board. It can be powered from either of the USB connectors, the VIN pin on the I/O header, or an off-board 1.71 V–3.6 V supply from the 3.3 V pin on the I/O header. The USB and VIN supplies are regulated on-board using a 3.3 V linear regulator to produce the main power supply and a 1.8 V linear regulator to produce the VDDIO_E power supply. A direct voltage supply to the K28F MCU is also available via J18, J15, and J22. The following table provides the operational details and requirements for the power supplies.

Table 1. FRDM-K28F power requirements

Supply source	Valid range	OpenSDA v2.2 operational	Regulated on-board
OpenSDA v2.2 USB	5 V	Yes	Yes
K28F USB	5 V	No	Yes
P5-9V_VIN pin	5 V–9 V	No	Yes
3.3 V VDD header (J18)	1.71 V–3.6 V	No	No
1.8 V VDDIO_E header (J15)	1.71 V–3.6 V	No	No
1.2 V VDD_CORE header (J22)	1.17 V–1.32 V (RUN mode) 1.33 V–1.47 V (HSRUN mode)	No	No

NOTE

The OpenSDA v2.2 circuit is only operational when a USB cable is connected and supplies power to the OpenSDA v2.2 USB. However, a protection circuitry is provided to enable multiple sources to be powered at once. By default, the FRDM-K28F VDD_CORE = 1.2 V is operating in the RUN mode. To operate in the HSRUN mode, supply 1.33 V–1.47 V externally.

CAUTION

When 3.3 V is supplied directly through the Freedom platform compatibility header J3, enable the protection diode D9 by opening the J26 shorting header.

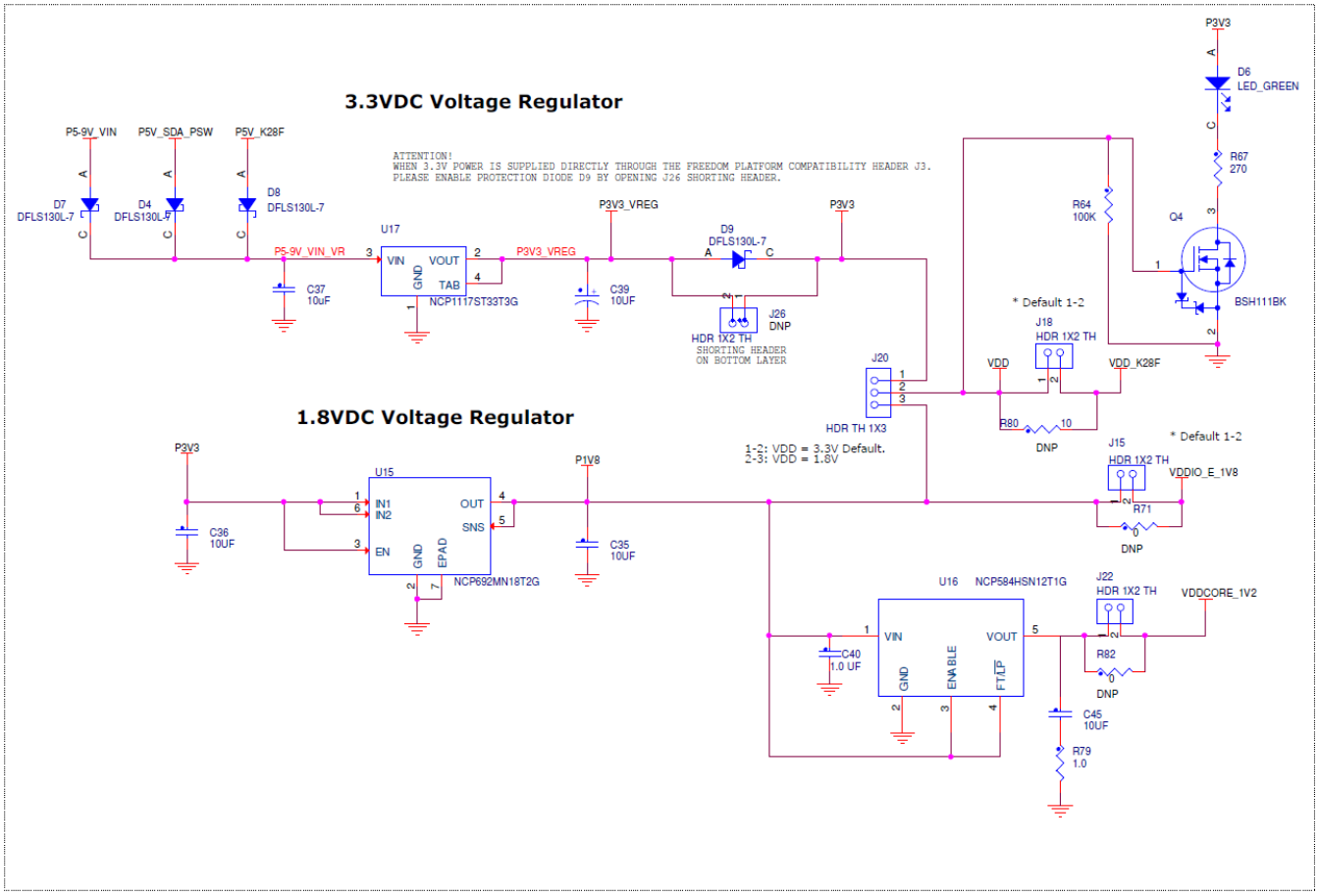

Figure 3. Power supply schematic

Table 2. FRDM-K28F power supplies

Power supply name	Description	Notes
P5-9V_VIN	Power supply from the VIN pin of the I/O headers (J3 pin 16). Sources the main 3.3 V voltage regulator and the optional 5 V regulator at J25. A Schottky diode provides the back-drive protection.	—
P3V3_VREG	Regulated 3.3 V supply. Sources power to the P3V3 supply rail. A back-drive protection Schottky diode (D9) is provided to enable an external 2.7 V–3.3 V supply connection at the J3 header P3V3 pins.	Open J26 (shorted on the bottom of the board) if the J3 header P3V3 pins are used to supply an alternate voltage from the on-board 3.3 V supply.
VDD_K28F	K28F MCU voltage supply. Select the 3.3 V or 1.8 V regulator options at header J20, or the 2.7 V–3.3 V P3V3 inputs on the J3 header. Header J18 provides a convenient means for energy consumption measurements.	The IS42SM16800H-6BLI SDRAM is a 3.3 V component. Open J10 (shorted on the bottom of the board) if the VDD_K28F node is less than 2.7 V.
VDDIO_E_1V8	K28F VDDIO_E MCU voltage supply. Header J15 provides a convenient means for energy consumption measurements.	The MT25QU256ABA1EW7-0SIT QSPI flash is a 1.8 V component. Open J16 (shorted on the bottom of the board) if the VDDIO_E_1V8 node is ever raised above 1.8 V.
VDDCORE_1V2	K28F VDD_CORE MCU voltage supply. Header J22 provides a convenient means for energy consumption measurements.	—
P3V3	Main supply for the 3 V MCU VDD and peripheral functions. Supplies nominal 3 V at the J3 header P3V3 nodes. Sourced from the P3V3_VREG or P3V3 inputs on the J3 I/O header.	When the J3 P3V3 inputs are used, the voltage must be in the 2.7 V–3.3V range. See the VDD_K28F note.
P1V8	Power supply for the 1.8 V MCU VDDIO_E pins and the QSPI peripheral. P1V8 can be selected as the MCU VDD source at header J20.	See the VDD_K28F note if P1V8 is selected as the source at header J20.
VDD	Supply the voltage for the MCU and many board functions. Select the 3.3 V or 1.8 V regulator options on header J20, or the P3V3 inputs on the J3 header.	When the J3 P3V3 inputs are used, the voltage must be in the 2.7 V–3.3 V range. See the VDD_K28F note.
P3V3_SDA	OpenSDA v2.2 circuit 3.3 V supply generated on the K20DX from the USB cable VBUS signal.	—
P5V	Nominal 5 V supplied to the I/O headers (J3 pin 10).	—

3.2. Serial and Debug Adapter version 2 (OpenSDA v2.2)

OpenSDA v2.2 is a serial and debug adapter circuit which includes open-source hardware design, open-source bootloader, and debug interface software. It bridges the serial and debug communications between the USB host and the embedded target processor, as shown in the following figure. The hardware circuit is based on the Kinetis K20 family MCU with 128 KB of embedded flash and an integrated USB controller. OpenSDA v2.2 is pre-loaded with the CMSIS-DAP bootloader (an open-source MSD bootloader), and the DAP-Link interface firmware which provides the MSD flash

programming interface, virtual serial port interface, and CMSIS-DAP debug protocol interface. For more information about the OpenSDA v2.2 software, see mbed.org and github.com/mbedmicro/CMSIS-DAP.

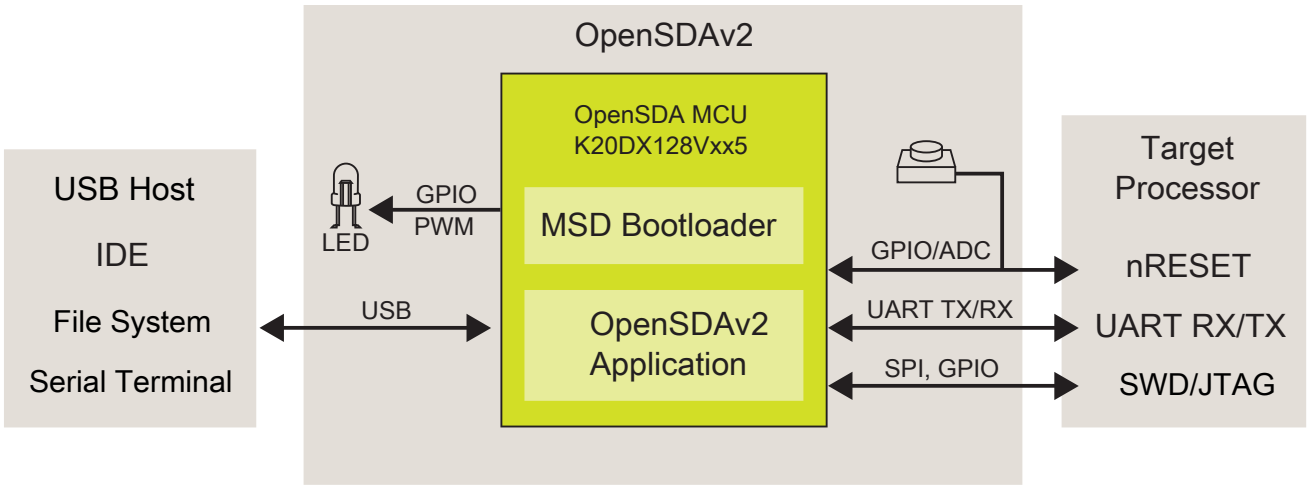

Figure 4. OpenSDA high-level block diagram

OpenSDA v2.2 is managed by the Kinetis K20 MCU built upon the ARM Cortex-M4 core. The OpenSDA v2.2 circuit includes a status LED (D3) and a push-button (SW1). The push-button asserts the reset signal to the K28F target MCU. It can be also used to place the OpenSDA v2.2 circuit into the bootloader mode. The SPI and GPIO signals provide an interface to either the SWD debug port or the K20. Additionally, signal connections are available to implement the UART serial channel. The OpenSDA v2.2 circuit receives power when the USB connector J6 is plugged into a USB host.

3.2.1. Debug interface

Signals with the UART and GPIO capability are used to connect directly to the SWD of the K28F. These signals are also brought out to the standard 10-pin (0.05”) Cortex debug connector (J23). It is possible to isolate the K28F MCU from the OpenSDA v2.2 circuit and use J23 to connect to an off-board MCU. To do this, cut the trace on the bottom side of the PCB that connects the J17 pin 2 to the J23 pin 4. This disconnects the SWD_CLK pin from the K28F so that it does not interfere with the communication to an off-board MCU connected to J17.

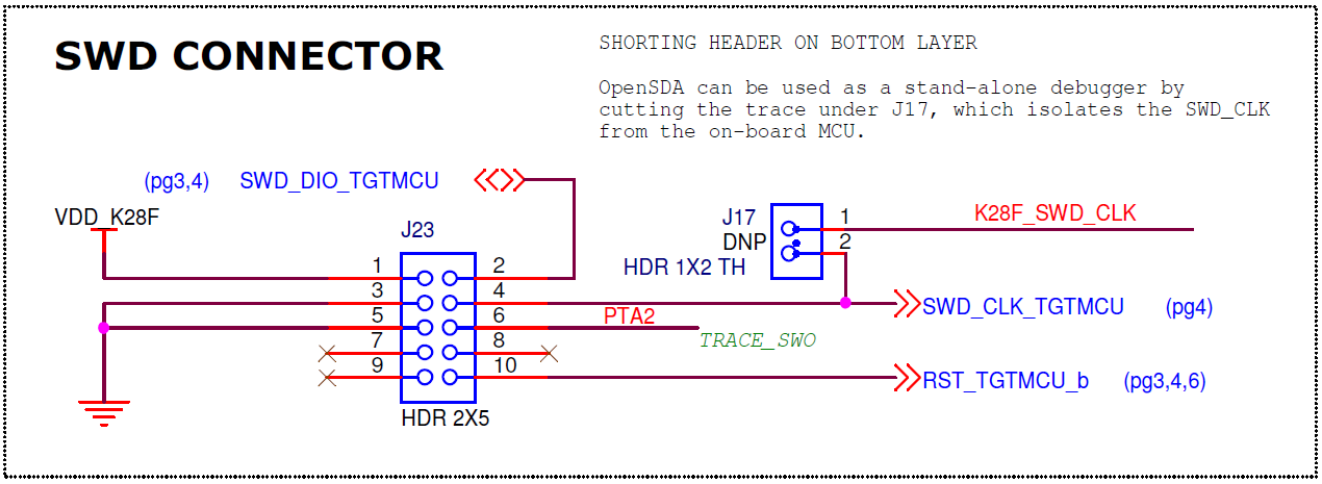

Figure 5. SWD debug connector

The J23 header is populated by default. A mating cable (such as the Samtec FFSD IDC cable) can then be used to connect the OpenSDA v2.2 of the FRDM-K28F to an off-board SWD connector.

3.2.2. Virtual serial port

A serial port connection is available between the OpenSDA v2.2 MCU and pins PTC24 and PTC25 of the K28 MCU.

4. MCU

FRDM-K28F features the MK28FN2M0VMI15 MCU. This 150 MHz MCU is a part of the Kinetis K2x family and it is implemented in the 169 MAPBGA and 210 WLCSP (K28 only) packages. The FRDM-K28F board also supports the K27 and K28 MCUs. The following table describes some of the features of the MK28FN2M0VMI15 MCU that is populated on this board.

Table 3. MK28FN2M0VMI15 MCU features

Feature	Description
Performance	• Up to 150 MHz ARM Cortex-M4-based core with DSP instructions and a single precision floating-point unit.
Memory and memory expansion	• 2 MB program flash memory and 1 MB RAM. • Dual QuadSPI with XIP. • FlexBus external bus interface and SDRAM controller.
Analog modules	• One 16-bit SAR ADC, two 6-bit DACs, and one 12-bit DAC. • Two analog comparators (CMP) containing a 6-bit DAC and a programmable reference input. • Voltage reference: 1.2 V.
Communication interfaces	• USB high-speed device/host. • USB full-/low-speed on-the-go controller with the device charge detect capability. • Secure Digital Host Controller (SDHC). • FlexIO. • Two I^2S modules, four SPI modules (SPI3 supports more than 40 Mbit/s), four I^2C modules, and five LPUART modules.
Security	• Hardware random-number generator. • Supports DES, AES, and SHA accelerator (CAU). • Cyclic Redundancy Check (CRC). • Multiple levels of embedded flash security.
Timers	• One 4-channel 32-bit periodic interrupt timer. • Two 16-bit low-power timer PWM modules. • Two 8-channel motor-control/general-purpose/PWM timers. • Two 2-channel quadrature decoder/general-purpose timers. • Real-time clock with an independent 3.3 V power domain. • Programmable delay block.
Human machine interface	• Up to 120 general-purpose inputs/outputs.
Operating Characteristics	• Main VDD voltage and flash write voltage range: 1.71 V–3.6 V. • Temperature range (ambient): -40–105°C. • Independent VDD_CORE: 1.17 V-1.47 V. • Independent VDDIO for PORTE (QuadSPI): 1.71 V–3.6 V. • Independent VBAT (RTC): 1.71 V–3.6 V.

5. Clocking

CAUTION

The resonator is not recommended when the HS USB is used.

The K28F MCU starts up from an internal Digitally-Controlled Oscillator (DCO). Software can enable the main external oscillator (EXTAL0/XTAL0) if desired. The external oscillator/resonator can range from 32.768 kHz up to 32 MHz. The default external source for the MCG oscillator inputs (EXTAL) is the 12 MHz crystal, which is configured to operate in the low-power mode, so the feedback resistor (R78) is not needed. The 12 MHz reference clock is suitable for both the audio codec and the HS USB features.

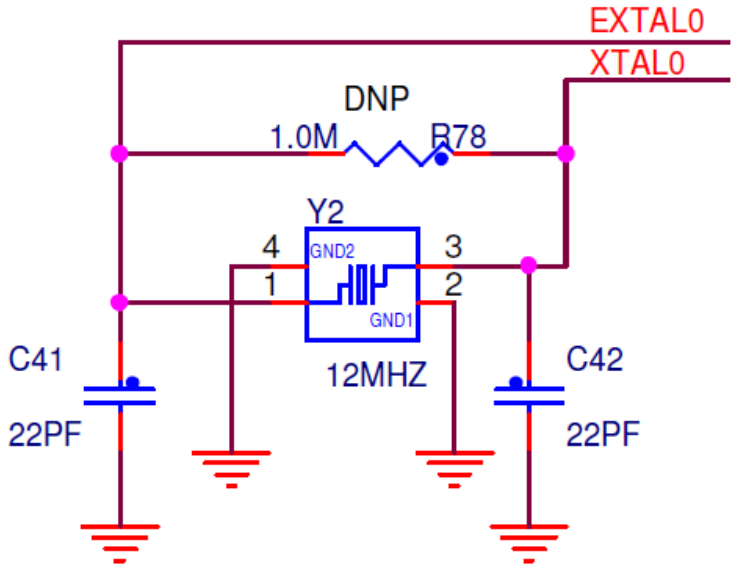

Figure 6. 12 MHz crystal clock source for MCU

By default, the 32.768 KHz crystal is connected to the K28F MCU's RTC oscillator inputs.

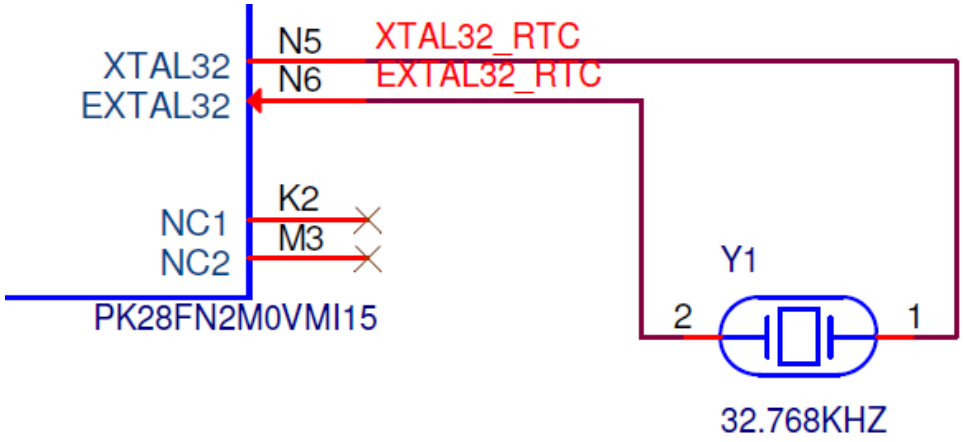

Figure 7. 32.768 kHz crystal for RTC

6. Universal Serial Bus (USB)

The MK28FN2M0VMI15 MCU features the HS USB with the host/device capability and a full-speed/low-speed USB module with the on-the-go/host/device capability and a built-in transceiver. The FRDM-K28F board routes the USB D+ and D signals from the MK28FN2M0VMI15 MCU to the high-speed analog switch (NXP NX3DV42), selecting between the HS and FS USB signals to the on-board micro USB connector (J24).

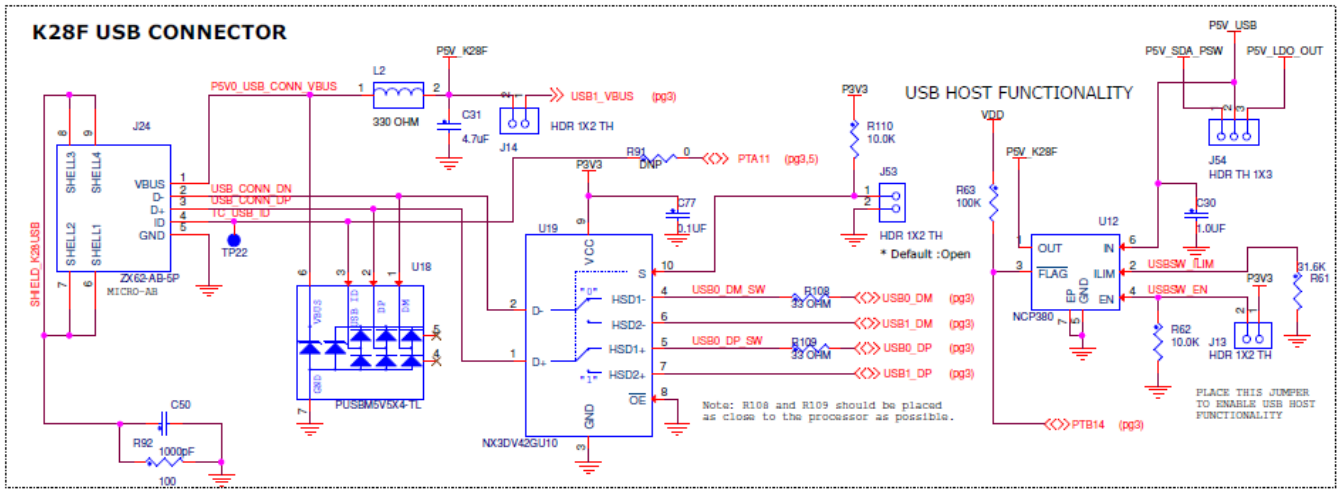

Figure 8. K28F USB port

When the FRDM-K28F board operates in the USB host mode, J13 must be shunted to supply 5 V to VBUS (J24 pin 1). The 5 V source can be the OpenSDA v2.2 USB port (J6) or the optional 5 V regulator populated at J25 and supplied by P5-9V_VIN at pin 16 of the J3 connector.

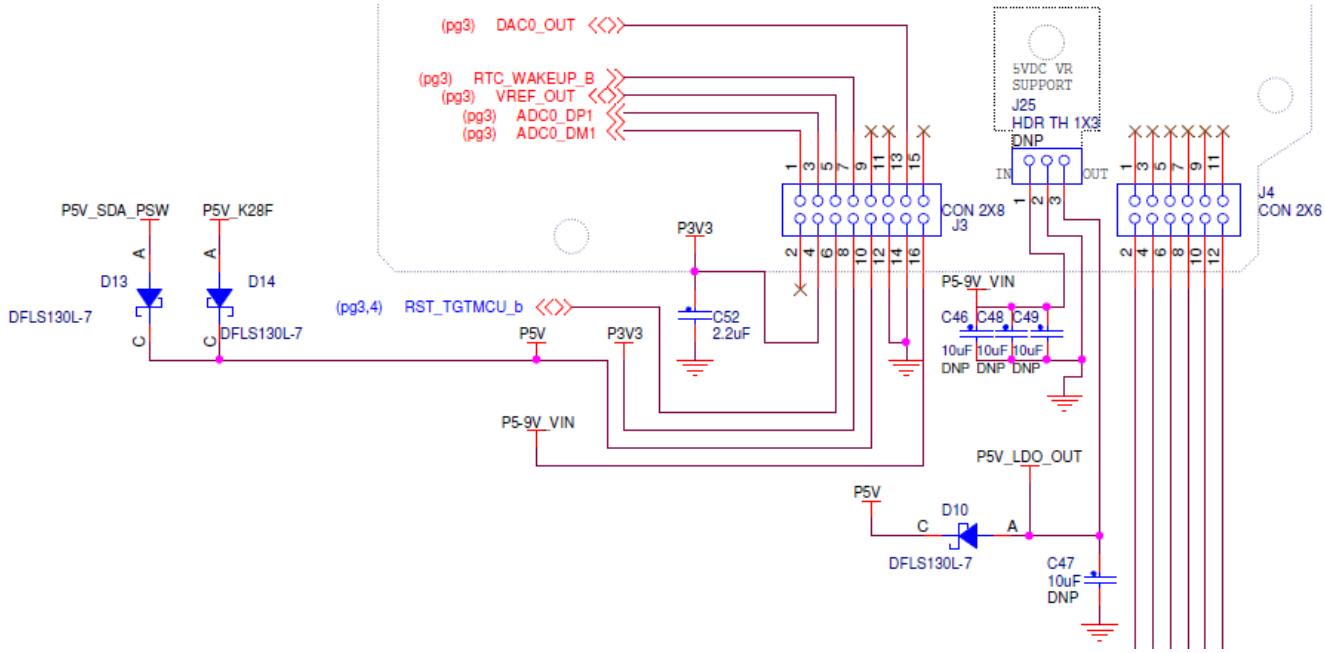

Figure 9. K28F USB port power inputs for host mode

7. VBAT

The Real-Time Clock (RTC) module is powered on its own domain. FRDM-K28F provides a battery holder for a coin cell battery that can be used as the VBAT supply. The holder supports common 20 mm diameter 3 V lithium coin cell batteries (for example, 2032 and 2025).

If a coin cell battery is used, add a small amount of solder to the coin cell ground pad before adding the battery holder.

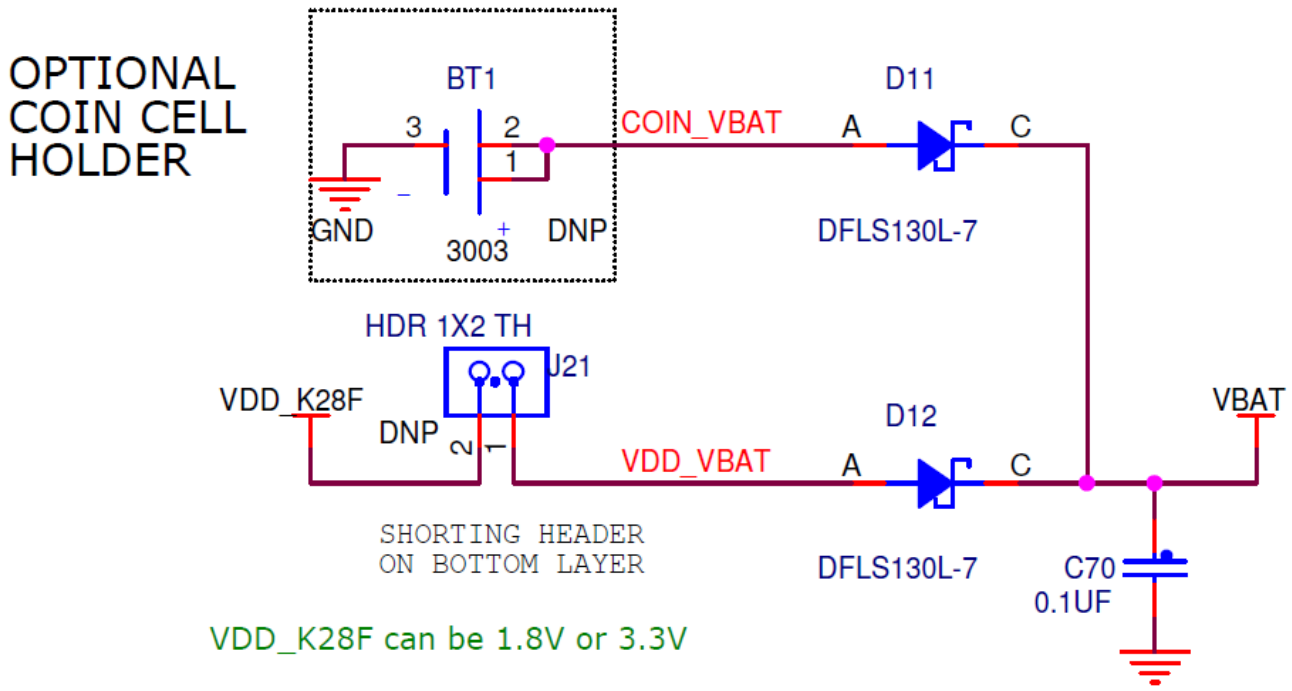

Figure 10. Coin cell

8. Accelerometer and magnetometer

The FXOS8700CQ low-power, six-axis sensor with the accelerometer and magnetometer is interfaced through the I^2C bus and two GPIO signals, as shown in the following table. By default, the I^2C address is 0x1C (pull-up on SA1 and pull-down on SA0).

Table 4. Accelerometer and magnetometer signal connection

FXOS8700Q	K28F connection
SCL	PTC29/ **I2C3_SCL**
SDA	PTC28/ **I2C3_SDA**
INT1	**PTC26**
RST	**PTC27**

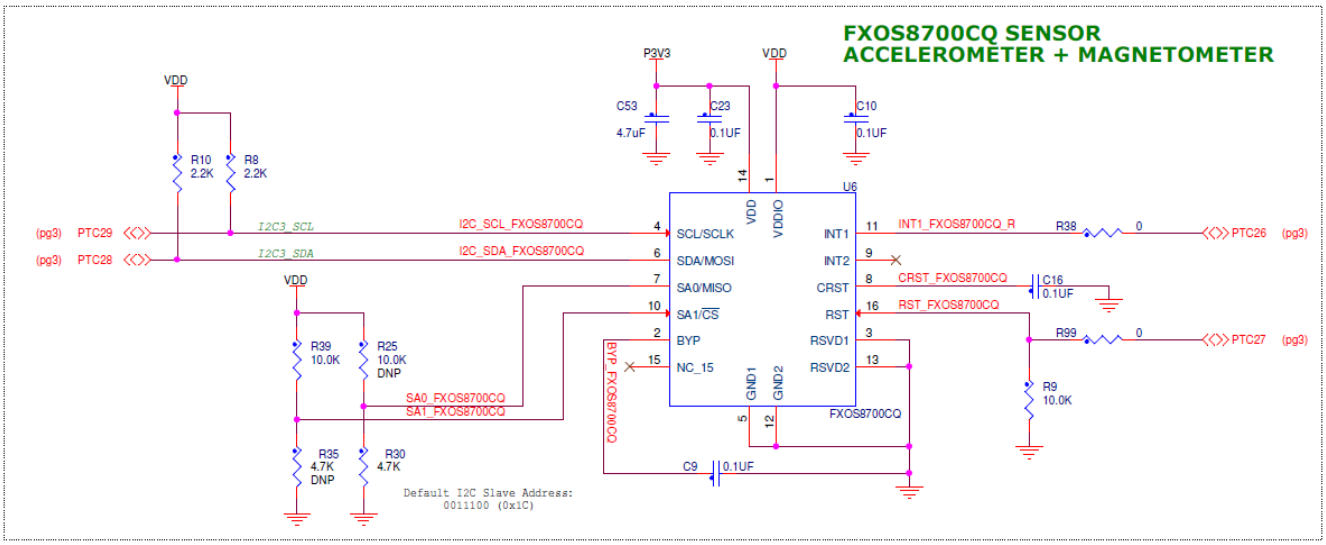

Figure 11. Accelerometer and magnetometer

9. RGB LED

The RGB LED is connected through the GPIO pins. The signal connections are shown in the following table. Note that the RGB LED operates in the range of the MCU supply voltage.

Table 5. LED signal connection

RGB LED	K28F connection
RED	**PTE6**
GREEN	**PTE7**
BLUE	**PTE8**

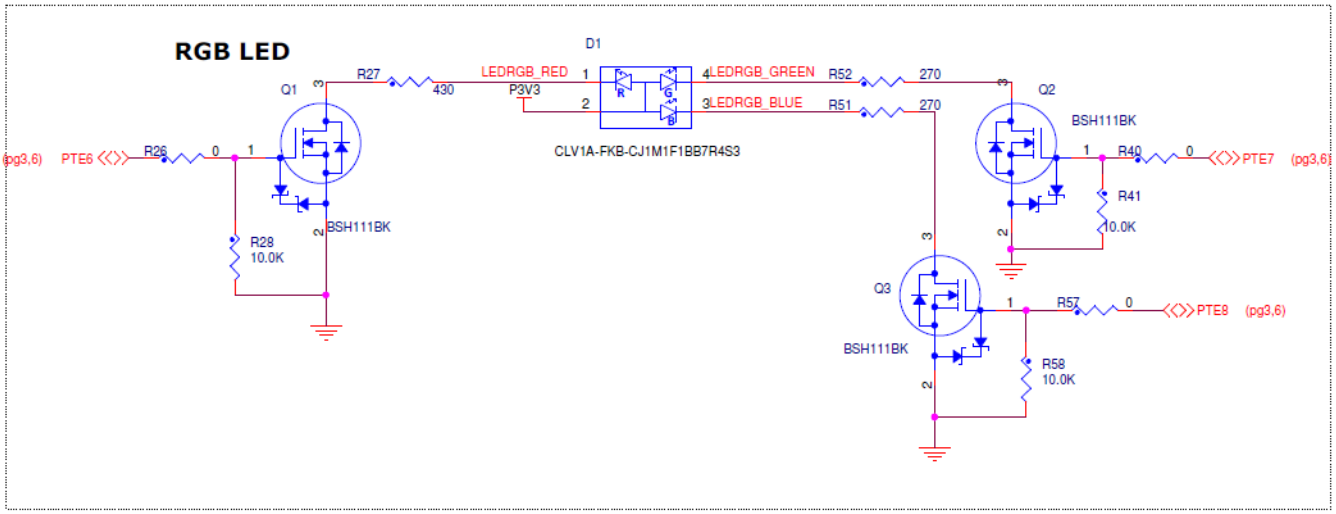

Figure 12. Accelerometer and magnetometer

10. Serial port

The primary serial port interface signals are PTC24 LPUART0_RX_TGTMCU and PTC25 LPUART0_TX_TGTMCU. These signals are connected to the OpenSDA v2.2 circuit.

11. QuadSPI memory

FRDM-K28F includes a single QuadSPI memory with Execute in Place (XiP). The on-board QuadSPI uses the Micron MT25QU256ABA, which is 256 Mb (32 MB) in size. The QuadSPI interface offers up to 100 MHz performance for the Single Data Rate (SDR). Header J16 provides a convenient means for energy consumption measurement. The QuadSPI is also supported by the internal Kinetis BootROM.

12. Mobile SDRAM memory

FRDM-K28F also includes a single 128 Mb mobile SDRAM memory that operates at 3.3 V. The on-board mobile SDRAM uses the ISSI IS42SM16800H-6BLI. The SDRAM controller interface offers performance of up to 75 MHz. Header J10 provides a convenient means for energy consumption measurement.

13. Secure Digital (SD) card

A micro SD card slot is available on the FRDM-K28F board. It is connected to the SD Host Controller (SDHC) signals of the MCU. This slot accepts micro SD memory cards. The SD card detect pin is an open switch that shorts with VDD when a card is inserted. Table 6 shows the SDHC signal connection details.

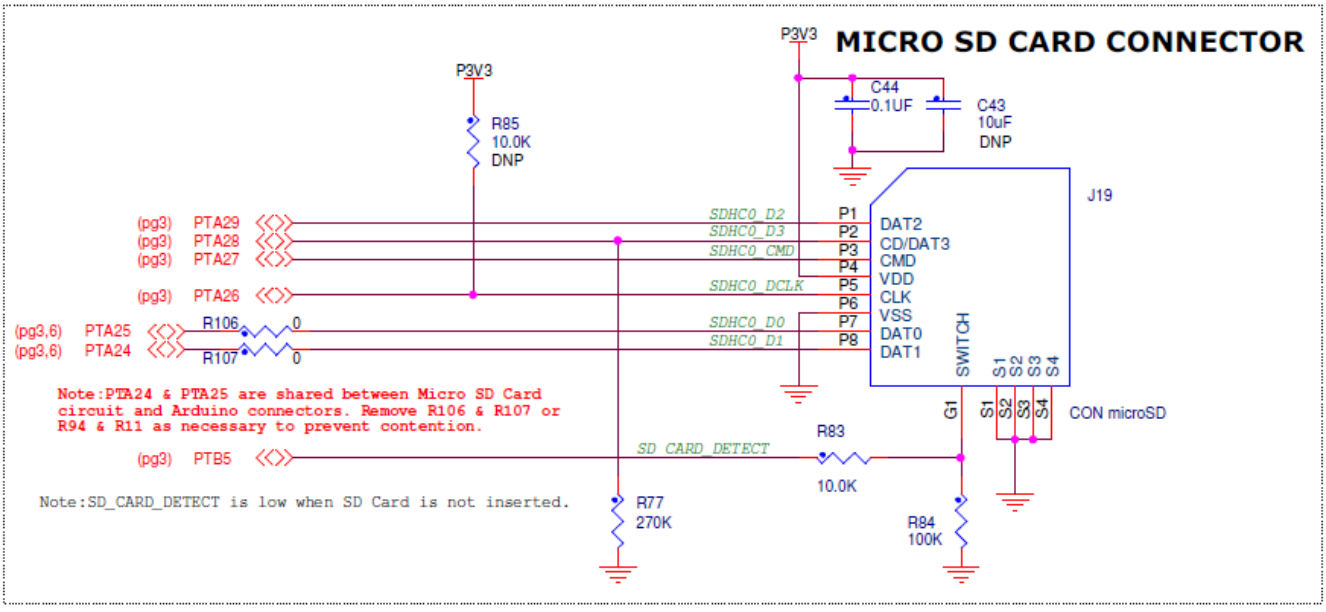

Figure 13. Micro SD card connector

Table 6. Micro SD card signal connections

Pin	Function	FRDM-K28F connection
P1	DAT2	PTE5/SPI1_PCS2/UART3_RX/SDHC0_D2/FTM3_CH0
P2	CD/DAT3	PTE4/LLWU_P2/SPI1_PCS0/UART3_TX/SDHC0_D3/TRACE_D0
P3	CMD	PTE3/ADC1_SE7A/SPI1_SIN/UART1_RTS/SDHC0_CMD/TRACE_D1/SPI1_SOUT
P4	VDD	3.3 V board supply (P3V3)
P5	CLK	PTE2/LLWU_P1/ADC1_SE6A/SPI1_SCK/UART1_CTS/SDHC0_DCLK/TRACE_D2
P6	VSS	Ground
P7	DAT0	PTE1/LLWU_P0/ADC1_SE5A/SPI1_SOUT/UART1_RX/SDHC0_D0/TRACE_D3/I2C1_SL/SPI1_SIN
P8	DAT1	PTE0/ADC1_SE4A/SPI1_PCS1/UART1_TX/SDHC0_D1/TRACE_CLKOUT/I2C1_SDA/RTC_CLKOUT
G1	SWITCH	PTB5
S1-S4	S1-S4	Shield ground

14. FlexIO socket

There is a 28-pin header with 20 FlexIO signals connected on the bottom of the board. It is compatible with the MikroElektronica TFT Proto 5” capacitive touch display.

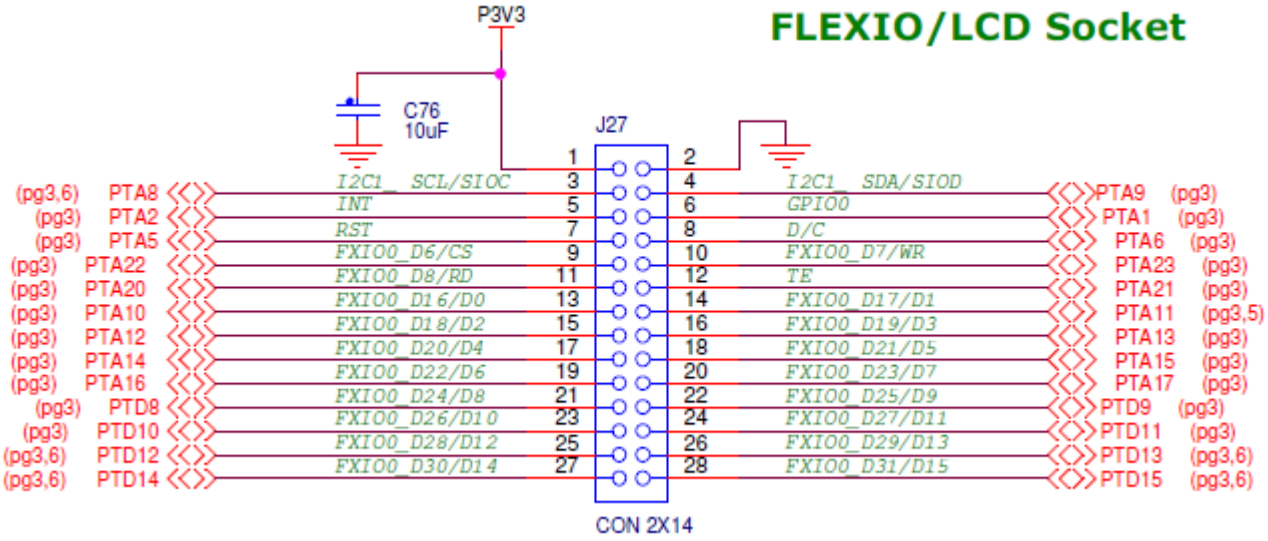

Figure 14. Accelerometer and magnetometer

15. Reset

The reset push-button (SW1) is connected to the reset signal on the K28F MCU through a level-shifter (U8) and to the OpenSDA v2.2 circuit. The reset button can be used to force an external reset on the target MCU. The reset button can also be used to force the OpenSDA v2.2 circuit into the bootloader mode. When not using the OpenSDA v2.2 circuit to supply power, the reset signal can be connected directly to the target MCU. For more details, see Section 3.2, "Serial and Debug Adapter version 2 (OpenSDA v2.2)".

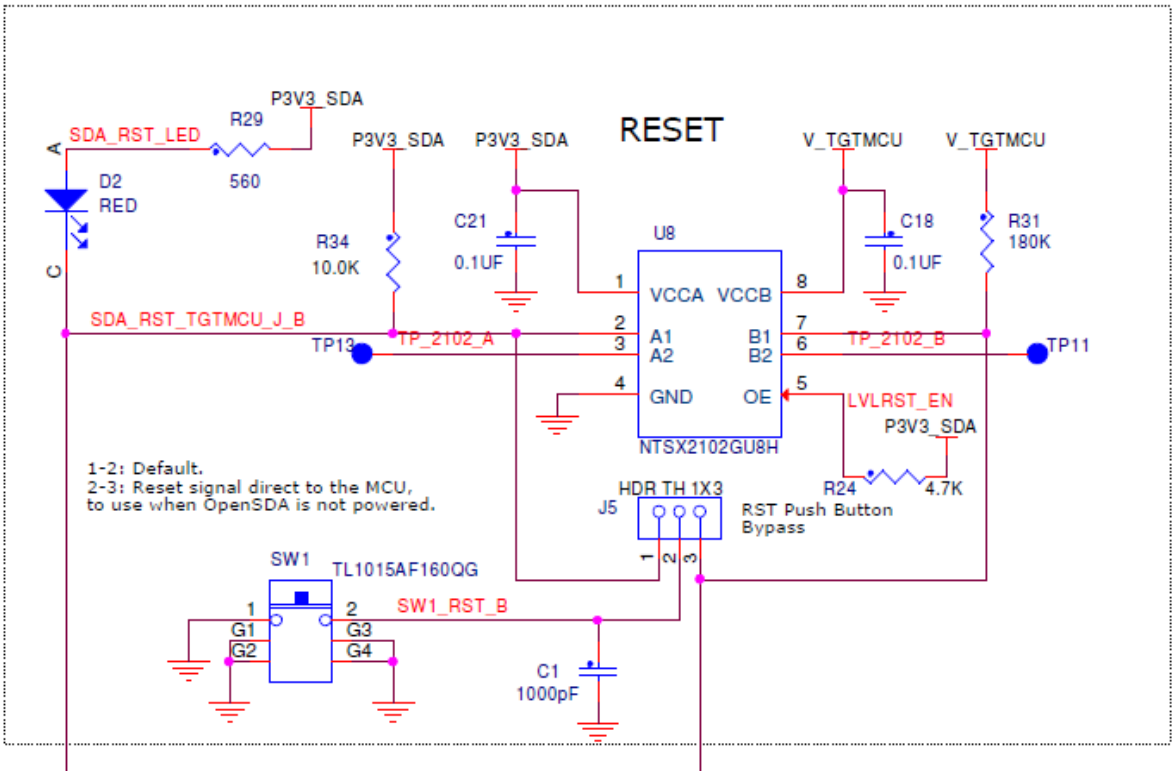

Figure 15. Reset circuit

16. Push-button switches

Two push-buttons (SW2 and SW3) are available on the FRDM-K28F board. SW2 is connected to PTA4 and SW3 is connected to PTD0. Besides the general-purpose input/output functions, SW2 can be also used as a Low-Leakage Wakeup (LLWU) source.

Table 7. Push-button switch connections

Switch	K28F connection
SW2	**PTA4/NMI_B**
SW3	**PTD0/LLWU_P12**

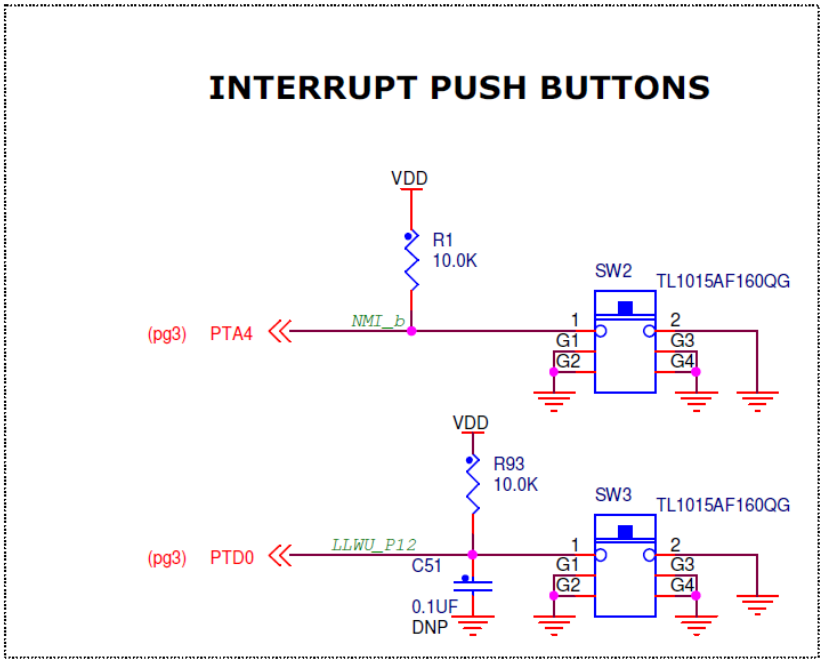

Figure 16. Push-button switches

17. Visible light sensor

FRDM-K28F has an on-board visible light sensor (Q5) which is connected to ADC0_SE16.

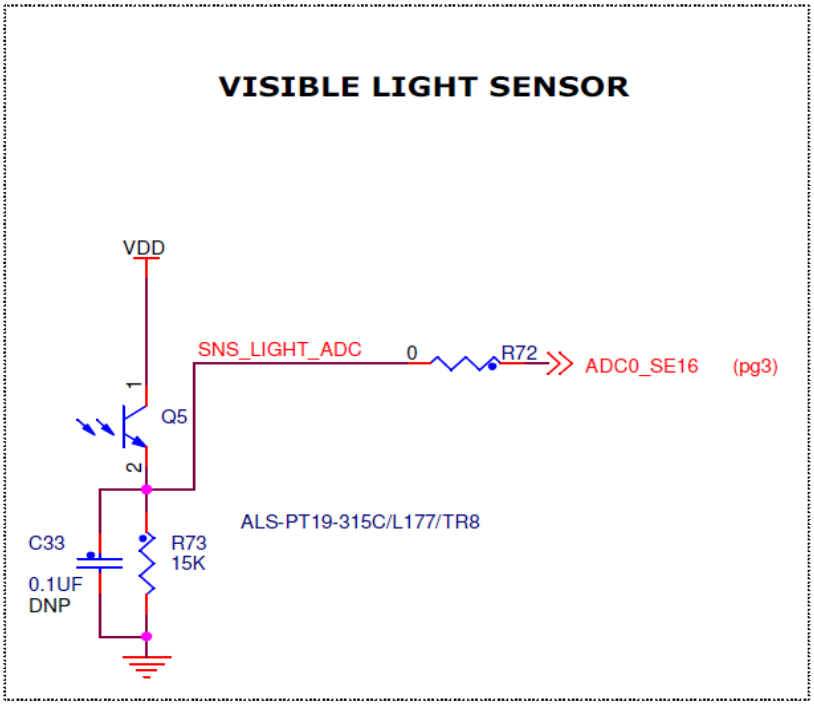

Figure 17. Visible light sensor

18. Debug

The debug interface on the MK28FN2M0VMI15 MCU is the Serial Wire Debug (SWD) port with the trace output capability. There are two debug interfaces on FRDM-K28F: the on-board OpenSDA v2.2 circuit (J12) and the K28F direct SWD connection via the 10-pin header (J23). To use an external debugger (such as J-Link on J23), you may need to disconnect the OpenSDA v2.2 SWD circuit from the K28F by removing jumpers J7 and J8.

19. Input/output connectors

The MK28FN2M0VMI15 MCU is packaged in the 169 MAPBGA package. Some pins are used in the on-board circuitry, but some are connected directly to one of the four I/O headers (J1, J2, J3, and J4).

The pins on the K28F MCU are named after their General-Purpose Input/Output (GPIO) port pin function. For example, the first pin on port A is referred to as PTA1. The name assigned to the I/O connector pin corresponds to the GPIO pin of the K28F MCU.

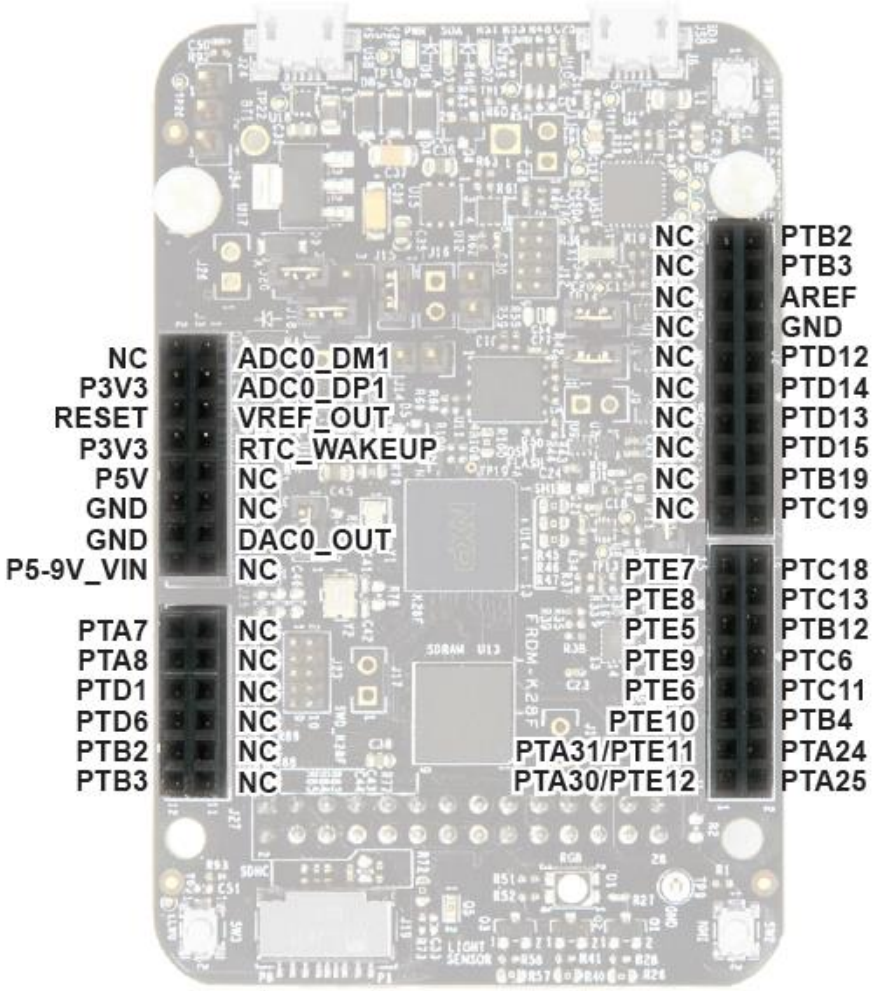

Figure 18. FRDM-K28F I/O header pinout

20. Arduino compatibility

The I/O headers on the FRDM-K28F board are compatible with the peripheral boards (known as shields) that connect to the Arduino and Arduino-compatible MCU boards. The outer rows of pins (the even numbered pins) on the headers share the mechanical spacing and placement with the I/O headers on the Arduino Revision 3 (R3) standard.

21. Jumper table

The following table shows the available jumper options on the FRDM-K28F board. The default jumper settings are shown in **bold**.

Table 8. FRDM-K28F jumper table

Jumper	Option	Setting	Description
J5	Reset push-button bypass	**1-2**	Reset button connected to OpenSDA
J7	SWD_CLK	**1-2**	OpenSDA SWD_CLK isolation jumper
J8	SWD_DIO	**1-2**	OpenSDA SWD_DIO isolation jumper
J9	OpenSDA reset	DNP*	OpenSDA reset isolation jumper (*shorted on board)
J10	SDRAM supply	DNP*	Measurement point for the SDRAM supply (*shorted on board)
J11	OpenSDA power	DNP*	Isolate the power to the OpenSDA circuit (*shorted on board)
J13	USB host	1-2	**OFF host power disable** ON host power enable
J14	VBUS	1-2	USB1_VBUS isolation
J15	VDDIO_E supply	**1-2**	Measurement point for the K28 VDDIO_E (1.8 V) power domain
J16	QuadSPI supply	DNP*	Measurement point for the QuadSPI supply (*shorted on board)
J17	SWD_CLK	DNP*	Isolate the SWD_CLK from the SWD header (*shorted on board)
J18	VDD supply	**1-2**	Measurement point for the K28 VDD (1.8 V or 3.3 V) power domain
J20	VDD selection	**1-2** 2-3	**VDD domain is 3.3 V** VDD domain is 1.8 V
J21	VBAT supply	DNP*	Isolate the VDD_VBAT (*shorted on board)
J22	VDD CORE supply	**1-2**	Measurement point for the K28 VDD (1.2 V) power domain
J25	5V DC support	DNP	Optional 5 V regulator
J26	P3V3_VREG protection	DNP*	Enable the diode protection when using an external supply on P3V3 (*shorted on board)
J53	USB HS and FS selection	1-2	**OFF USB HS** ON USB FS
J54	USB host power selection	1-2 2-3	From the SDA circuit From the 5 V regulator

22. References

These references are available at www.nxp.com/FRDM-K28F:

- *FRDM-K28F Quick Start Guide*
- *FRDM-K28F Schematic*
- *FRDM-K28F Design Package*

The following reference is available at www.nxp.com/kboot:

- Kinetis Flashloader

23. Revision history

Table 9. Revision history

Revision number	Date	Substantive changes
0	04/2017	Initial release

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