



QorIQ T1024/14 and T1023/13 Communications Processors

Next-generation system-on-chip (SoC) for low-cost enterprise and service provider edge and network control applications

TARGET APPLICATIONS

- ▶ Wired and wireless branch routers
- ▶ WLAN 11ac enterprise access points
- ▶ Service provider WLAN access points
- ▶ Unified threat management gateways
- ▶ Multifunction printers
- ▶ Router and switch controllers
- ▶ Line card controllers
- ▶ Industrial automation and computing, single board computers
- ▶ Aerospace and defense ruggedized network equipment

The QorIQ T1024/23 communications processors combine single or dual 64-bit cores, built on Power Architecture® technology, with high-performance Data Path Acceleration Architecture (DPAA) and network peripheral bus interfaces required for networking and telecommunications applications. The T1024 and T1014 processors come in a full featured 23 x 23 mm package which provides scalable pin compatibility with the quad-core T1042 processor, and even the eight-core T2081 processor, for price and power scaling with a single system design. The T1023 and T1013 processors are interfaces and power-optimized SoCs designed to deliver impressive

single- or dual-core performance for cost and power sensitive networking systems. Both versions offer an excellent software compatible 64-bit and I/O upgrade path for the popular QorIQ P10XX family of 32-bit communications processors.

SOFTWARE AND TOOL SUPPORT

With the help of our partner network, we deliver a wide range of tools, run-time software, reference solutions and services to accelerate your designs.

- ▶ CodeWarrior Development Studio for Power Architecture technology
- ▶ Proprietary QorIQ Linux® SDK
- ▶ VortiQa application software
 - VortiQa application identification software (AIS)
 - Enterprise software for networking
 - VortiQa open network switch software
 - VortiQa open network director software

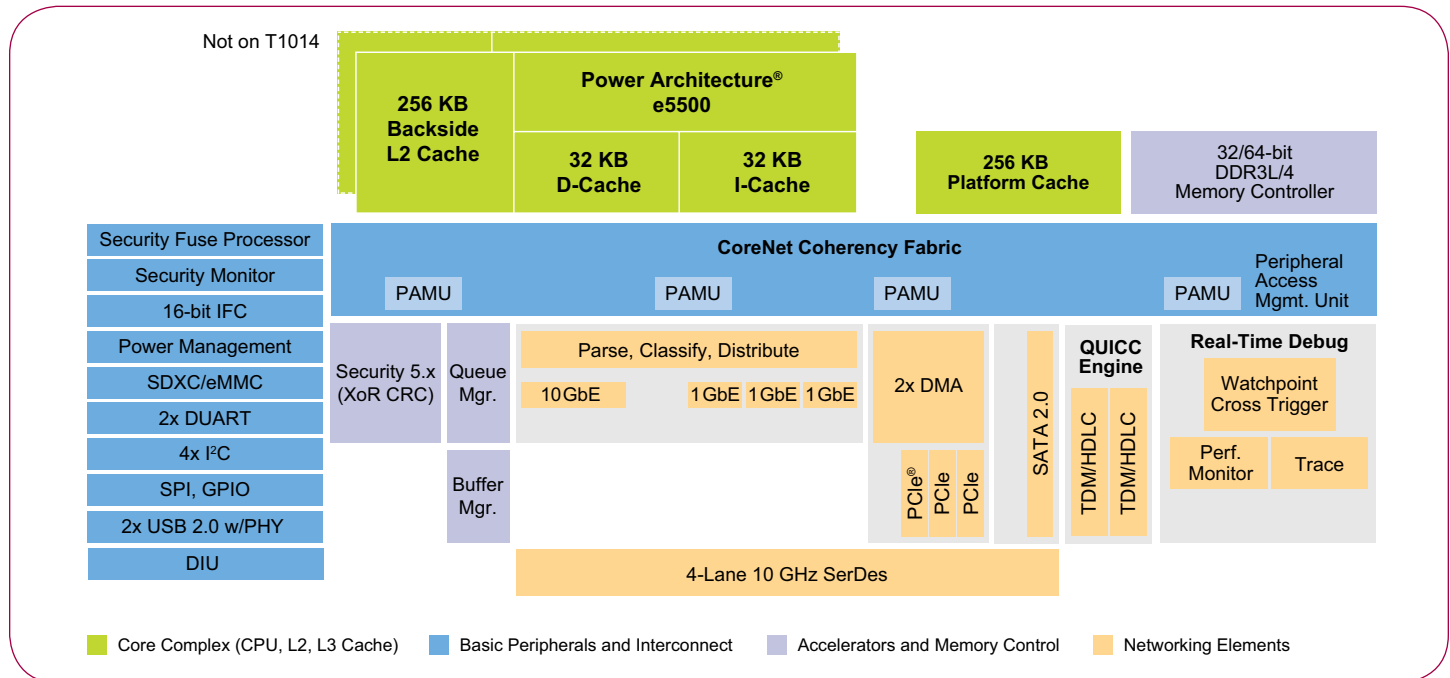


- Professional services and support
 - Commercial services
 - Linux SDK support package
 - Reference design software (RDS) support package
- Third-party software and tools
 - Enea, Green Hills, Mentor Graphics and Wind River

QorIQ P1020 AND T102X PROCESSORS COMPARISON TABLE

| | P1020/11 | T1023/13 | T1024/14 | T1042 |
|---|--------------|---------------|---------------|---------------|
| Core | 1-2 x e500v2 | 1-2 x e5500 | 1-2 x e5500 | 4 x e5500 |
| Power ISA | 32-bit | 64-bit | 64-bit | 64-bit |
| Max MHz | 800 | 1400 | 1400 | 1400 |
| L2 Backside Cache | – | 256 KB | 256 KB | 256 KB |
| Platform Cache | 256 KB | 256 KB | 256 KB | 256 KB |
| DDR Type and Speed | 2/3 1333MTs | 3L/4 1600MTs | 3L/4 1600MTs | 3L/4 1600MTs |
| DDR Speed | to 1333MTs | to 1600MTs | to 1600MTs | to 1600MTs |
| DDR Width | 36 b | 36 b | 36 b/72 b | 36 b/72 b |
| SerDes | 4 | 4 | 4 | 8 |
| PCIe Lanes | 2 x 1 v1 | 3 x 1 v2 | 3 x 1 v2 | 4 x 1 v2 |
| GbE | up to 3 | up to 4 | up to 4 | up to 5 |
| 10GbE I/O | – | 1 | 1 | – |
| MACSEC | – | All ports | All ports | All ports |
| Hardware Offload | – | DPAA | DPAA | DPAA |
| Crypto | SEC 3.x | SEC 5.x | SEC 5.x | SEC 5.x |
| Pattern Matching | – | – | – | Yes |
| QUICC Engine TDM/HDLC, ISDN, Industrial | Yes | – | Yes | Yes |
| SATA | – | 2.0 x 1 | 2.0 x 1 | 2.0 x 2 |
| USB | 2.0 x 2 | 2.0 x 2 w Phy | 2.0 x 2 w Phy | 2.0 x 2 w Phy |
| Lossless Deep Sleep | – | – | Yes | Yes |
| Auto Response | – | – | Yes | Yes |
| Display Interface | – | – | Yes | Yes |
| Single Clock Source | – | Yes | Yes | Yes |
| Package | 31 x 31 PBGA | 19 x 19 FCBGA | 23 x 23 FCBGA | 23 x 23 FCBGA |
| Pin Compatible | No | No | Yes | Yes |

QORIQ T1014 AND T1024 COMMUNICATIONS PROCESSOR



QorIQ T1023/24 PROCESSORS FEATURES LIST

| | |
|--|---|
| Two or four e5500 single-threaded cores built on Power Architecture technology | <ul style="list-style-type: none"> Up to 1.4 GHz with 64-bit ISA support Low latency, per core, core clocked 256 KB dedicated cache Hybrid 32-bit mode to support legacy software and transition to a 64-bit architecture Nap, wait and doze low-power modes |
| CoreNet platform cache | <ul style="list-style-type: none"> 256 KB shared platform cache for stashing support |
| Hierarchical interconnect fabric | <ul style="list-style-type: none"> CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet endpoints QMAN fabric supporting packet-level queue management and quality of service |
| 64-bit DDR3L/4 SDRAM memory controller with ECC support | <ul style="list-style-type: none"> 32-bit or 64-bit low power DDR up to 1600 MT/s |
| DPAA incorporating acceleration for the following functions | <ul style="list-style-type: none"> Full L2/3 tunneling and en/decrypt offload support for functions such as WLAN CAPWAP/DTLS secure wired links Packet parsing, classification and distribution Queue management for scheduling, packet sequencing and congestion management Hardware buffer management for buffer allocation and de-allocation Cryptography acceleration (SEC 5.x) |
| SerDes | <ul style="list-style-type: none"> Four lanes at up to 10 Gbit/s Supports SGMII, 2.5 Gbit SGMII, QSGMII, XFI, 10G BASE-KR, PCI Express® and SATA |
| Ethernet interfaces | <ul style="list-style-type: none"> Up to 4 x Ethernet MACs |
| QUICC Engine module | <ul style="list-style-type: none"> Integrated support for legacy WAN protocols TDM, HDLC, UART, ISDN and industrial protocols |
| High-speed peripheral interfaces | <ul style="list-style-type: none"> Three PCI Express 2.0 controller |
| Additional peripheral interfaces | <ul style="list-style-type: none"> One serial ATA (SATA 2.0) controller Two high-speed USB 2.0 controllers with integrated PHYs Enhanced secure digital host controller (SD/MMC/eMMC) Enhanced serial peripheral interface Two I²C controllers Four UARTS Integrated flash controller supporting NAND and NOR flash memory |
| DMA | <ul style="list-style-type: none"> Dual four channel |
| Support for hardware virtualization and partitioning enforcement | <ul style="list-style-type: none"> Extra privileged level for hypervisor support |
| QorIQ trust architecture | <ul style="list-style-type: none"> Secure boot, secure debug, tamper detection, volatile key storage |
| Single source clocking | <ul style="list-style-type: none"> For BOM cost reduction |