

# DATA SHEET

**74F132**

Quad 2-input NAND Schmitt trigger

Product specification

1991 Jun 26

IC15 Data Handbook

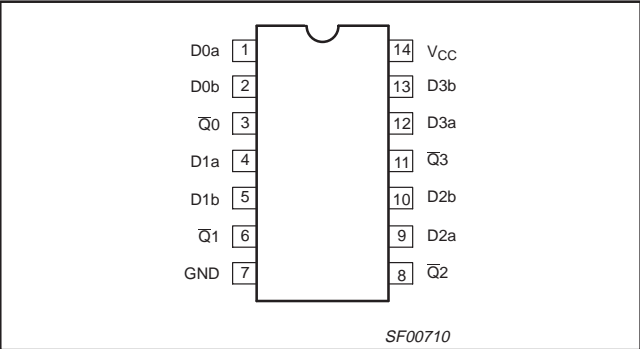
Quad 2-input NAND Schmitt trigger

74F132

DESCRIPTION

The 74F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates. Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than  $V_{T+MAX}$ , the gate will respond in the transition of the other input as shown in Waveform 1.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F132	6.3ns	13mA

ORDERING INFORMATION

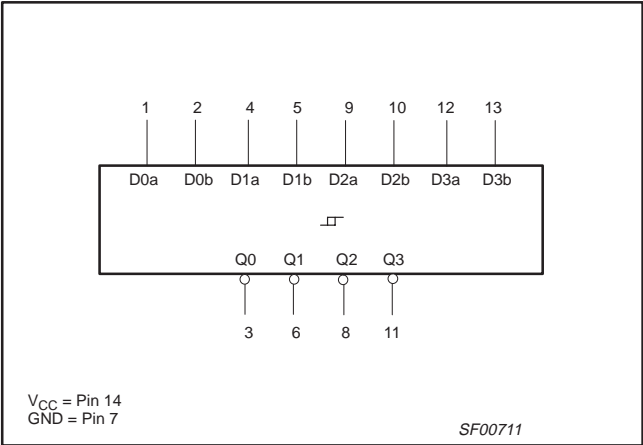
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$	PKG DWG #
14-pin plastic DIP	N74F132N	SOT27-1
14-pin plastic SO	N74F132D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

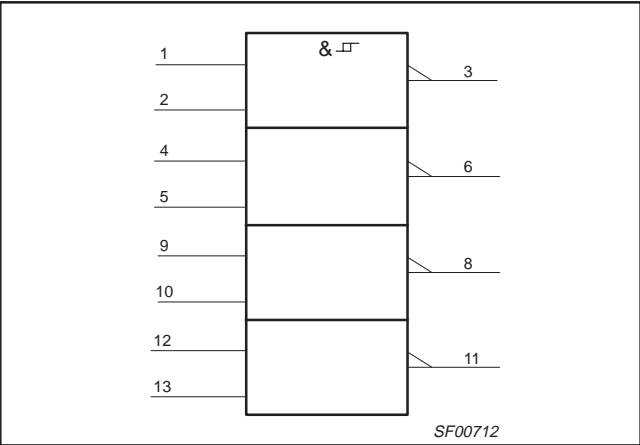
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}n$	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



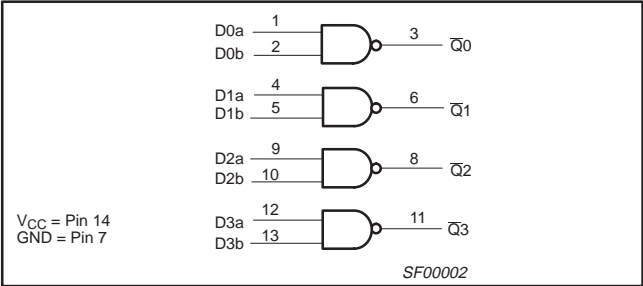
IEC/IEEE SYMBOL



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	Qn
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:  
H = High voltage level  
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	−0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	−0.5 to +7.0	V
I <sub>IN</sub>	Input current	−30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	−0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
I <sub>IK</sub>	Input clamp current			−18	mA
I <sub>OH</sub>	High-level output current			−1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C

## Quad 2-input NAND Schmitt trigger

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**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>		LIMITS			UNIT
					MIN	TYP <sup>2</sup>	MAX	
V <sub>T+</sub>	Positive-going threshold		V <sub>CC</sub> = 5.0V		1.5	1.7	2.0	V
V <sub>T–</sub>	Negative-going threshold–		V <sub>CC</sub> = 5.0V		0.7	0.9	1.1	V
ΔV <sub>T</sub>	Hysteresis (V <sub>T+</sub> – V <sub>T–</sub> )		V <sub>CC</sub> = 5.0V		0.4	0.8		V
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = MIN, V <sub>I</sub> =V <sub>T–MAX</sub> , I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.5			V
				±5%V <sub>CC</sub>	2.7	3.4		
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>I</sub> =V <sub>T+MAX</sub> , I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.30	0.50	V
				±5%V <sub>CC</sub>		0.30	0.50	
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			–0.73	–1.2	V
I <sub>T+</sub>	Input current at positive-going threshold		V <sub>CC</sub> = 5.0V, V <sub>I</sub> =V <sub>T+</sub>			0		μA
I <sub>T–</sub>	Input current at negative-going threshold		V <sub>CC</sub> = 5.0V, V <sub>I</sub> =V <sub>T–</sub>			–350		μA
I <sub>I</sub>	Input current at maximum input voltage		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				100	μA
I <sub>IH</sub>	High-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA
I <sub>IL</sub>	Low-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V				–0.6	mA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>		V <sub>CC</sub> = MAX		–60		–150	mA
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX	V <sub>I</sub> N= GND		8.5	12.0	mA
		I <sub>CCL</sub>		V <sub>I</sub> N = 4.5V		13.0	19.5	

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5V, T_{amb} = 25^\circ C$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

Quad 2-input NAND Schmitt trigger

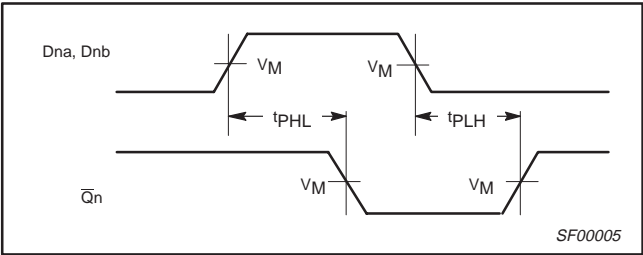
74F132

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5.0V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5.0V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay D <sub>na</sub> , D <sub>nb</sub> to Q̄ <sub>n</sub>	Waveform 1	3.5 4.5	5.5 6.0	7.0 8.5	3.0 4.5	8.5 9.0	ns

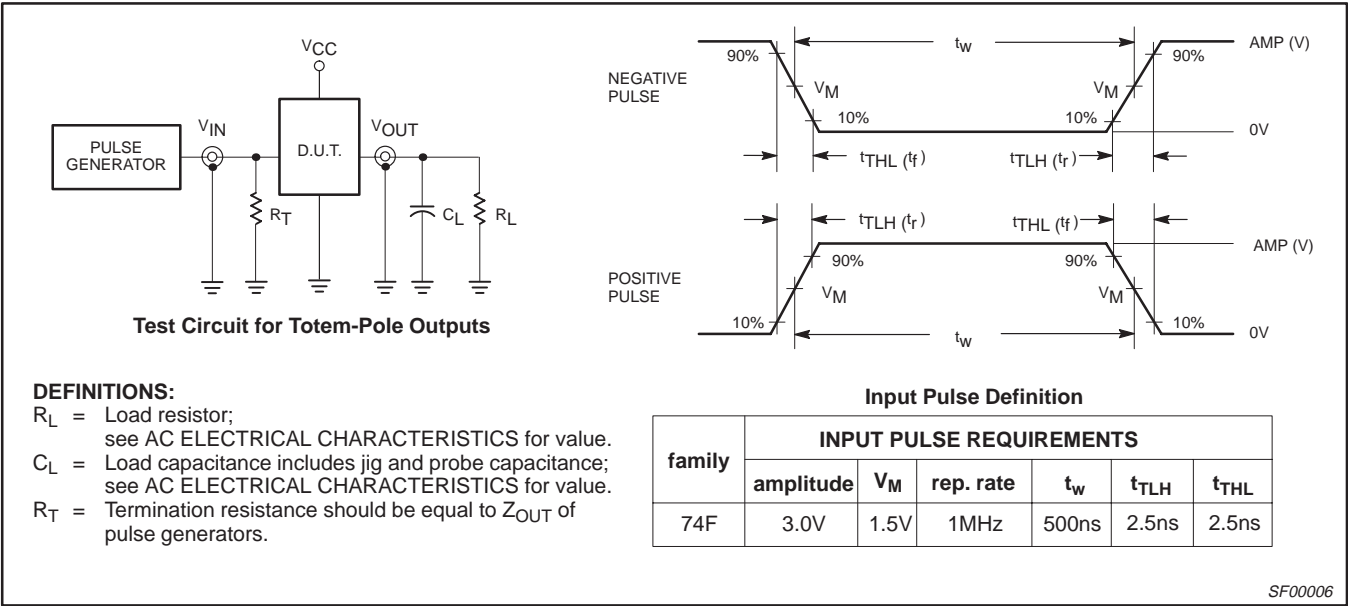
AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .



Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS

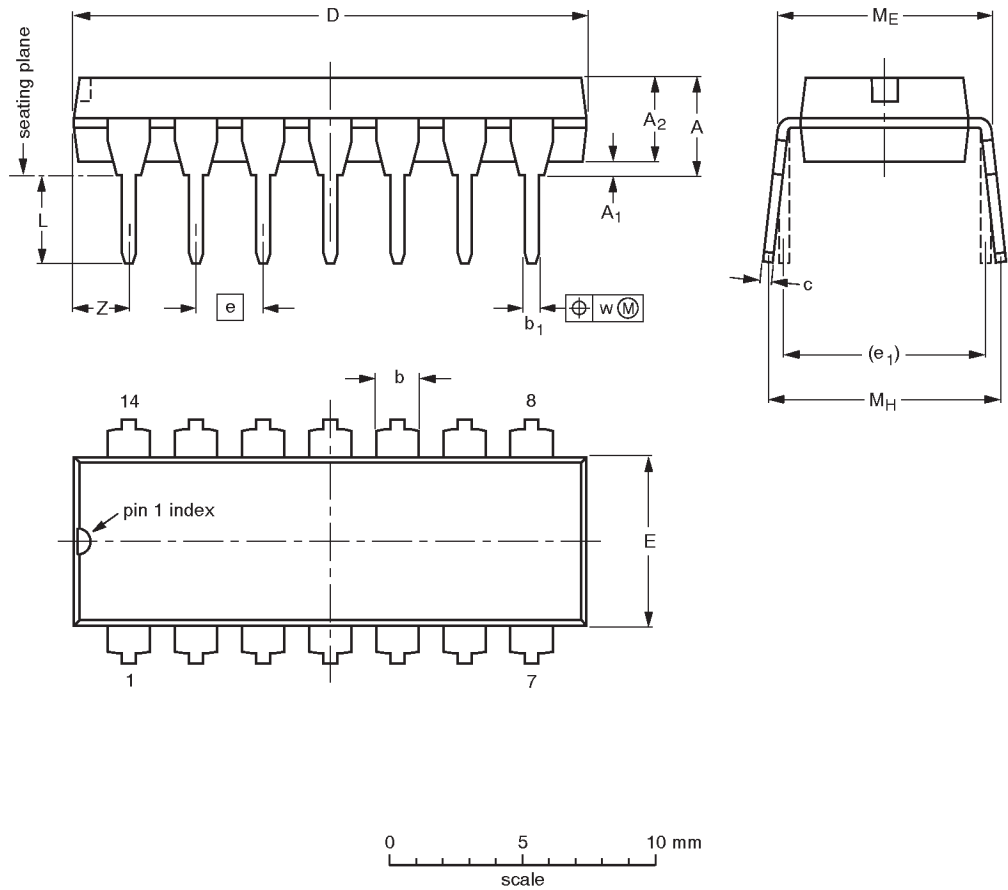


Quad 2-input NAND Schmitt trigger

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

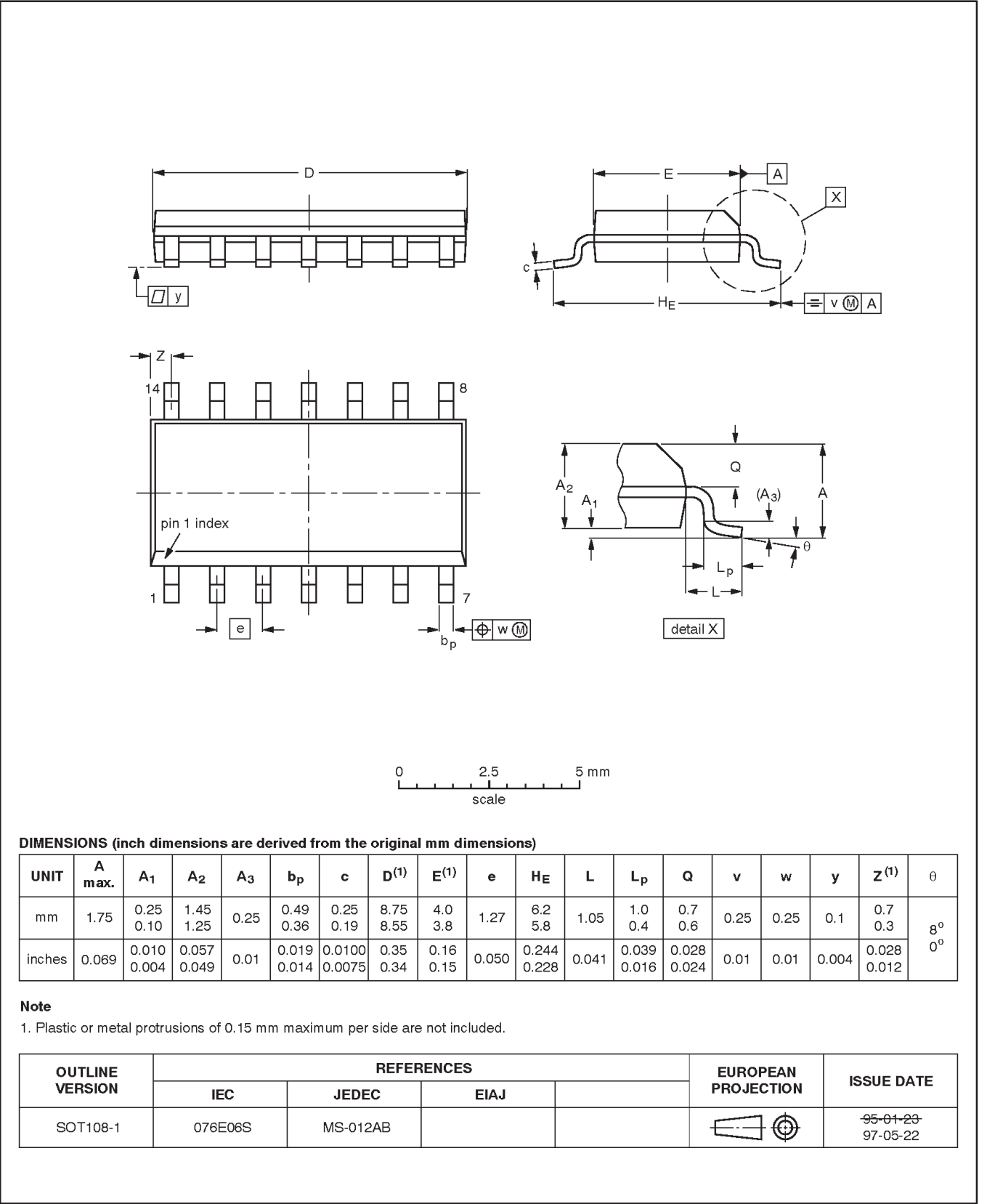
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11

Quad 2-input NAND Schmitt trigger

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



## Quad 2-input NAND Schmitt trigger

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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