# BUK652R7-30C

## N-channel TrenchMOS intermediate level FET

Rev. 02 — 16 December 2010 Product data sheet

# 1. Product profile

## 1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC Q101 standard for use in high performance automotive applications.

## 1.2 Features and benefits

- AEC Q101 compliant
- Suitable for intermediate level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

## 1.3 Applications

- 12 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

## 1.4 Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | - | 30 | V |
| $I_D$ | drain current | $V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1 | [1] | - | - | 100 | A |
| $P_{tot}$ | total power dissipation | $T_{mb} = 25$ °C; see Figure 2 | | - | - | 204 | W |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 13; see Figure 14 | | - | 2.72 | 3.3 | mΩ |
| | | $V_{GS} = 5$ V; $I_D = 15$ A; $T_j = 25$ °C; see Figure 15 | | - | 11.1 | 13 | mΩ |

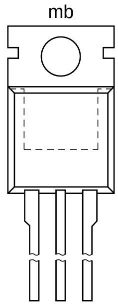
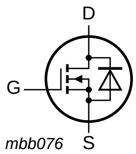
**Table 1. Quick reference data** *...continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 100 A; $V_{sup}$ ≤ 30 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped | - | - | 501 | mJ |
| **Dynamic characteristics** | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 25 A; $V_{DS}$ = 24 V; $V_{GS}$ = 10 V; see Figure 17; see Figure 18 | - | 33.3 | - | nC |

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | G | gate |  SOT78A (TO-220AB) |  |
| 2 | D | drain | | |
| 3 | S | source | | |
| mb | D | mounting base; connected to drain | | |

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BUK652R7-30C | TO-220AB | plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB | SOT78A |

## 4. Limiting values

**Table 4. Limiting values**
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | 30 | V |
| $V_{GS}$ | gate-source voltage | DC | [1] | -16 | 16 | V |
| | | Pulsed | [2] | -20 | 20 | V |
| $I_D$ | drain current | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see Figure 1 | [3] | - | 100 | A |
| | | $T_{mb}$ = 100 °C; $V_{GS}$ = 10 V; see Figure 1 | [3] | - | 100 | A |
| $I_{DM}$ | peak drain current | $T_{mb}$ = 25 °C; pulsed; $t_p \leq 10$ µs; see Figure 3 | | - | 721 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; see Figure 2 | | - | 204 | W |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | [3] | - | 100 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p \leq 10$ µs; $T_{mb}$ = 25 °C | | - | 721 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 100 A; $V_{sup} \leq 30$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped | | - | 501 | mJ |
| $E_{DS(AL)R}$ | repetitive drain-source avalanche energy | | [4][5][6] | - | - | J |

[1] -16V accumulated duration not to exceed 168 hrs

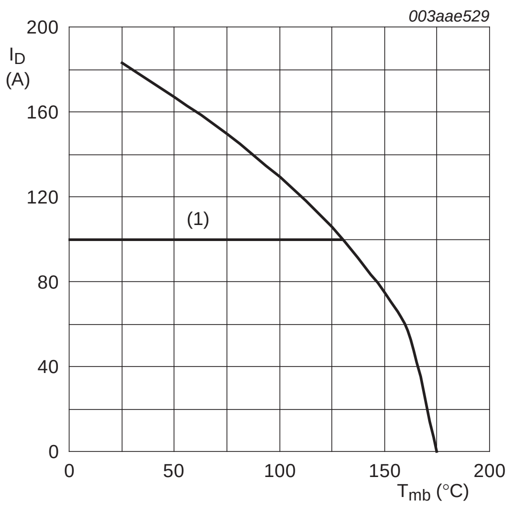
[2] Accumulated pulse duration not to exceed 5mins.

[3] Continuous current is limited by package.

[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[5] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

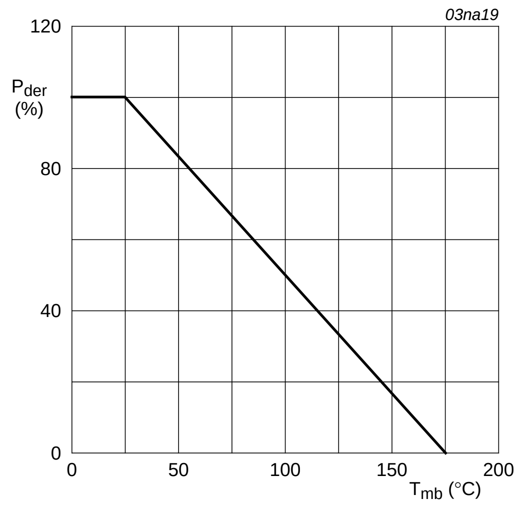
[6] Refer to application note AN10273 for further information.




$V_{GS} \geq 10$ V

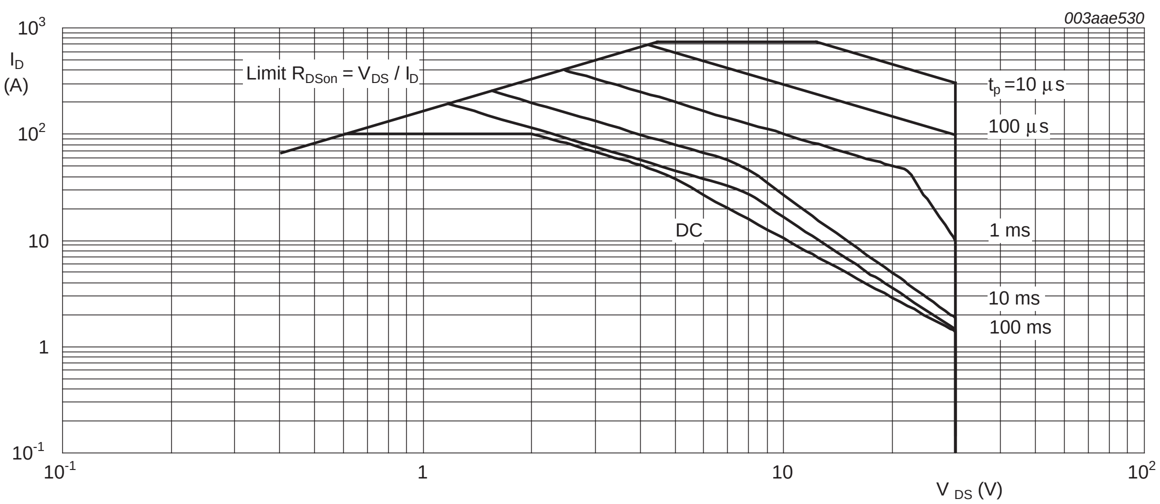
(1) capped at 100 A due to package

**Fig 1. Continuous drain current as a function of mounting base temperature**




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**




$T_{mb}$ = 25°C; $I_{DM}$ is a single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

# 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | - | 0.74 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | vertical in free air | - | 60 | - | K/W |

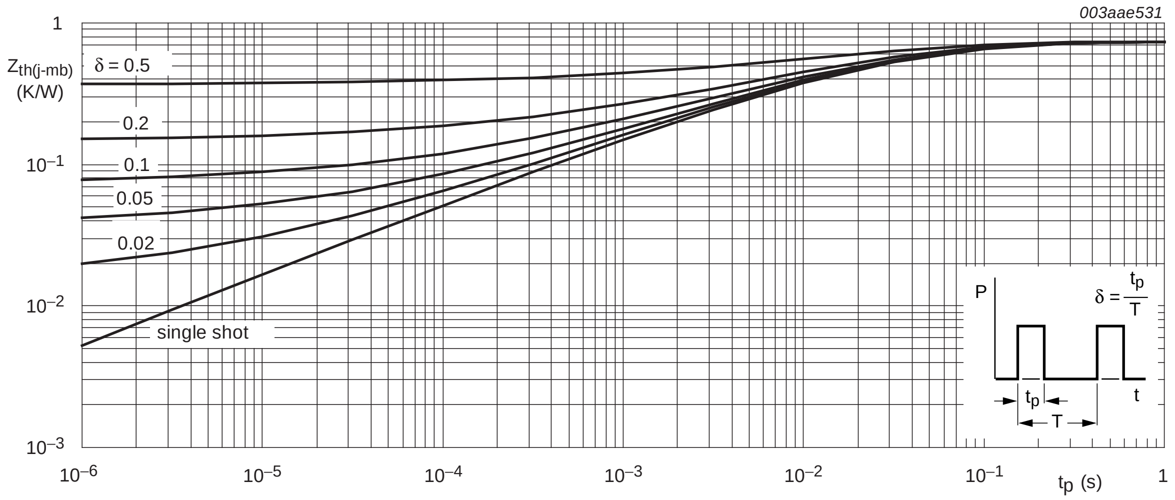



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

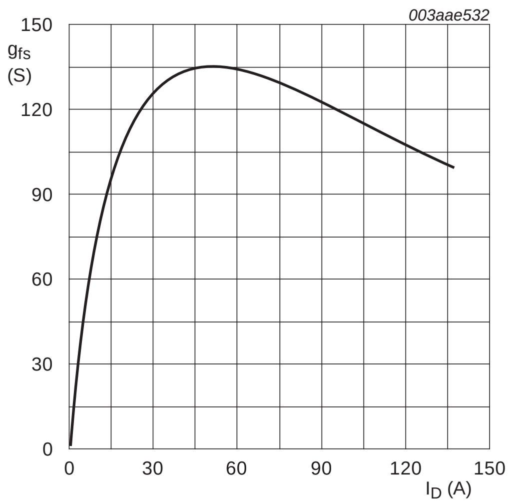
## 6. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | 30 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | 27 | - | - | V |
| | | | 27 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; see Figure 9; see Figure 10 | 1.8 | 2.3 | 2.8 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 175 °C; see Figure 11 | 0.5 | - | - | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; see Figure 10 | - | - | 3.3 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; see Figure 11; see Figure 12 | 1.1 | 1.5 | 2 | V |
| | | $I_D$ = 2.5 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 175 °C; see Figure 10 | 0.8 | - | - | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | - | 0.02 | 1 | µA |
| | | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C | - | - | 500 | µA |
| | | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C | - | - | 500 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | 2 | 100 | nA |
| | | $V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | 2 | 100 | nA |
| | | $V_{GS}$ = -15 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see Figure 13; see Figure 14 | - | 2.72 | 3.3 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 15 A; $T_j$ = 25 °C; see Figure 15 | - | 11.1 | 13 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C; see Figure 13; see Figure 14 | - | 3.9 | 5.3 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 15 A; $T_j$ = 25 °C; see Figure 15 | - | 11.4 | 12 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 15 A; $T_j$ = 25 °C; see Figure 15 | - | 10 | 11.7 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 25 A; $T_j$ = 25 °C; see Figure 13 | - | 3.45 | 4.4 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 175 °C; see Figure 13 | - | 5.75 | 6.3 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 45 A; $V_{DS}$ = 15 V; $V_{GS}$ = 4.5 V; $T_j$ = 25 °C; see Figure 16; see Figure 17 | - | 5.9 | - | C |
| | | $I_D$ = 25 A; $V_{DS}$ = 24 V; $V_{GS}$ = 10 V; see Figure 17; see Figure 18 | - | 114 | - | nC |
| | | $I_D$ = 25 A; $V_{DS}$ = 24 V; $V_{GS}$ = 5 V; see Figure 17; see Figure 18 | - | 66 | - | nC |
| $Q_{GS}$ | gate-source charge | $I_D$ = 25 A; $V_{DS}$ = 24 V; $V_{GS}$ = 10 V; see Figure 17; see Figure 18 | - | 18 | - | nC |
| $Q_{GD}$ | gate-drain charge | | - | 33.3 | - | nC |

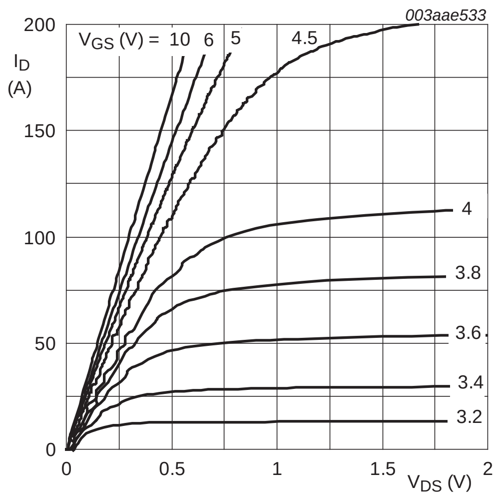
**Table 6. Characteristics** *...continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz; $T_j$ = 25 °C; see Figure 19 | - | 5216 | 6960 | pF |
| $C_{oss}$ | output capacitance | | - | 896 | 1100 | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 537 | 740 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 25 V; $R_L$ = 1 Ω; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 10 Ω | - | 22 | - | ns |
| $t_r$ | rise time | | - | 59 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 209 | - | ns |
| $t_f$ | fall time | | - | 113 | - | ns |
| $L_D$ | internal drain inductance | from drain lead 6 mm from package to centre of die ; $T_j$ = 25 °C | - | 4.5 | - | nH |
| $L_S$ | internal source inductance | from source lead to source bond pad ; $T_j$ = 25 °C | - | 7.5 | - | nH |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; see Figure 20 | - | 0.8 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 20 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 25 V | - | 50 | - | ns |
| $Q_r$ | recovered charge | | - | 73 | - | nC |



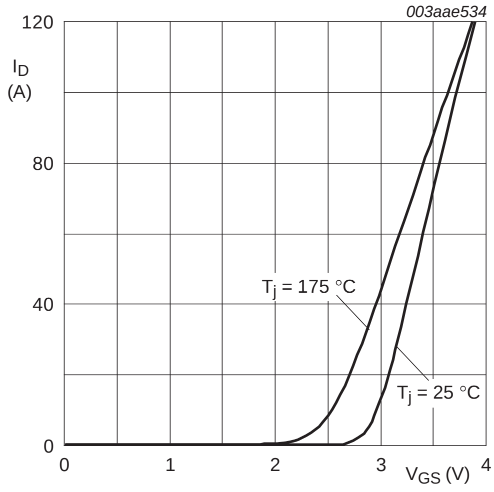

$T_j$ = 25°C; $V_{DS}$ = 25 V

**Fig 5. Forward transconductance as a function of drain current; typical values**



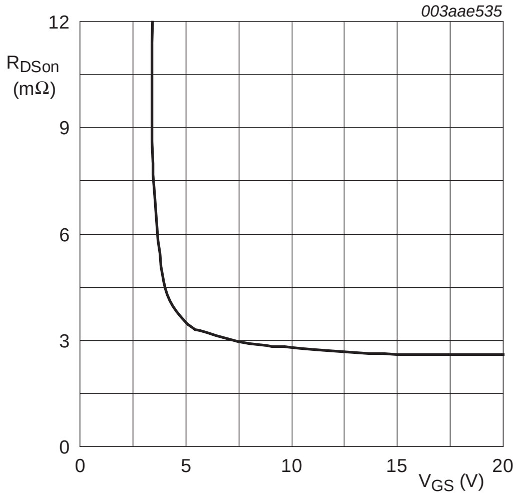

$T_j$ = 25°C and $t_p$ = 300 us

**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



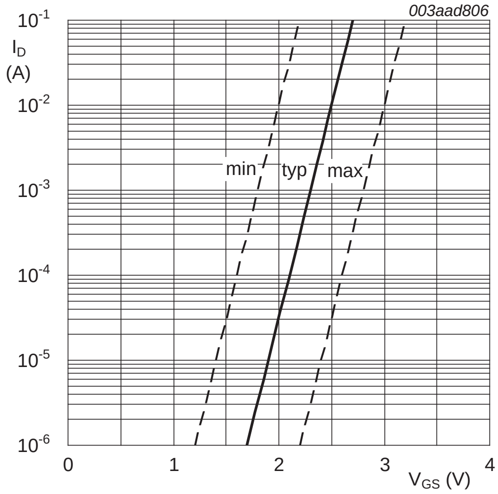

$V_{DS}$ = 25 V

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



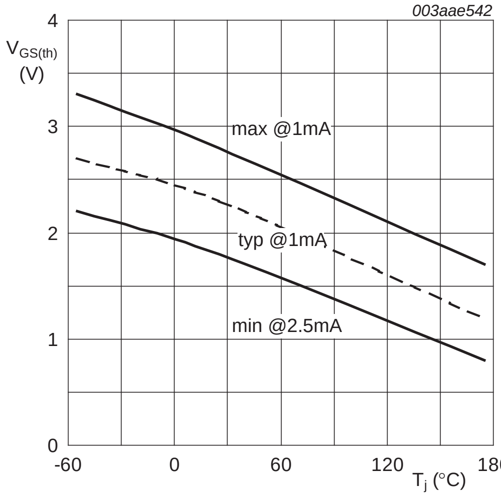

$T_j$ = 25°C; $I_D$ 25 A

**Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**



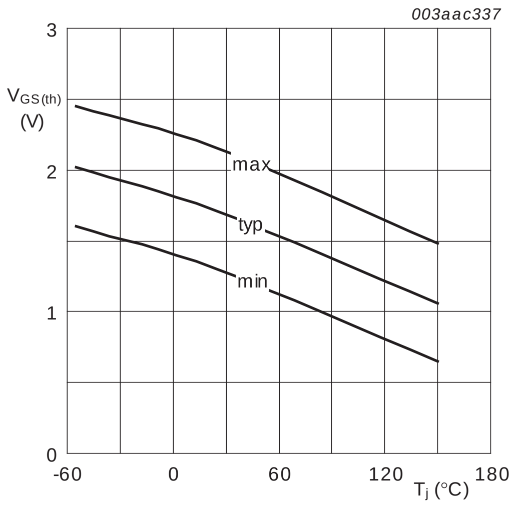

$T_j = 25°C; V_{DS} = 5V$

**Fig 9. Sub-threshold drain current as a function of gate-source voltage**



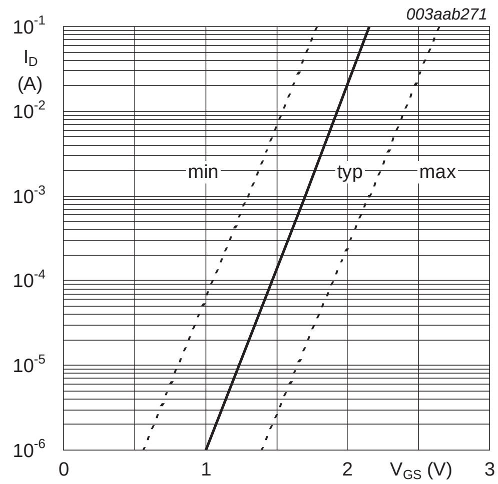

$I_D = 1mA; V_{DS} = V_{GS}$

**Fig 10. Gate-source threshold voltage as a function of junction temperature**



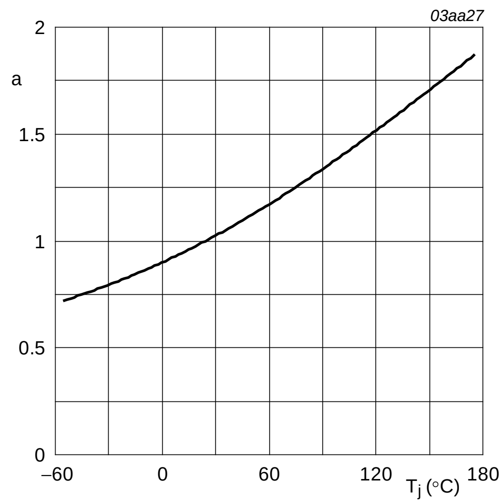

$I_D = 1mA; V_{DS} = V_{GS}$

**Fig 11. Gate-source threshold voltage as a function of junction temperature**



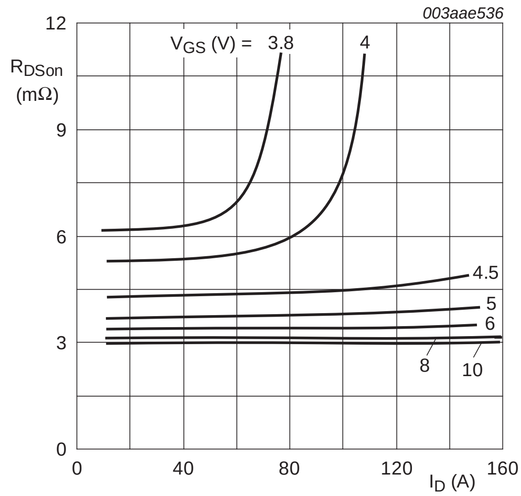

$T_j = 25\,°C; V_{DS} = 5V$

**Fig 12. Sub-threshold drain current as a function of gate-source voltage**



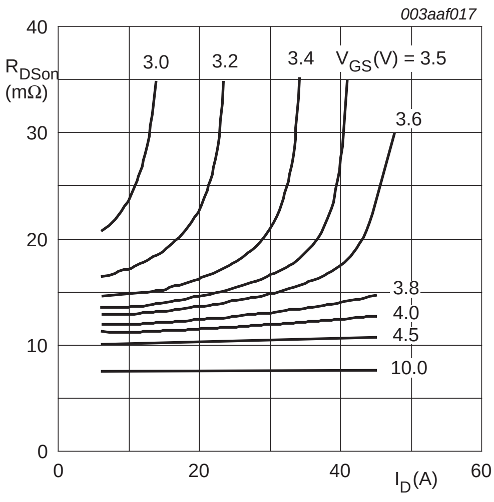

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature**



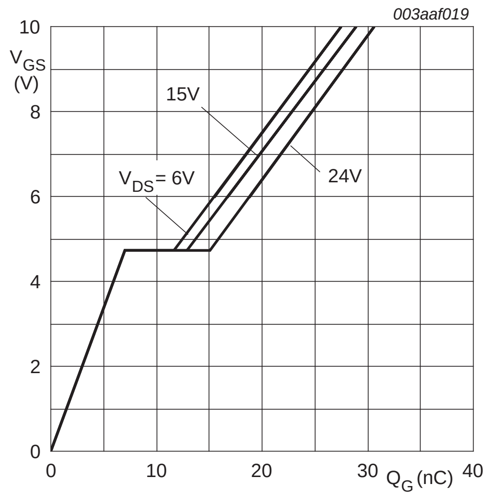

$T_j = 25°C; t_p = 300\ \mu s$

**Fig 14. Drain-source on-state resistance as a function of drain current; typical values**




$T_j = 25°C$

**Fig 15. Drain-source on-state resistance as a function of drain current; typical values**




$T_j = 25°C; I_D = 25A$

**Fig 16. Gate-source voltage as a function of gate charge; typical values**

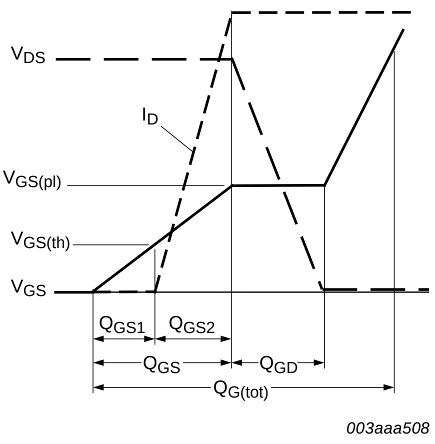
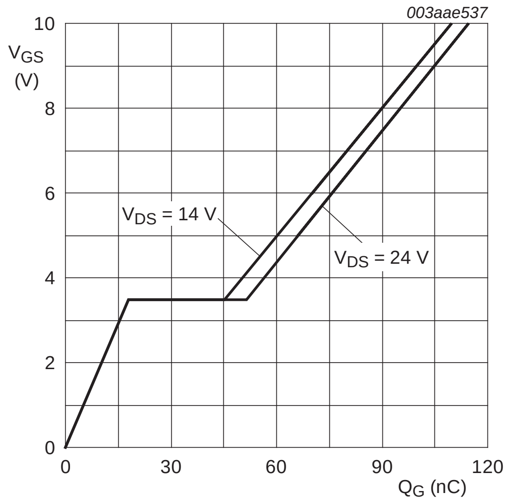
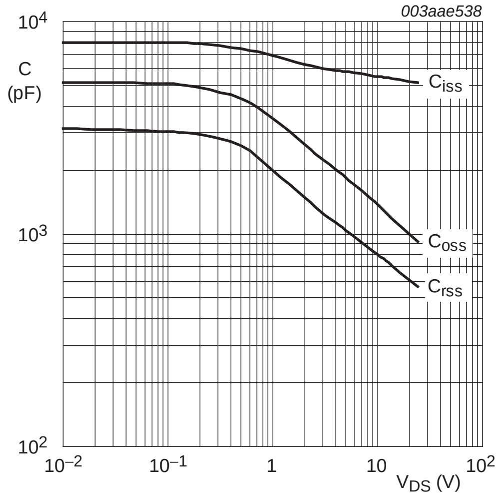



**Fig 17. Gate charge waveform definitions**



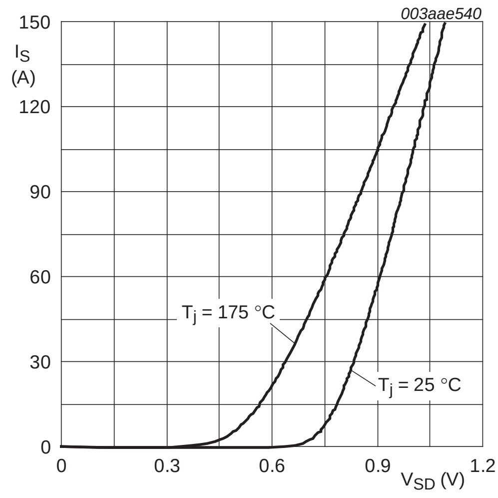

$T_j$ = 25°C and $I_D$ = 25 A

**Fig 18. Gate-source voltage as a function of gate charge; typical values**




$V_{GS}$ = 0 V; f = 1 MHz

**Fig 19. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

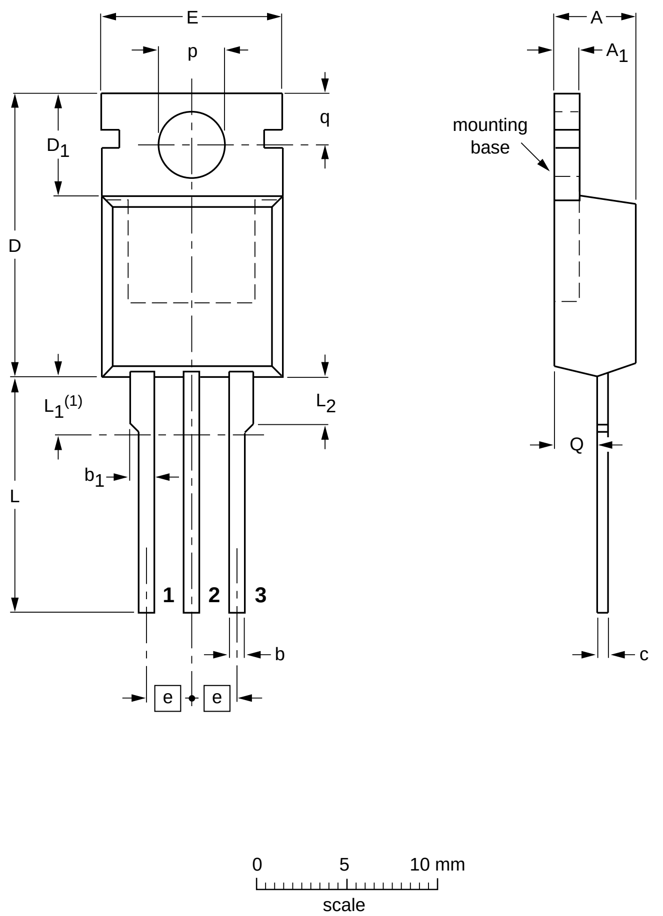



$V_{GS}$ = 0 V

**Fig 20. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

## 7. Package outline

**Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB** **SOT78A**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$ | c | D | $D_1$ | E | e | L | $L_1$(1) | $L_2$ max. | p | q | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.5<br>4.1 | 1.39<br>1.27 | 0.9<br>0.6 | 1.3<br>1.0 | 0.7<br>0.4 | 15.8<br>15.2 | 6.4<br>5.9 | 10.3<br>9.7 | 2.54 | 15.0<br>13.5 | 3.30<br>2.79 | 3.0 | 3.8<br>3.6 | 3.0<br>2.7 | 2.6<br>2.2 |

**Note**

1. Terminals in this zone are not tinned.

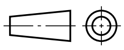
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT78A | | 3-lead TO-220AB | SC-46 | |  | ~~03-01-22~~<br>05-03-14 |

**Fig 21. Package outline SOT78A (TO-220AB)**

## 8. Revision history

**Table 7. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BUK652R7-30C v.2 | 20101216 | Product data sheet | - | BUK652R7-30C v.1 |
| Modifications: | • Various changes to content.<br>• Status changed from Objective to Product. | | | |
| BUK652R7-30C v.1 | 20100705 | Objective data sheet | - | - |

# 9. Legal information

## 9.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 9.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 9.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. The product is not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

### 9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**Adelante**, **Bitport**, **Bitsound**, **CoolFlux**, **CoReUse**, **DESFire**, **EZ-HV**, **FabKey**, **GreenChip**, **HiPerSmart**, **HITAG**, **I²C-bus** logo, **ICODE**, **I-CODE**, **ITEC**, **Labelution**, **MIFARE**, **MIFARE Plus**, **MIFARE Ultralight**, **MoReUse**, **QLPAK**, **Silicon Tuner**, **SiliconMAX**, **SmartXA**, **STARplug**, **TOPFET**, **TrenchMOS**, **TriMedia** and **UCODE** — are trademarks of NXP B.V.

**HD Radio** and **HD Radio** logo — are trademarks of iBiquity Digital Corporation.

## 10. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

## 11. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 16 December 2010**

**Document identifier: BUK652R7-30C**