



BUK961R4-30E

N-channel TrenchMOS logic level FET

Rev. 2 — 16 May 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True Logic level gate with $V_{GS(th)}$ rating of greater than 0.5V at 175 °C

1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

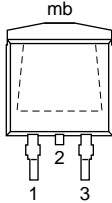
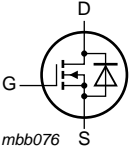
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	30	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	[1]	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	357	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 11	-	1.18	1.4	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 24\text{ V}$; see Figure 13 ; see Figure 14	-	39.2	-	nC

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		
SOT404 (D2PAK)				

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK961R4-30E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
BUK961R4-30E	BUK961R4-30E

5. Limiting values

Table 5. Limiting values

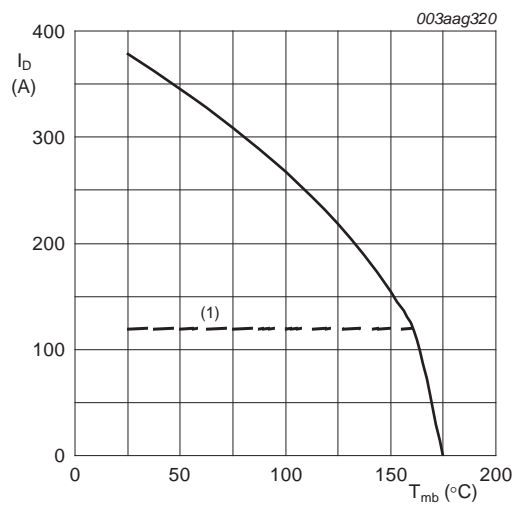
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	30	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	30	V
V _{GS}	gate-source voltage	DC	-10	10	V
		Pulsed	-15	15	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; see Figure 1	[1] -	120	A
		T _{mb} = 100 °C; V _{GS} = 5 V; see Figure 1	[1] -	120	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; see Figure 4	-	1513	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	357	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	[1] -	120	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	1513	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 120 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; see Figure 3	[2][3] -	1380	mJ

[1] Continuous current is limited by package.

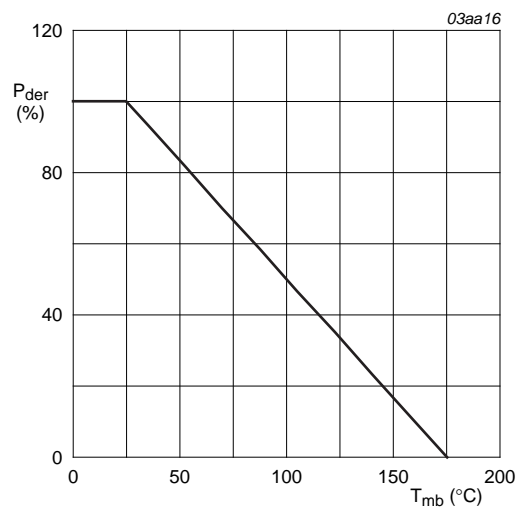
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[3] Refer to application note AN10273 for further information.



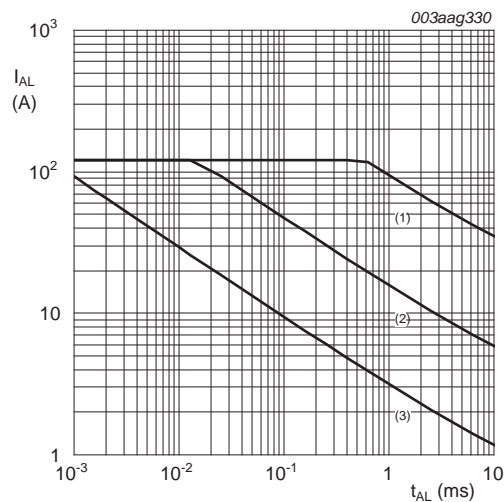
$V_{GS} \geq 5\text{ V}$
(1) Capped at 120 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



(1) $T_j = 25^\circ\text{C}$; (2) $T_j = 150^\circ\text{C}$; (3) Repetitive Avalanche

Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

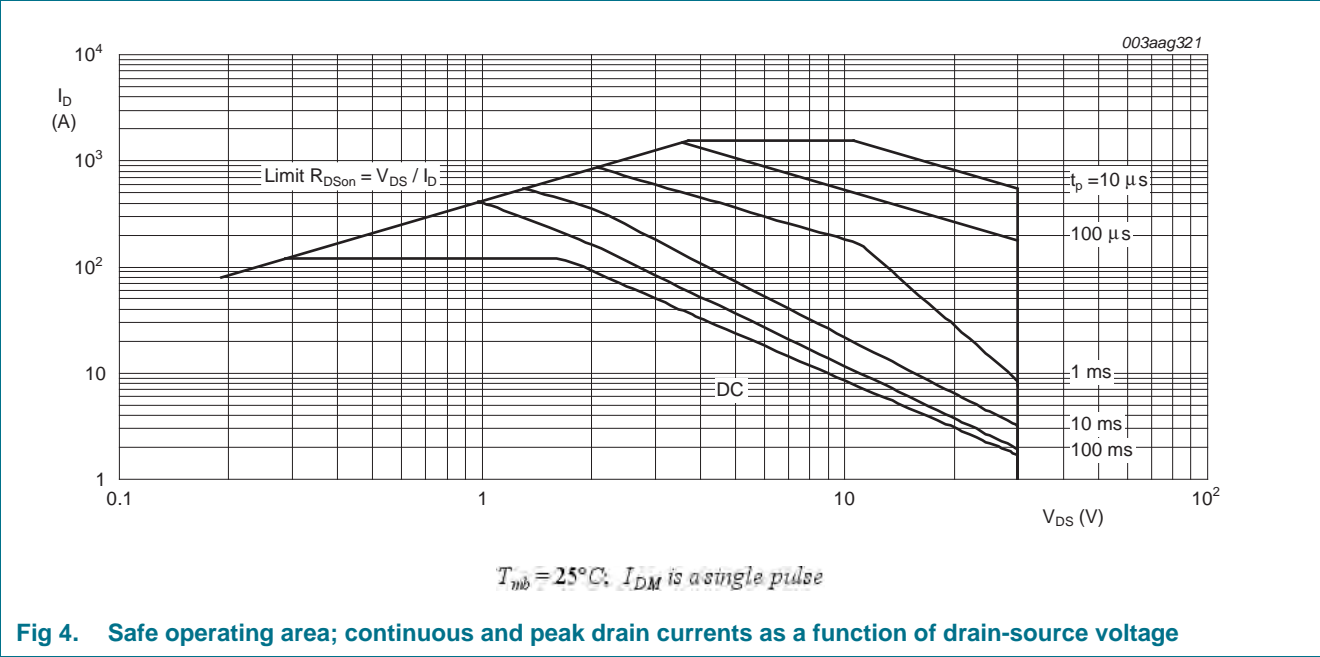


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	0.42	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W

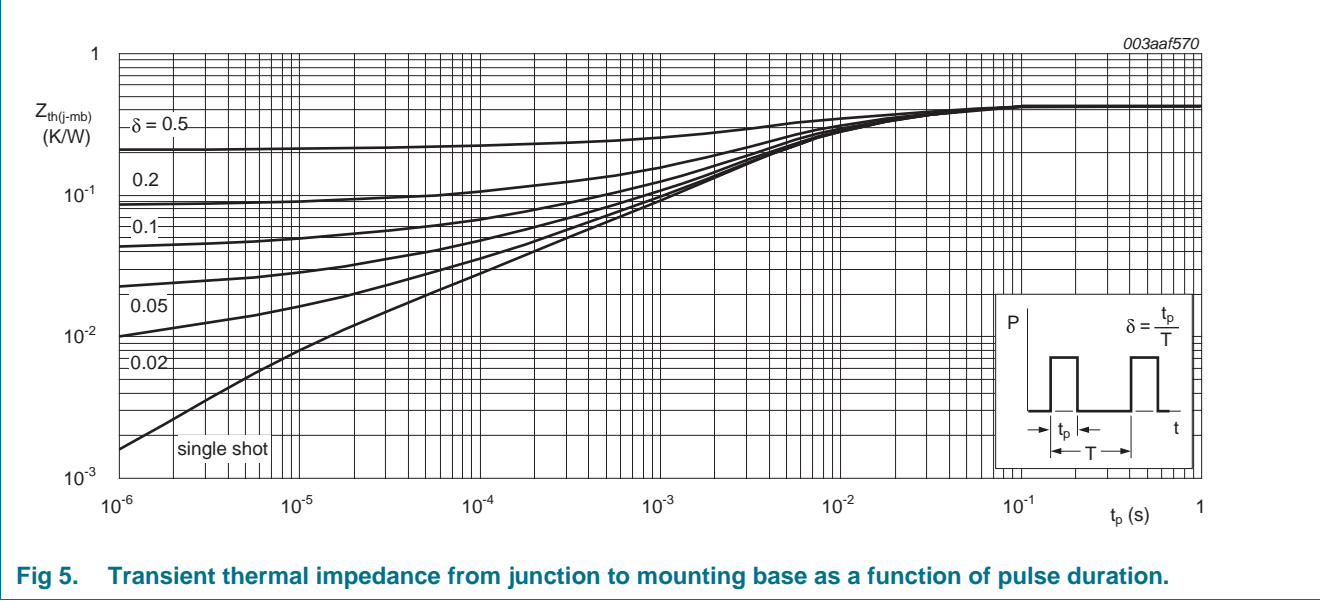


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	30	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 9 ; see Figure 10	1.4	1.7	2.1	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 9	-	-	2.45	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 9	0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C	-	0.1	1	μA
		V _{DS} = 30 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; see Figure 11	-	1.18	1.4	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 11	-	1	1.2	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; see Figure 11 ; see Figure 12	-	-	2.5	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 24 V; V _{GS} = 5 V; see Figure 13 ; see Figure 14	-	113	-	nC
Q _{GS}	gate-source charge		-	29	-	nC
Q _{GD}	gate-drain charge		-	39.2	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; see Figure 15	-	12100	16150	pF
C _{oss}	output capacitance		-	1840	2210	pF
C _{rss}	reverse transfer capacitance		-	898	1240	pF
t _{d(on)}	turn-on delay time	V _{DS} = 25 V; R _L = 1 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω	-	71	-	ns
t _r	rise time		-	127	-	ns
t _{d(off)}	turn-off delay time		-	184	-	ns
t _f	fall time		-	111	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L _S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 16	-	0.76	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V	-	62	-	ns
Q _r	recovered charge		-	112	-	nC

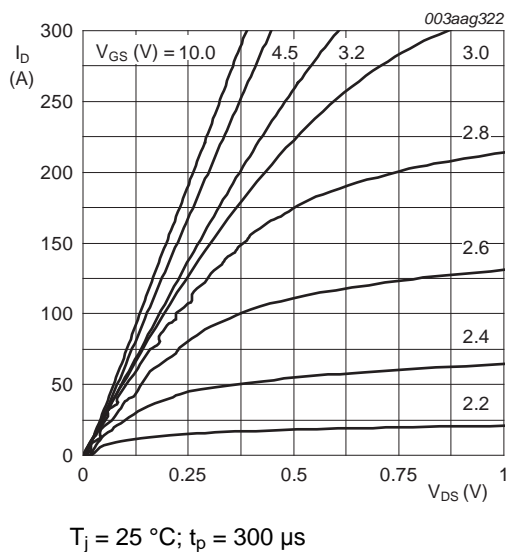


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

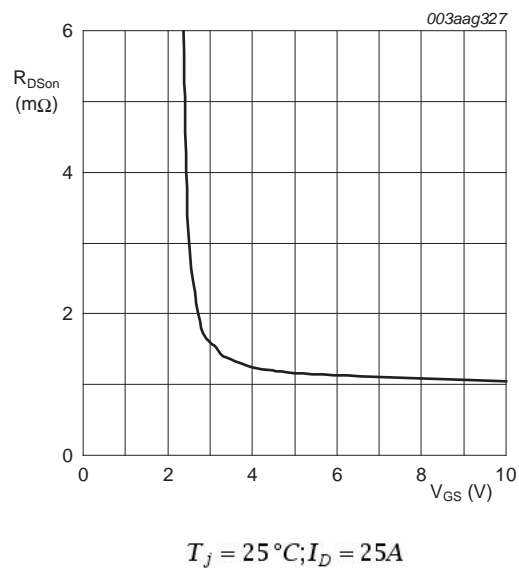


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

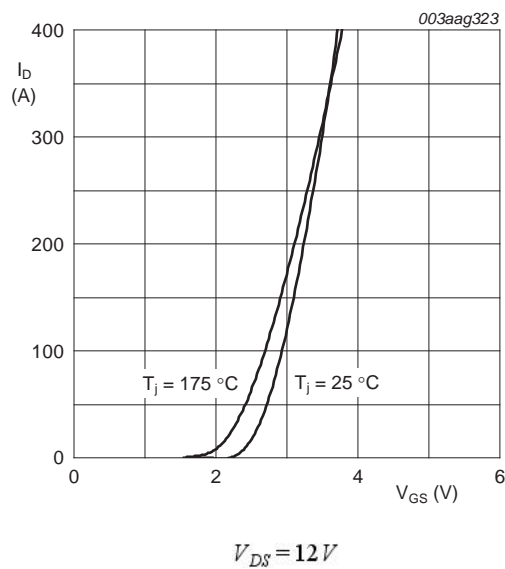


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

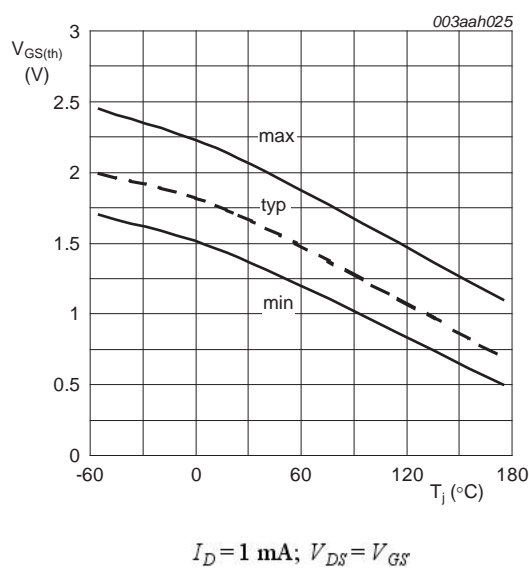


Fig 9. Gate-source threshold voltage as a function of junction temperature

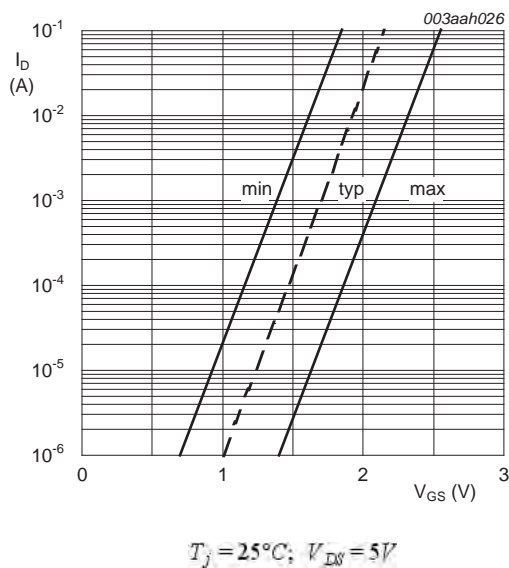


Fig 10. Sub-threshold drain current as a function of gate-source voltage

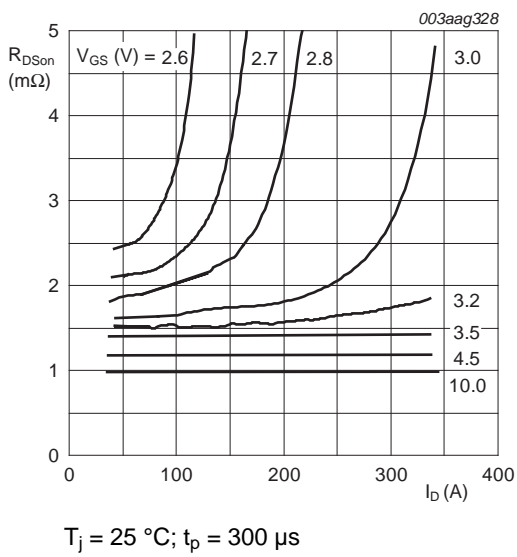


Fig 11. Drain-source on-state resistance as a function of drain current; typical values

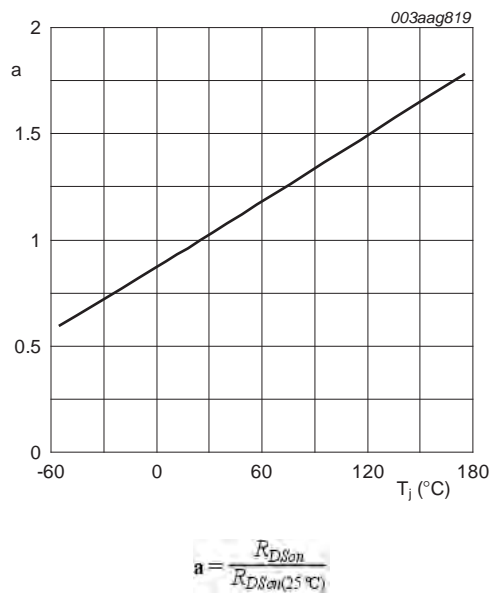


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

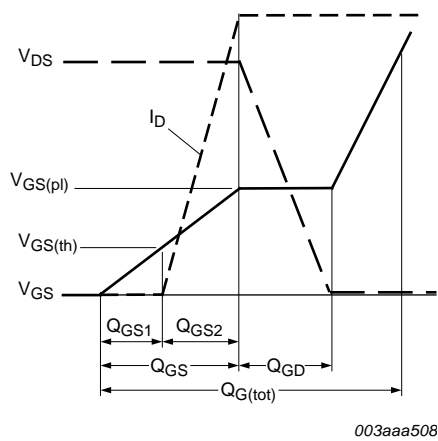
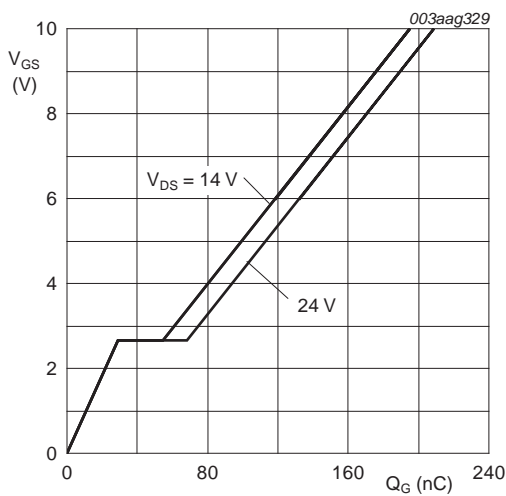
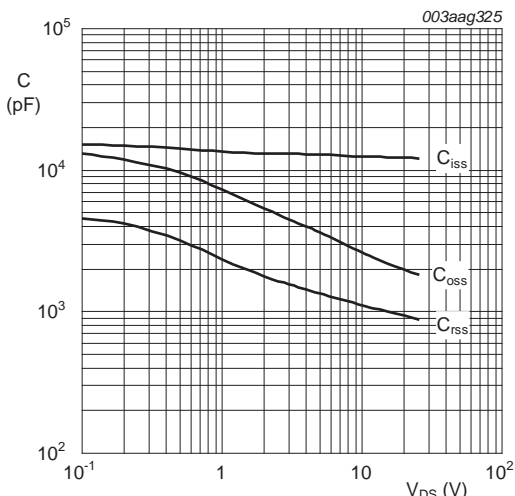


Fig 13. Gate charge waveform definitions



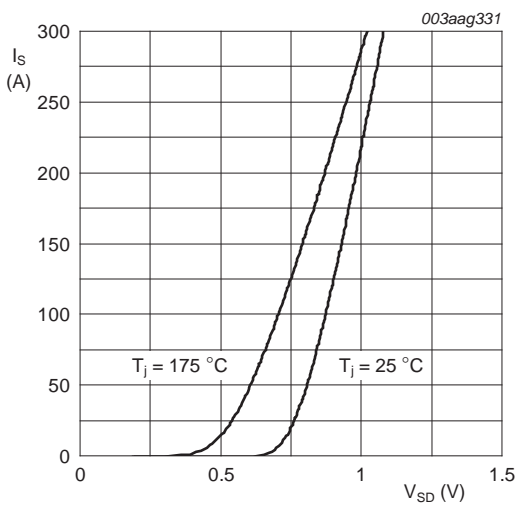
$T_j = 25\text{ }^{\circ}\text{C}$; $I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 17. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK961R4-30E v.2	20120516	Product data sheet	-	BUK961R4-30E v.1
Modifications:	<ul style="list-style-type: none">• Status changed from objective to product.• Various changes to content.			
BUK961R4-30E v.1	20120404	Objective data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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