INTEGRATED CIRCUITS



Product data

2002 May 21



Philips Semiconductors

NE/SA/AU5232

DESCRIPTION

The NE/SA/AU5232 is a matched, low voltage, high performance dual operational amplifier. Among its unique input and output characteristics is the capability for both input and output rail-to-rail operation, particularly critical in low voltage applications. The output swings to less than 50 mV of both rails across the entire power supply range. The NE/SA/AU5232 is capable of delivering 5.5 V peak-to-peak across a 600 Ω load and will typically draw only 700 μ A per amplifier. The bandwidth is 2.5 MHz and the 1% settling time is 1.4 μ s.

FEATURES

- Wide common-mode input voltage range: 250 mV beyond both rails
- Output swing within 50 mV of both rails
- Functionality to 1.8 V typical
- Low current consumption: 700 μA per amplifier
- ±15 mA output current capability
- Unity gain bandwidth: 2.5 MHz
- Slew rate: 0.8 V/µs
- Low noise: 33 nV/√Hz
- Electrostatic discharge protection
- Short-circuit protection
- Output inversion prevention

PIN CONFIGURATION





APPLICATIONS

- Automotive electronics
- Signal conditioning and sensing amplification
- Portable instrumentation
 - Test and measurement
 - Medical monitors and diagnostics
 - Remote meters
- Audio equipment
- Security systems
- Communications
 - Pagers
 - Cellular telephone
 - LAN
 - 5 V Datacom bus
- Error amplifier in motor drives
- Transducer buffer amplifier

ORDERING INFORMATION

ORDER CODE	DESCRIPTION	TEMPERATURE RANGE	DWG #
NE5232D	8-Pin Plastic Small Outline (SO) package	0 °C to +70 °C	SOT96-1
NE5232N	8-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C	SOT97-1
SA5232D	8-Pin Plastic Small Outline (SO) package	–40 °C to +85 °C	SOT96-1
SA5232N	8-Pin Plastic Dual In-Line Package (DIP)	–40 °C to +85 °C	SOT97-1
AU5232N	8-Pin Plastic Dual In-Line Package (DIP)	–40 °C to +125 °C	SOT97-1
AU5232D	8-Pin Plastic Small Outline (SO) package	–40 °C to +125 °C	SOT96-1

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Single supply voltage	7	V
V _{ESD}	ESD protection voltage at any pin ⁵ human body model robot model	2000 200	V V
Vs	Dual supply voltage	±3.5	V
V _{DP}	Voltage at any device pin ¹	$V_{S} \pm 0.5$	V
I _{DP}	Current into any device pin ¹	±50	mA
V _{i(dif)}	Differential input voltage ²	0.5	V
V _{i(CM)}	Common-mode input voltage (positive)	V _{CC} + 0.5	V
V _{i(CM)}	Common-mode input voltage (negative)	V _{EE} - 0.5	V
PD	Power dissipation ³	500	mW
Тј	Operating junction temperature ³	+150	°C
V _{SC}	Supply voltage allowing indefinite output short circuit to either rail ^{3,4}	7	V
T _{stg}	Storage temperature range	-65 to +150	°C
T _{sld}	Lead soldering temperature (10 sec max)	+230	°C
θ _{JA}	Thermal impedance 8-pin plastic DIP 8-pin plastic SO		°C/W °C/W

NOTES:

 Each pin is protected by ESD diodes. The voltage at any pin is limited by the ESD diodes.
The differential input of each amplifier is limited by two internal diodes, connected in parallel and opposite to each other. For more differential input range, use differential resistors in series with the input pins. The maximum operating junction temperature is +150 °C. At elevated temperatures, devices must be derated according to the package

3. thermal resistance and device mounting conditions. Derates above +25 °C: N package at 9.5 mW/°C; D package at 6.25 mW/°C.

Simultaneous short circuits of two amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual 4. destruction of the device.

5. Guaranteed by design.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Single supply voltage	+2 to +5.5	V
VS	Dual supply voltage	±1 to ±2.75	V
V _{i(CM)}	Common-mode input voltage (positive)	V _{CC} + 0.25	V
V _{i(CM)}	Common-mode input voltage (negative)	V _{EE} – 0.25	V
	Temperature		
т.	NE	0 to +70	°C
'amb	SA	-40 to +85	°C
	AU	-40 to +125	°C

DC ELECTRICAL CHARACTERISTICS

 V_{CC} = 2 V to 5.5 V, V_{EE} = 0 V, T_{amb} = 25 °C; V_{EE} < $V_{i(CM)}$ < V_{CC} ; unless otherwise stated.

			LIMITS							
SYMBOL	PARAMETER	TEST CONDITIONS		NE5232	2		SA5232	2	UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX	1	
		V _{CC} = 5.5V		1.4	2.0		1.4	2.0		
Icc	Supply current	V _{CC} = 5.5 V; over full temp. range		1.5	2.3		1.6	2.4	mA	
V	Offeet veltere			±0.2	±4		±0.2	±4	m\/	
VOS	Oliset voltage	Over full temp. range		±0.4	±5		±0.6	±5		
$\Delta V_{OS} / \Delta T$	Offset voltage drift with temperature			4			4		μV/°C	
AVos	Offset voltage difference between any amplifiers in			0.4	3		0.4	3	mV	
	same common mode level ¹	Over full temp. range		0.8	4		1.2	4		
108	Offset current			±3	±20		±3	±30	nA	
103		Over full temp. range		±4	±30		±6	±60		
$\Delta I_{OS} / \Delta T$	Offset current drift with temperature			0.02	±.3		0.03	±.3	nA/°C	
		$V_{EE} < V_{i(CM)} < V_{EE}$ +0.5 V	-200	-90		-200	-90			
	Input biog ourrept1	Over full temp. range	-225	-100		-250	-150			
^I B	Input blas current	V_{EE} +1 V < $V_{i(CM)}$ < V_{CC}		25	70		25	75		
		Over full temp. range		35	100		35	120		
$\Delta I_{B} / \Delta T$	Input bias current drift with temperature			0.5			0.5		nA/°C	
	Input bias current	$V_{EE} < V_{i(CM)} < V_{EE}$ +0.5 V		10	30		10	30		
ΔI_B	difference between any	Over full temp. range		25	50		50	70	nA	
	package at the same	V_{EE} +1 V < $V_{i(CM)}$ < V_{CC}		5	20		5	20		
	common mode level.	Over full temp. range		15	30		25	50	1	
		$V_{OS} \le 6 \text{ mV}$	V _{EE} -0.25		V _{CC} +0.25	V _{EE} -0.25		V _{CC} +0.25		
V _{i(CM)}	Common-mode input range	V _{OS} ≤ 6 mV; Over full temp. range	V _{EE} 0.1		V _{CC} +0.1	V _{EE} -0.1		V _{CC} +0.1	V	
	Common-mode rejection	V _{EE} < V _{i(CM)} < V _{EE} +0.5V; V _{EE} +1V < V _{i(CM)} < V _{CC}	80	100		80	100			
CMRR	ratio, small signal	Over full temp. range	75	100		75			dB	
	Common-mode rejection	$V_{EE} < V_{i(CM)} < V_{CC}$	65	90		65	90		1	
	ratio, large signal	Over full temp. range	60	80		60			1	
0000	Power supply rejection	$V_{EE} < V_{i(CM)} < V_{CC}$	80	100		80	100		-ID	
PSRR	ratio	Over full temp. range	80	90		80	90		ав	
	Peak load current, sink and		10	12		10	12			
<u>''</u>	source	Over full temp. range	5	8		5	8			
			90	110		90	110			
AVOL	Open-loop voltage gain	Over full temp. range		90			90			
		I _{PEAK} = 0.1 mA	V _{EE} +0.05		V _{CC} -0.05	V _{EE} +0.1		V _{CC} -0.1		
	Output voltage swing	I _{PEAK} = 10 mA	V _{EE} +0.25		V _{CC} -0.25	V _{EE} +0.25		V _{CC} -0.25		
V _{OUT}		I _{PEAK} = 5 mA; over full temp. range	V _{EE} +0.22		V _{CC} -0.22	V _{EE} +0.2		V _{CC} -0.2		
	Output voltage swing for	$R_L = 2 k\Omega$	V _{EE} +0.2		V _{CC} -0.2	V _{EE} +0.2		V _{CC} -0.2		
	$V_{CC} = 2.75 \text{ V}, V_{EE} = -2.75 \text{ V}$	R _L = 600 Ω	V _{EE} +0.25		V _{CC} -0.25	V _{EE} +0.25		V _{CC} -0.25		

NOTE:

These parameters are measured for V_{EE} < V_{CM} < V_{EE}+0.5 V and for V_{EE}+1 V < V_{CM} < V_{CC}. By design these parameters are intermediate for common mode ranges between the measured regions.

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DC ELECTRICAL CHARACTERISTICS

 V_{CC} = 2 V to 5.5 V, V_{EE} = 0 V, T_{amb} = 25 °C; V_{EE} < $V_{i(CM)}$ < V_{CC} ; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS		AU5232	2	UNIT		
			MIN	TYP	MAX			
		$V_{CC} = 5.5V$		1.4	2.0			
Icc	Supply current	V _{CC} = 5.5 V; over full temp. range		1.6	2.4	mA		
Vee	Offect voltage			±0.2	±4	m\/		
VOS	Cliser voltage	Over full temp. range		±0.6	±5			
$\Delta V_{OS} / \Delta T$	Offset voltage drift with temperature			4		μV/°C		
11/22	Offset voltage difference between any amplifiers in the			0.4	3	m\/		
∆v0s	same package at the same common mode level ¹	Over full temp. range		1.2	4			
100				±3	±30	nΑ		
105		Over full temp. range		±6	±60			
$\Delta I_{OS} / \Delta T$	Offset current drift with temperature			0.03	±.3	nA/°C		
		$V_{EE} < V_{i(CM)} < V_{EE}$ +0.5 V	-200	-90				
	Input bias current ¹	Over full temp. range	-250	-150		nA		
I 'B		V_{EE} +1 V < $V_{i(CM)}$ < V_{CC}		25	75			
		Over full temp. range		35	120			
$\Delta I_B / \Delta T$	Input bias current drift with temperature			0.5		nA/°C		
	Input bias current difference between any amplifier in the	$V_{EE} < V_{i(CM)} < V_{EE}$ +0.5 V		10	30	nA		
ΔI_B		Over full temp. range		50	70			
	same package at the same common mode level.	V_{EE} +1 V < $V_{i(CM)}$ < V_{CC}		5	20			
		Over full temp. range		25	50			
		$V_{OS} \le 6 \text{ mV}$	V _{EE} -0.25		V _{CC} +0.25			
V _{i(CM)}	Common-mode input range	$V_{OS} \le 6 \text{ mV};$ Over full temp. range	V _{EE} 0.1		V _{CC} +0.1	V		
	Common-mode rejection ratio, small signal	$\label{eq:VEE} \begin{array}{l} V_{EE} < V_{i(CM)} < V_{EE} + 0.5V; \\ V_{EE} + 1V < V_{i(CM)} < V_{CC} \end{array}$	80	100				
CMRR		Over full temp. range	70			dB		
	Common-mode rejection ratio large signal	$V_{EE} < V_{i(CM)} < V_{CC}$	65	90				
	Sommon mode rejection ratio, large signal	Over full temp. range	55					
DODD	Power supply rejection ratio	$V_{EE} < V_{i(CM)} < V_{CC}$	80	100		dB		
		Over full temp. range	75	90		uD		
I 1.	Peak load current sink and source		10	12		mA		
·Ľ		Over full temp. range	5	8				
Avoi	Open-loop voltage gain		90	110		dB		
/ VOL		Over full temp. range		90		uD		
		I _{PEAK} = 0.1 mA	V _{EE} +0.1		V _{CC} -0.1			
	Output voltage swing	I _{PEAK} = 10 mA	V _{EE} +0.25		V _{CC} -0.25	V		
V _{OUT}		I _{PEAK} = 5 mA; over full temp. range	V _{EE} +0.2		V _{CC} -0.2			
	Output voltage swing for	$R_L = 2 k\Omega$	V _{EE} +0.2		V _{CC} -0.2	V		
	V _{CC} = 2.75 V, V _{EE} = -2.75 V	$R_{L} = 600 \Omega$	V _{EE} +0.25		V _{CC} -0.25	,		

NOTE:
1. These parameters are measured for V_{EE} < V_{CM} < V_{EE}+0.5 V and for V_{EE}+1 V < V_{CM} < V_{CC}. By design these parameters are intermediate for common mode ranges between the measured regions.

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AC ELECTRICAL CHARACTERISTICS

 T_{amb} = +25 °C; V_{CC} = 2 V to 5.5 V; R_L = 10 kΩ; C_L = 100 pF; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS		NE5232		s	UNIT		
			MIN	ТҮР	MAX	MIN	TYP	MAX	
SR	Slew rate	Over full temperature range	0.5	0.8		0.5	0.8		V/µs
BW	Unity gain bandwidth: –3 dB	Over full temperature range	2	2.5	4.0	2	2.5	4.0	MHz
θΜ	Phase Margin	C _L = 50 pF		55			55		deg
t _S	1% settling time	$A_V = 1, 1 V \text{ step}$		1.4			1.4		μs
V _N	Input referred voltage noise	$A_V = 1$, $R_S = 0 \Omega$, at 1 kHz		33			33		nV/Hz ^{1/2}
THD	Total harmonic distortion	10 kHz, 1V _{P-P} , A _V = 1		0.1			0.1		%

OUTPUT INVERSION PREVENTION



Figure 2. Output inversion prevention.

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DIP8: plastic dual in-line package; 8 leads (300 mil) D M_{E} seating plane ⊕ wM 7 b₁ е (e₁ M_H b2 pin 1 index 4 10 mm 5 scale DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	с	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	м _н	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

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1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN				
VERSION	VERSION IEC		EIAJ		PROJECTION	ISSUE DATE	
SOT97-1	050G01	MO-001	SC-504-8			-95-02-04 99-12-27	

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NOTES

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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Contact information

For additional information please visit http://www.semiconductors.philips.com. Fax: +31 40 27 24825

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For sales offices addresses send e-mail to: sales.addresses@www.semiconductors.philips.com

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