NTSX2102

Dual supply translating transceiver; open drain; auto direction sensing

Rev. 2 — 11 February 2013 Product data sheet

1. General description

The NTSX2102 is a 2-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 2-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both supplies can be supplied at any voltage between 1.65 V and 5.5 V. This flexibility makes the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.65 V to 5.5 V and $V_{CC(B)}$: 1.65 V to 5.5 V
- Maximum data rates:
  - 50 Mbps
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - HBM JS-001 Class 2 exceeds 2000 V
  - CDM JESD22-C101E exceeds 2000 V
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options
- Specified from –40 °C to +85 °C

3. Applications

- I^2C/SMBus
- UART
- GPIO

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NTSX2102GM	–40 °C to +85 °C	XQFN8	plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2
NTSX2102GU8	–40 °C to +85 °C	XQFN8	XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.4 × 1.2 × 0.5 mm	SOT1309-1
NTSX2102GD	–40 °C to +85 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT996-2

5. Marking

Table 2. Marking

Type number	Marking code
NTSX2102GM	sX2
NTSX2102GU8	sX
NTSX2102GD	sX2

6. Functional diagram

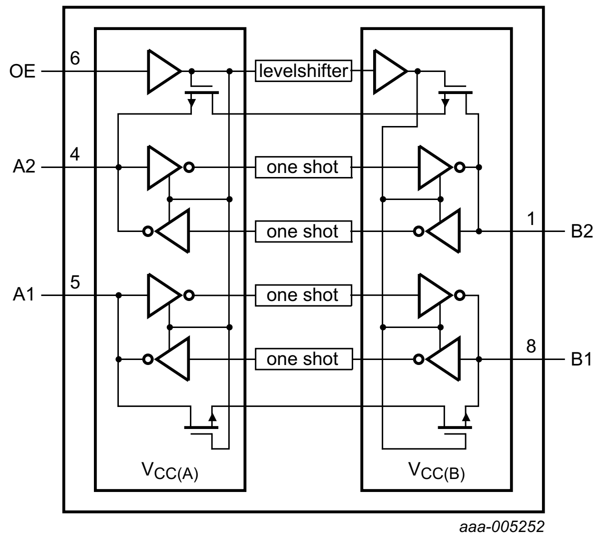


Fig 1. Logic symbol

7. Pinning information

7.1 Pinning

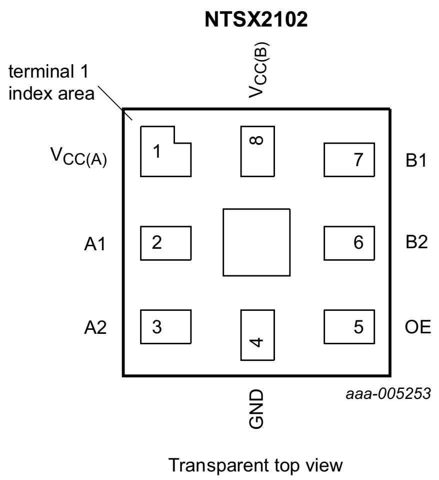


Fig 2. Pin configuration SOT902-2 (XQFN8)

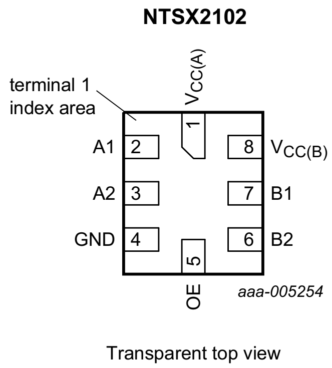


Fig 3. Pin configuration SOT1309-1 (XQFN8)

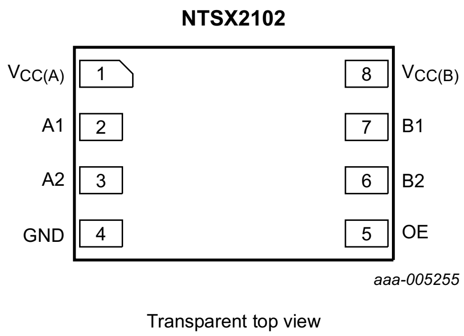


Fig 4. Pin configuration SOT996-2 (XSON8)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
B2, B1	6, 7	data input or output (referenced to $V_{CC(B)}$)
GND	4	ground (0 V)
$V_{CC(A)}$	1	supply voltage A
A2, A1	3, 2	data input or output (referenced to $V_{CC(A)}$)
OE	5	output enable input (active HIGH; referenced to $V_{CC(A)}$)
$V_{CC(B)}$	8	supply voltage B

8. Functional description

Table 4. Function table[1]

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	An	Bn
1.65 V to 5.5 V	1.65 V to 5.5 V	L	Z	Z
1.65 V to 5.5 V	1.65 V to 5.5 V	H	input or output	output or input
GND[2]	GND[2]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into power-down mode.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			–0.5	+6.5	V
$V_{CC(B)}$	supply voltage B			–0.5	+6.5	V
V_I	input voltage	A port and OE input	[1][2]	–0.5	+6.5	V
		B port	[1][2]	–0.5	+6.5	V
V_O	output voltage	Active mode	[1][2]			
		A or B port		–0.5	V_{CCO} + 0.5	V
		Power-down or 3-state mode	[1]			
		A or B port		–0.5	+6.5	V
I_{IK}	input clamping current	V_I < 0 V		–50	-	mA
I_{OK}	output clamping current	V_O < 0 V		–50	-	mA
I_O	output current	V_O = 0 V to V_{CCO}	[2]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C		-	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output.

10. Recommended operating conditions

Table 6. Recommended operating conditions[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.65	5.5	V
$V_{CC(B)}$	supply voltage B		1.65	5.5	V

Table 6. Recommended operating conditions[1] *...continued*

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	ambient temperature		–40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A, B or OE port			
		$V_{CC(A)}$ = 1.65 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	10	ns/V

[1] Hold the A and B sides of an unused I/O pair in the same state, both at V_{CCI} or both at GND.

11. Static characteristics

Table 7. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	input capacitance	OE input; $V_{CC(A)} = V_{CC(B)}$ = 0 V	-	2.2	-	pF
$C_{I/O}$	input/output capacitance	A or B port; $V_{CC(A)}$ = 5.0 V; $V_{CC(B)}$ = 5.0 V	-	10	-	pF

[1] V_{CCO} is the supply voltage associated with the output.

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		–40 °C to +85 °C		Unit
				Min	Max	
V_{IH}	HIGH-level input voltage	A or B port				
		$V_{CC(A)}$ = 1.65 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	[1]	V_{CCI} – 0.4	-	V
		OE input				
		$V_{CC(A)}$ = 1.65 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		0.65$V_{CC(A)}$	-	V
V_{IL}	LOW-level input voltage	A or B port				
		$V_{CC(A)}$ = 1.65 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	0.4	V
		OE input				
		$V_{CC(A)}$ = 1.65 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	0.35$V_{CC(A)}$	V
V_{OL}	LOW-level output voltage	A or B port; I_O = 6 mA	[2]			
		$V_I \leq$ 0.15 V; $V_{CC(A)}$ = 1.65 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	0.4	V
I_I	input leakage current	OE input; V_I = 0 V to $V_{CC(A)}$; $V_{CC(A)}$ = 1.65 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	±1	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V to 5.5 V	[2]	-	±2	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 5.5 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V		-	±2	μA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 5.5 V		-	±2	μA

Table 8. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		–40 °C to +85 °C		Unit
				Min	Max	
I_{CC}	supply current	V_I = 0 V or V_{CCI}; I_O = 0 A	[1]			
		$I_{CC(A)}$				
		$V_{CC(A)}$ = 1.65 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V; OE = LOW or HIGH		-	5	µA
		$V_{CC(A)}$ = 1.65 V to 5.5 V; $V_{CC(B)}$ = 0 V		-	2	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	–2	µA
		$I_{CC(B)}$				
		$V_{CC(A)}$ = 1.65 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V; OE = LOW		-	5	µA
		$V_{CC(A)}$ = 1.65 V to 5.5 V; $V_{CC(B)}$ = 0 V		-	–2	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	2	µA

[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.

12. Dynamic characteristics

Table 9. Typical dynamic characteristics for temperature 25 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for waveforms see Figure 5 and Figure 6.

Symbol	Parameter	Conditions		V_{CCO}[1]				Unit
				1.8 V	2.5 V	3.3 V	5.0 V	
t_{TLH}	LOW to HIGH output transition time	A or B port		7	5	4	3	ns
t_{THL}	HIGH to LOW output transition time	A or B port		4	6	8	11	ns
C_{PD}	power dissipation capacitance	OE = $V_{CC(A)}$; $V_{CC(A)}$ = $V_{CC(B)}$; f_i = 400 kHz; V_I = V_{CCI}[3]	[2]	-	-	-	13.5	pF

[1] V_{CCO} is the supply voltage associated with the output.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[3] V_{CCI} is the supply voltage associated with the input.

Table 10. Dynamic characteristics for temperature range –40 °C to +85 °C[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for wave forms see Figure 5 and Figure 6.

Symbol	Parameter	Conditions		$V_{CC(B)}$								Unit
				1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Typ	Max	Typ	Max	Typ	Max	Typ	Max	
$V_{CC(A)}$ = 1.8 V ± 0.15 V												
t_{PHL}	HIGH to LOW propagation delay	A to B		3	7	3	6	3	5	5	7	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		5	12	5	8	4	8	4	7	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		3	7	3	6	3	5	5	7	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		5	12	1	3	1	2	1	2	ns
t_{PZL}	OFF-state to LOW propagation delay	OE to A		9	16	9	18	10	14	10	15	ns
		OE to B		9	16	6	12	6	12	6	14	ns
t_{PLZ}	LOW to OFF-state propagation delay	OE to A		100	120	100	120	100	120	100	120	ns
		OE to B		100	120	100	120	100	120	100	120	ns
$t_{sk(o)}$	output skew time	between channels	[2]	-	1	-	1	-	1	-	1	ns
f_{data}	data rate			-	18	-	18	-	18	-	18	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V												
t_{PHL}	HIGH to LOW propagation delay	A to B		3	6	2	5	2	5	2	5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		1	3	2	4	2.5	7	2.5	5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		3	6	2	5	2	5	2	5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		5	8	2	4	1.5	3	1	3	ns
t_{PZL}	OFF-state to LOW propagation delay	OE to A		6	12	5	10	8	10	5	8	ns
		OE to B		9	18	5	10	4.5	9	4	8	ns
t_{PLZ}	LOW to OFF-state propagation delay	OE to A		100	120	100	120	100	120	100	120	ns
		OE to B		100	120	100	120	100	120	100	120	ns
$t_{sk(o)}$	output skew time	between channels	[2]	-	1	-	1	-	1	-	1	ns
f_{data}	data rate			-	18	-	32	-	32	-	32	Mbps
$V_{CC(A)}$ = 3.3 V ± 0.3 V												
t_{PHL}	HIGH to LOW propagation delay	A to B		3	5	2	5	2	4	2	4	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		1	2	1.5	3	1.5	3	2	4	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		3	5	2	5	2	4	2	4	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		4	8	2.5	7	1.5	3	1	3	ns
t_{PZL}	OFF-state to LOW propagation delay	OE to A		6	12	4.5	9	6	9	4	7	ns
		OE to B		10	14	5	10	6	9	4	8	ns

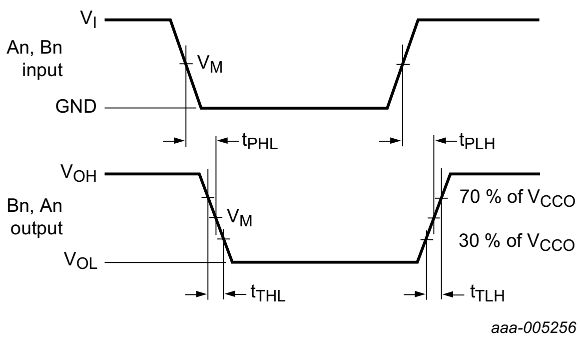
Table 10. Dynamic characteristics for temperature range –40 °C to +85 °C[1]
Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for wave forms see Figure 5 and Figure 6.

Symbol	Parameter	Conditions		$V_{CC(B)}$								Unit
				1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Typ	Max	Typ	Max	Typ	Max	Typ	Max	
t_{PLZ}	LOW to OFF-state propagation delay	OE to A		100	120	100	120	100	120	100	120	ns
		OE to B		100	120	100	120	100	120	100	120	ns
$t_{sk(o)}$	output skew time	between channels	[2]	-	1	-	1	-	1	-	1	ns
f_{data}	data rate			-	18	-	32	-	40	-	40	Mbps
$V_{CC(A)}$ = 5.0 V ± 0.5 V												
t_{PHL}	HIGH to LOW propagation delay	A to B		5	7	2	5	2	4	2	4	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		1	2	1	3	1	3	1	3	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		5	7	2	5	2	4	2	4	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		4	7	2.5	5	2	4	1	3	ns
t_{PZL}	OFF-state to LOW propagation delay	OE to A		6	14	4	8	4	8	3	5	ns
		OE to B		10	15	5	8	4	7	4	5	ns
t_{PLZ}	LOW to OFF-state propagation delay	OE to A		100	120	100	120	100	120	100	120	ns
		OE to B		100	120	100	120	100	120	100	120	ns
$t_{sk(o)}$	output skew time	between channels	[2]	-	1	-	1	-	1	-	1	ns
f_{data}	data rate			-	18	-	32	-	40	-	52	Mbps

[1] All typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.

[2] Skew between any two outputs of the same package switching in the same direction.

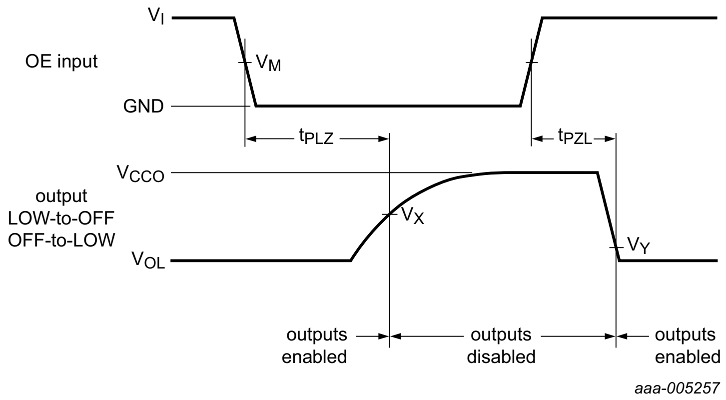
13. Waveforms



Measurement points are given in Table 11.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. The data input (An, Bn) to data output (Bn, An) propagation delay times



Measurement points are given in Table 11.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

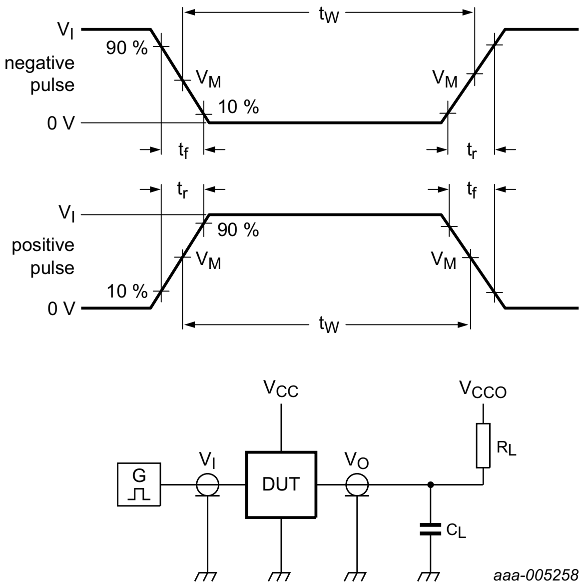
Fig 6. Enable and disable times

Table 11. Measurement points[1][2]

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.65 V to 5.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$0.5V_{CCO}$	$0.1V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 12.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ns.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{CC0} = Supply voltage associated with the output.

Fig 7. Test circuit for measuring switching times

Table 12. Test data

Supply voltage		Input		Load	
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	t_r/t_f	C_L	R_L
1.65 V to 1.95 V	1.65 V to 1.95 V	V_{CCI}	≤ 2.0 ns	50 pF	2.2 kΩ
2.3 V to 2.7 V	2.3 V to 2.7 V	V_{CCI}	≤ 2.0 ns	50 pF	2.2 kΩ
3.0 V to 3.6 V	3.0 V to 3.6 V	V_{CCI}	≤ 2.5 ns	50 pF	2.2 kΩ
4.5 V to 5.5 V	4.5 V to 5.5 V	V_{CCI}	≤ 2.5 ns	50 pF	2.2 kΩ

[1] V_{CCI} is the supply voltage associated with the input.

14. Application information

14.1 Applications

The NTSX2102 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is targeted at I^2C or 1-wire buses which use open-drain drivers.

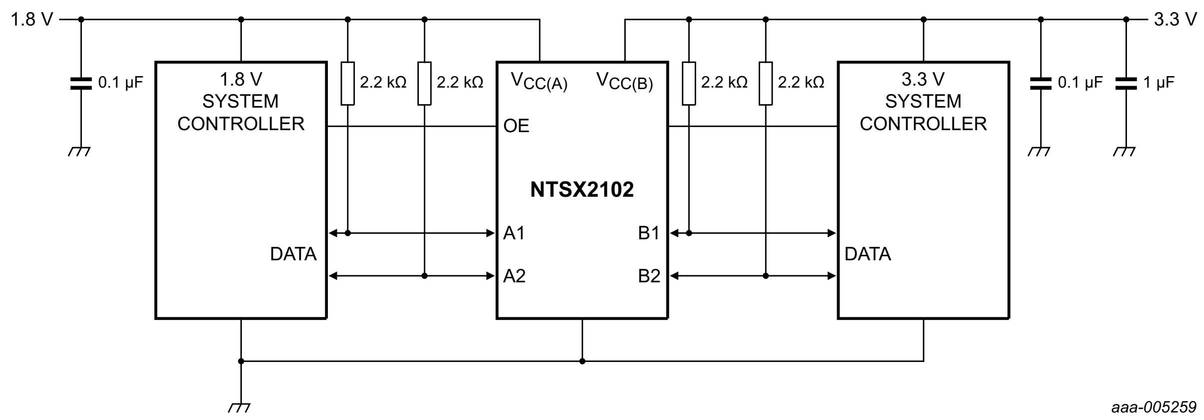


Fig 8. Typical voltage level-translation circuit

14.2 Architecture

The architecture of the NTSX2102 is shown in Figure 9. The device does not require an extra input signal to control the direction of data flow from A to B or B to A. The NTSX2102 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. Two pass-gate transistors (N-channel) that tie the ports together.
2. An output edge-rate accelerator that detects and accelerates rising and falling edges on the I/O pins (see Figure 10).

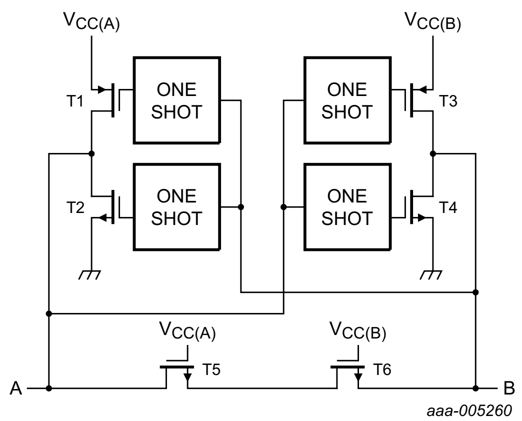
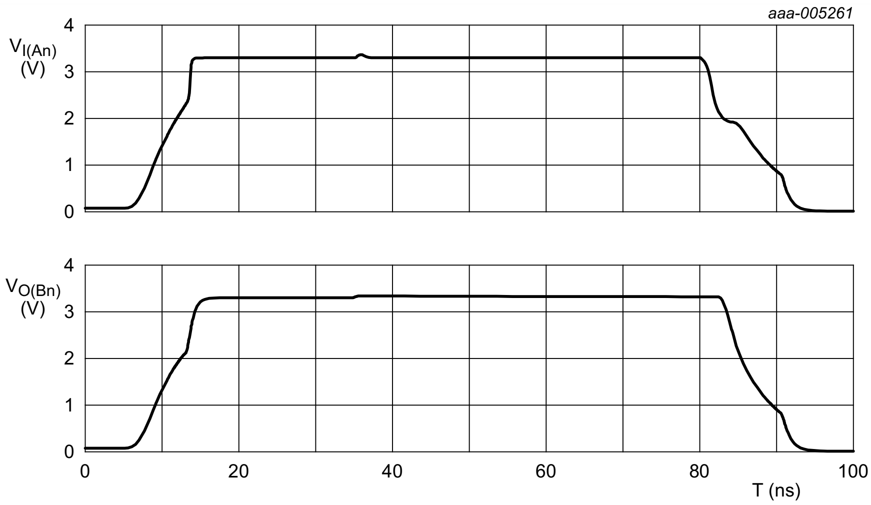


Fig 9. Architecture of NTSX2102 I/O cell (one channel)

During an input transition, a one-shot accelerates the output transition by switching on the PMOS transistors (T1, T3) for a LOW-to-HIGH transition. Alternatively, it switches on the NMOS transistors (T2, T4) for a HIGH-to-LOW transition. Once activated, the one-shot is de-activated after approximately 25 ns (see Figure 11). During the acceleration time, the driver output resistance is between approximately 10 Ω and 35 Ω. To avoid signal contention, the application must not exceed the maximum data rate or wait for the one-shot circuit to turn-off, before applying a signal in the opposite direction.



$V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V.

Fig 10. Input and output waveforms showing edge-rate acceleration

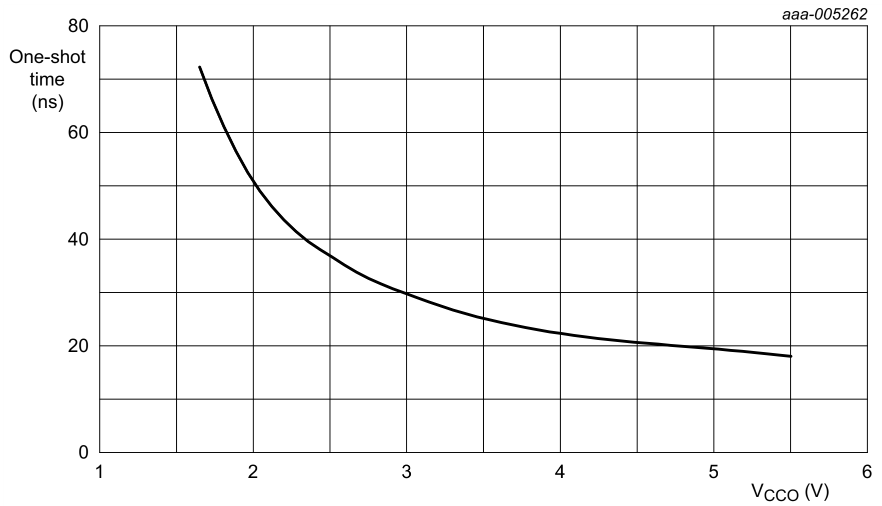


Fig 11. One-shot pulse time versus V_{CCO}

14.3 Input driver requirements

As the NTSX2102 is a switch type translator, properties of the input driver directly affect the output signal. The external open-drain driver applied to an I/O, determines the static current sinking capability of the system. The maximum data rate, output transition times (t_{THL}, t_{TLH}) and propagation delays (t_{PHL}, t_{PLH}) are dependent upon the output impedance and edge-rate of the external driver.

14.4 Output load considerations

The maximum lumped capacitive load that can be driven is dependent upon the one-shot pulse duration and has been tuned to 600 pF. In cases with higher capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration. To avoid excessive capacitive loading and to ensure correct triggering of the one-shot, use short trace lengths and low capacitance connectors on NTSX2102 PCB layouts. The length of the PCB trace should be such that the round-trip delay of any reflection is within the one-shot pulse duration. Such a length ensures low impedance termination and avoids output signal oscillations and one-shot retriggering.

14.5 Output enable (OE)

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state.

14.6 Power-up

When either of the supplies $V_{CC(n)}$ is at 0 V, outputs are in the high-impedance OFF-state. One of the advantages of NTSX translators is that either $V_{CC(A)}$ or $V_{CC(B)}$ may be powered up first. To reduce dissipation during power-up, ensure that output enable (OE) is defined. Connect it via a pull down resistor to GND or, if the application allows, hardwired to $V_{CC(A)}$. If the OE pin is hardwired to $V_{CC(A)}$, either supply can be powered up or down first. If a pull down is used, the following sequences are recommended.

For power-up:

1. Apply power to either supply pin
2. Apply power to other supply pin
3. Enable the device by driving OE HIGH

For power down:

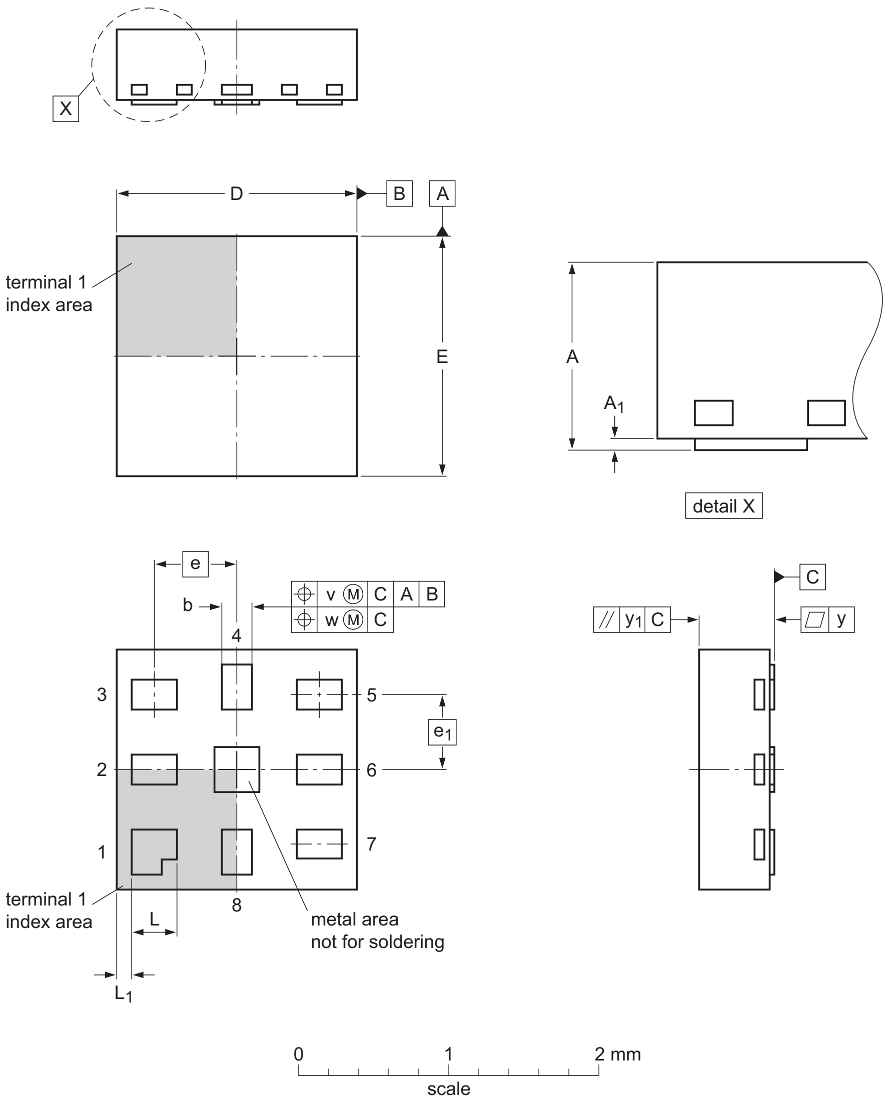
1. Disable the device by driving OE LOW
2. Remove power from either supply pin
3. Remove power from other supply pin

14.7 Pull-up resistors on I/O lines

Each A port I/O requires a pull-up resistor to $V_{CC(A)}$, and each B port I/O requires a pull-up resistor to $V_{CC(B)}$. Choose the magnitude of the pull-up resistors to ensure that the output voltage levels meet the application requirement.

15. Package outline

**XQFN8: plastic, extremely thin quad flat package; no leads;
8 terminals; body 1.6 x 1.6 x 0.5 mm** **SOT902-2**



Dimensions

Unit[1]		A	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
	max	0.5	0.05	0.25	1.65	1.65			0.35	0.15				
mm	nom			0.20	1.60	1.60	0.55	0.5	0.30	0.10	0.1	0.05	0.05	0.05
	min		0.00	0.15	1.55	1.55			0.25	0.05				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

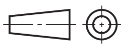
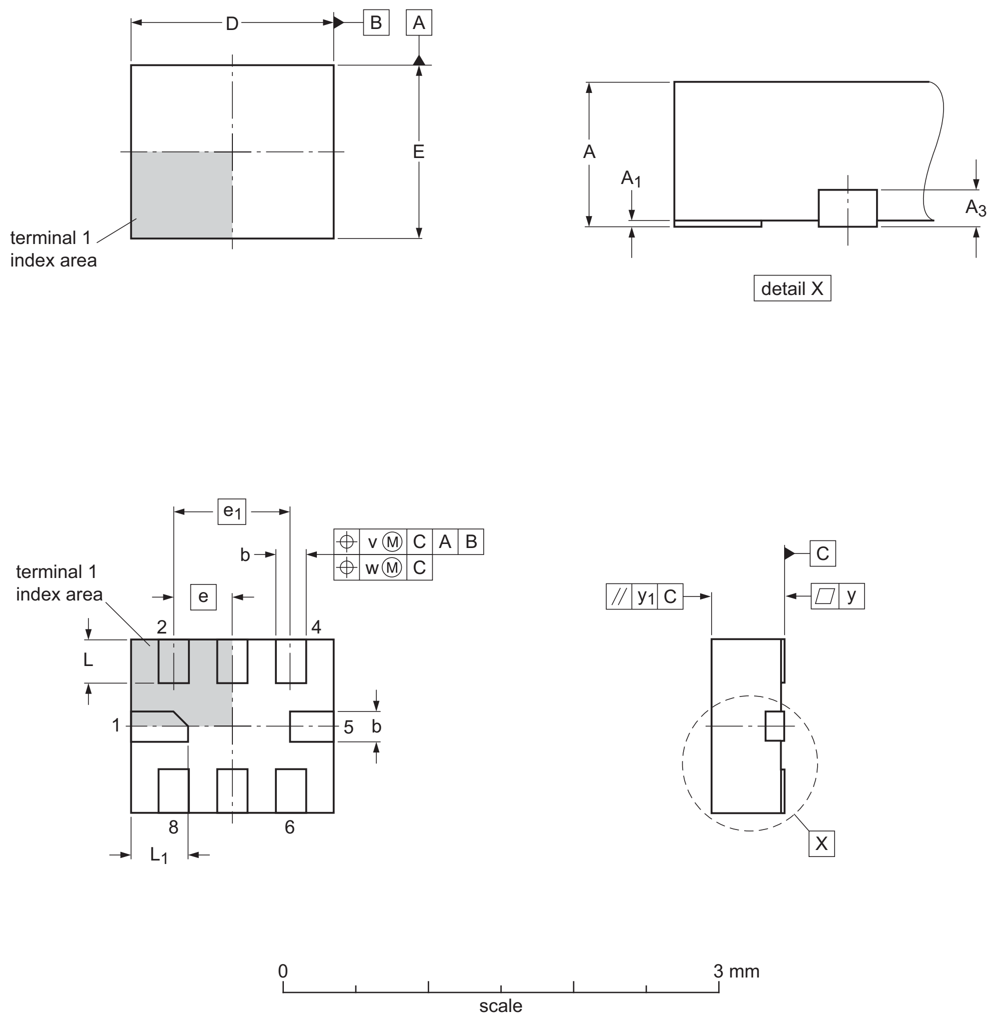
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT902-2	- - -	MO-255	- - -			~~10-11-02~~ 11-03-31

Fig 12. Package outline SOT902-2 (XQFN8)

XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.4 x 1.2 x 0.5 mm **SOT1309-1**



Dimensions

Unit		A	A_1	A_3	b	D	E	e	e_1	L	L_1	v	w	y	y_1
	max	0.50	0.025		0.25	1.45	1.25			0.35	0.45				
mm	nom			0.127	0.20	1.40	1.20	0.4	0.8	0.30	0.40	0.10	0.05	0.05	0.05
	min		0.00		0.15	1.35	1.15			0.25	0.35				

Note

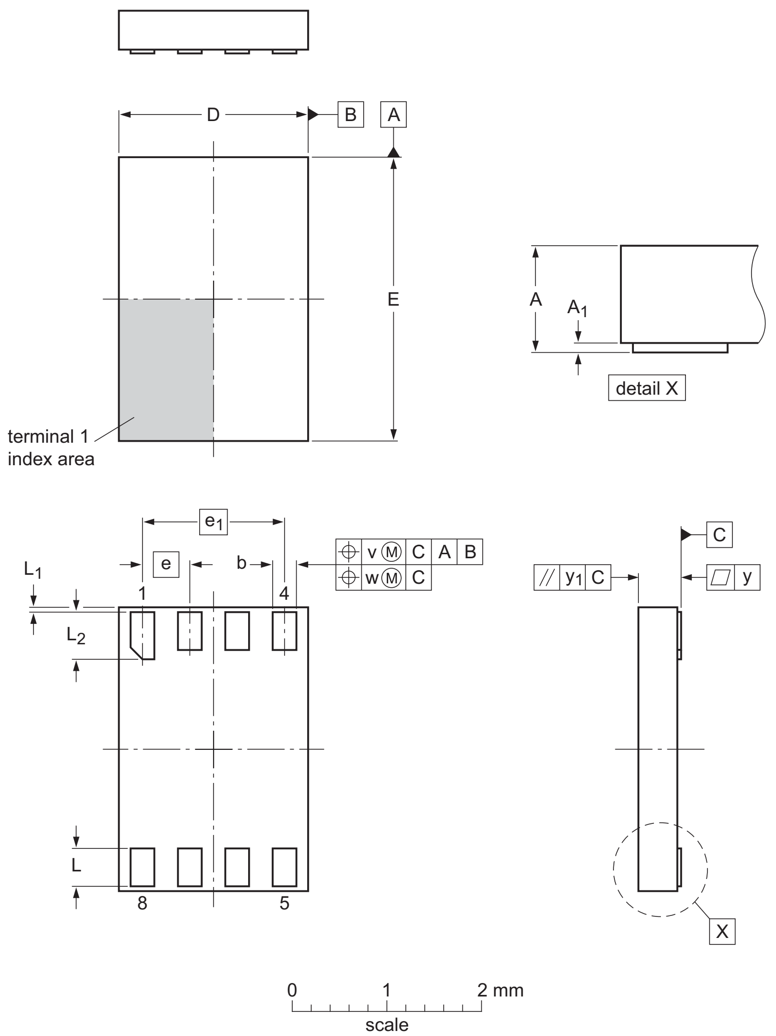
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

sot1309-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1309-1		MO-255				~~11-08-18~~ 11-08-23

Fig 13. Package outline SOT1309-1 (XQFN8)

**XSON8: plastic extremely thin small outline package; no leads;
8 terminals; body 3 x 2 x 0.5 mm** **SOT996-2**



Dimensions (mm are the original dimensions)

Unit[(1)]		A	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
mm	max		0.05	0.35	2.1	3.1			0.5	0.15	0.6				
	nom	0.5					0.5	1.5				0.1	0.05	0.05	0.1
	min		0.00	0.15	1.9	2.9			0.3	0.05	0.4				

sot996-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT996-2						~~07-12-21~~ 12-11-20

Fig 14. Package outline SOT996-2 (XSON8)

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input Output
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
PCB	Printed Circuit Board
PMOS	Positive Metal Oxide Semiconductor
SMBus	System Management Bus
UART	Universal Asynchronous Receiver Transmitter
UTLP	Ultra Thin Leadless Package

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTSX2102 v.2	20130211	Product data sheet	-	NTSX2102 v.1.1
Modifications:	• For type number NTSX2102GD XSON8U has changed to XSON8.			
NTSX2102 v.1.1	20121121	Product data sheet	-	NTSX2102 v.1
Modifications:	• Section 1 "General description" text updated.			
NTSX2102 v.1	20121119	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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