PCA9621

65 mA 8-bit 2-wire bus output port

Rev. 1 — 9 March 2011 Product data sheet

1. General description

The PCA9621 is a monolithic CMOS integrated circuit for general purpose output drive configurable from a 2-wire bus interface (including I^2C-bus, SMBus, PMBus, and other systems based on similar principles). Output ports have a 65 mA sink capability, making them ideal for driving LEDs.

The state of the outputs is determined by a programmable 8-bit register which can be read and written via signals from the 2-wire bus (e.g., I^2C-bus or similar).

The 2-wire bus interface also has 30 mA Fast-mode Plus (Fm+) capability, and consequently can be run in excess of 1 MHz or up to 4000 pF capacitance. As such, the PCA9621 can be connected to other 2-wire devices across long cable connections.

It can be mixed with other Fast-mode Plus slaves in systems driven by Fm+ buffers or by the PCA9646 (fully buffered 4-channel bus switch) to build large scale systems with high-speed or high-capacitance drive capability, for example large scale LED displays or controlled lighting.

2. Features and benefits

- 8 individually selectable open-drain output ports
- 65 mA static sink capability on all output ports
- Ports may be paralleled for up to 500 mA drive
- Ideal for simple LED or general purpose output drive
- Fast-mode Plus (30 mA, 4000 pF) 2-wire bus capability
- Works with I^2C-bus (Standard-mode, Fast-mode, and Fast-mode Plus), SMBus (standard and high power mode), and PMBus
- Fast switching times allow operation in excess of 1 MHz
- Operating voltages from 2.7 V to 5.5 V

3. Applications

- LED and 7-segment displays
- Simple high-power (500 mA) LED dimming
- General purpose output
- Instrumentation indicators

4. Ordering information

Table 1. Ordering information

T_{amb} = −40 to +85 °C.

Type number	Topside mark	Package		
		Name	Description	Version
PCA9621D	PCA9621	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
PCA9621PW	PCA9621	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Block diagram

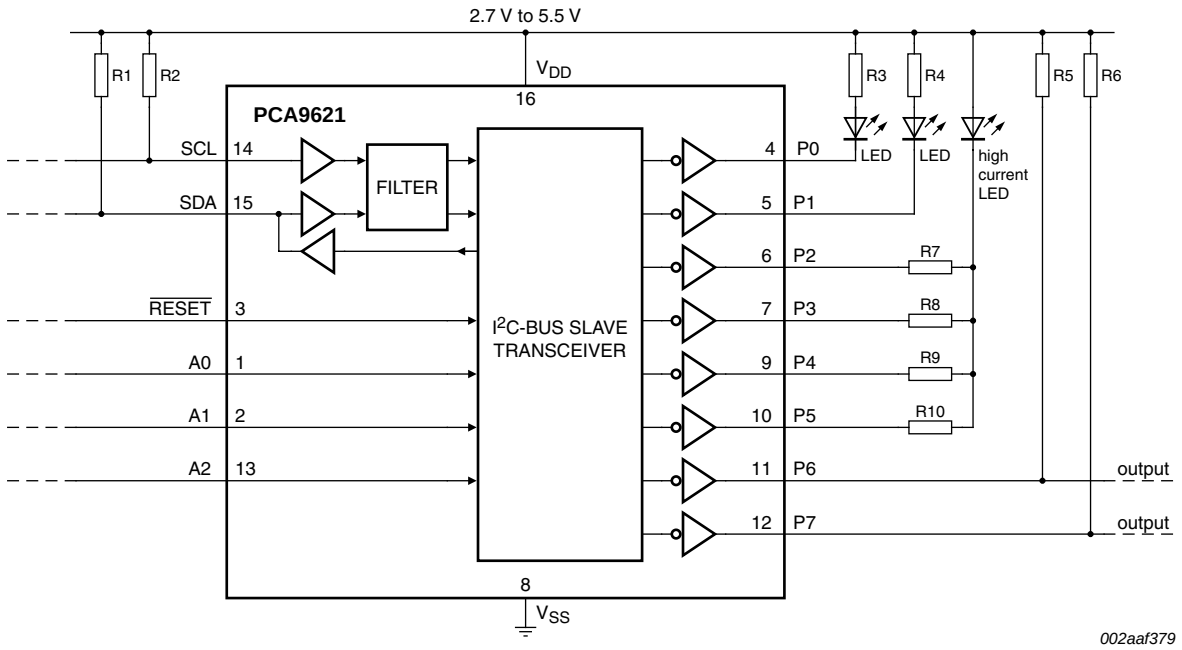


Fig 1. Block diagram of PCA9621

6. Pinning information

6.1 Pinning

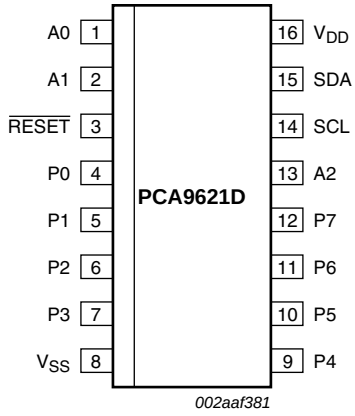


Fig 2. Pin configuration for SO16

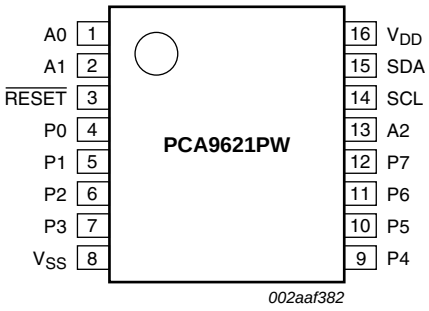


Fig 3. Pin configuration for TSSOP16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	address input 0
A1	2	address input 1
$\overline{\text{RESET}}$	3	active LOW reset input
P0	4	output port 0
P1	5	output port 1
P2	6	output port 2
P3	7	output port 3
V_{SS}	8	negative supply (ground)
P4	9	output port 4
P5	10	output port 5
P6	11	output port 6
P7	12	output port 7
A2	13	address input 2
SCL	14	serial clock line
SDA	15	serial data line
V_{DD}	16	positive supply

7. Functional description

Refer to Figure 1 “Block diagram of PCA9621”.

7.1 V_{DD}, V_{SS} — DC supply pins

The power supply voltage for the PCA9621 may be any voltage in the range 2.7 V to 5.5 V. All other I/Os are clamped to V_{DD} and V_{SS} through ESD protection diodes.

7.2 SCL, SDA — 2-wire bus interface

The state of the output ports is determined by the Control register, which is set and read via a 2-wire bus interface using I^2C-bus style signalling. The interface is Fast-mode Plus (Fm+) I^2C-bus compatible, though the ports contain ESD protection diodes to the positive and negative supplies. Consequently, $V_{I2C\text{-}bus}$ (voltage at SCL and SDA) must remain within the V_{DD} and V_{SS} supply levels.

7.3 P0 to P7 — output ports

There are eight open-drain output ports whose state is determined by the Control register. Programming a ‘1’ or HIGH to the relevant register bit will turn on the corresponding port, resulting at a LOW or ‘0’ at the port. In the case of LED driving, this would result in the LED turning ON.

Programming a ‘0’ or LOW in the register turns off the open-drain port, placing it in a high-impedance mode.

The ports are protected by ESD diodes to the supplies so they must not be driven above the V_{DD} or below the V_{SS} levels.

7.4 $\overline{\text{RESET}}$ — reset IC to default state

The active LOW $\overline{\text{RESET}}$ input is used to disable the buffer and reset it to its default state. The $\overline{\text{RESET}}$ signal will clear the contents of the Control register, turning off all output ports, and resetting the state of the I^2C-bus slave transceiver block.

7.5 Power-On Reset (POR)

During power-on, the PCA9621 is internally held in the reset condition for a maximum of t_{rst} = 500 ns. The default condition after reset is for the Control register to be erased (all zeros), resulting in all output ports being off (high-impedance).

7.6 A0, A1, A2 — address lines

The slave address of the PCA9621 is shown in Figure 4. The address pins (A2, A1, A0) must be driven to a HIGH or LOW level—they are not internally pulled to a default state.

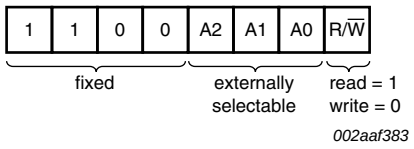
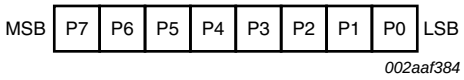


Fig 4. Slave address

The read/write bit must be set LOW to enable a write to the Control register, or HIGH to read from the Control register.

7.7 Control register

The Control register of the PCA9621 is shown in Figure 5. Each of the four output ports can be activated independently by setting the appropriate bit in the Control register.



1 = ON (sinking)

0 = OFF (high-impedance)

Fig 5. Control register

A LOW or ‘zero’ bit indicates that the respective channel (P7 to P0) is disabled (high-impedance). The default reset condition of the register is all zeros, all ports high-impedance. A HIGH or ‘one’ bit indicates the respective channel is active (sinking).

Example: Programming C1h (1100 0001b) into the Control register results in ports P0, P6 and P7 being ON (sinking) and the remaining ports being OFF (high-impedance).

8. Bus transaction

A typical I²C-bus write transaction to the PCA9621 is shown in Figure 6. During a write transaction, the output ports (P0 to P7) of the PCA9621 are updated upon receipt of the STOP condition.

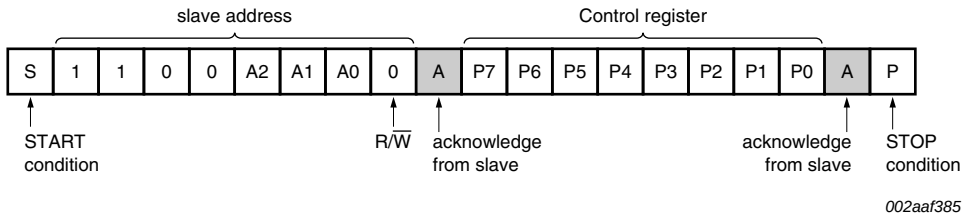


Fig 6. PCA9621 write transaction to Control register

A typical read transaction is shown in Figure 7.

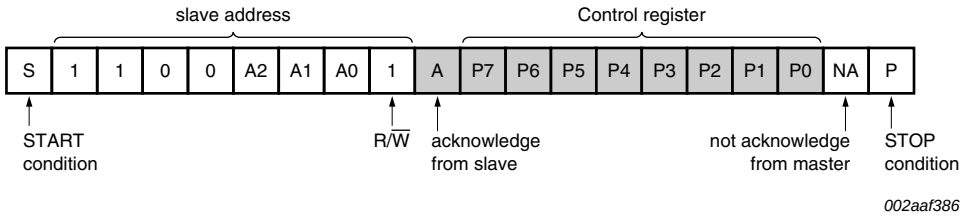


Fig 7. PCA9621 read transaction from Control register

9. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage		[1]	−0.3	+7	V
V_n	voltage on any other pin		[1]	V_{SS} − 0.5	V_{DD} + 0.5	V
I_I	input current	output ports (P0 to P7)	[2]	-	100	mA
		SDA, SCL pins		-	40	mA
		address pins A0 to A2; $\overline{\text{RESET}}$ pin		-	20	mA
I_{SS}	ground supply current			-	550	mA
P_{tot}	total power dissipation			-	300	mW
T_{stg}	storage temperature			−55	+125	°C
T_{amb}	ambient temperature	operating		−40	+85	°C

[1] Voltages are specified with respect to pin 8 (V_{SS}).

[2] 100 mA for one pin only in the group P0 to P3, and one pin only in the group P4 to P7. Otherwise 70 mA maximum, any pin.

10. Characteristics

Table 4. Characteristics

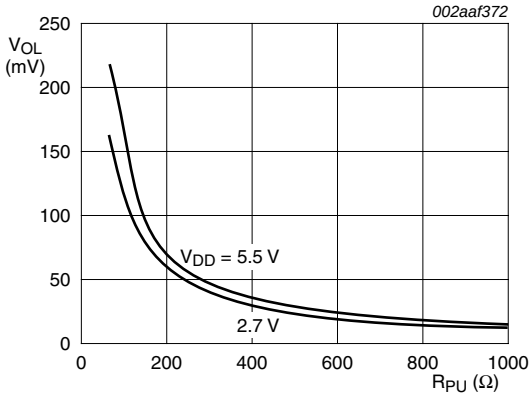
T_{amb} = −40 °C to +85 °C; voltages are specified with respect to ground (V_{SS}); V_{DD} = 5.5 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power supply							
V_{DD}	supply voltage	operating		2.7	-	5.5	V
I_{DD}	supply current	quiescent; V_I ($\overline{RESET}$ pin) = 0 V; V_{DD} = 5.5 V		-	-	1	μA
I²C-bus ports (SCL, SDA)							
$V_{I2C-bus}$	I²C-bus voltage	SDA, SCL		V_{SS} − 0.3	-	V_{DD} + 0.3	V
V_{IL}	LOW-level input voltage	V_{DD} = 2.7 V	[1]	-	-	0.4	V
		V_{DD} = 5.5 V	[1]	-	-	0.5	V
V_{IH}	HIGH-level input voltage	V_{DD} = 2.7 V	[1]	1.2	-	-	V
		V_{DD} = 5.5 V	[1]	2.0	-	-	V
I_{LI}	input leakage current	pin at V_{DD} or V_{SS}		−1	-	+1	μA
V_{OL}	LOW-level output voltage	I_{OL} = 30 mA; V_{DD} = 2.7 V		-	260	450	mV
		I_{OL} = 30 mA; V_{DD} = 5.5 V		-	140	275	mV
Open-drain output ports (P0 to P7)							
$I_{O(sink)}$	output sink current	LOW-level; port enabled		65	-	-	mA
V_{OL}	LOW-level output voltage	I_{OL} = 65 mA		-	440	725	mV
		I_{OL} = 100 μA		-	1	-	mV
$\overline{RESET}$							
V_{IH}	HIGH-level input voltage	V_{DD} = 2.7 V		2.0	-	-	V
		V_{DD} = 5.5 V		4.8	-	-	V
V_{IL}	LOW-level input voltage	V_{DD} = 2.7 V		-	-	650	mV
		V_{DD} = 5.5 V		-	-	900	mV
V_{hys}	hysteresis voltage	V_{DD} = 2.7 V		100	-	-	mV
		V_{DD} = 5.5 V		200	-	-	mV
I_{LI}	input leakage current	pin at V_{DD} or V_{SS}		−1	-	+1	μA
$t_{w(rst)L}$	LOW-level reset time	$V_I < V_{IL}$	[2]	-	25	-	ns
t_{rst}	reset time	$\overline{RESET}$ pin; from $V_I > V_{IH}$		-	250	500	ns
t_{POR}	power-on reset pulse time	$\overline{RESET}$ pin; from $V_I > V_{IH}$		-	250	500	ns
Address pins (A0, A1, A2)							
V_{IH}	HIGH-level input voltage	V_{DD} = 2.7 V		1.7	-	-	V
		V_{DD} = 5.5 V		3.5	-	-	V
V_{IL}	LOW-level input voltage	V_{DD} = 2.7 V		-	-	0.7	V
		V_{DD} = 5.5 V		-	-	1.5	V
I_{LI}	input leakage current	pin at V_{DD} or V_{SS}		−1	-	+1	μA
Timing characteristics							
t_f	fall time of both SDA and SCL signals	R_{PU} = 200 Ω; measured from 70 % V_{DD} to 30 % V_{DD}		-	16	-	ns
$t_{v(Q)}$	data output valid time		[3]	-	-	500	ns

[1] Supply voltage dependent; refer to graphs (Figure 8 through Figure 10) for typical trend.

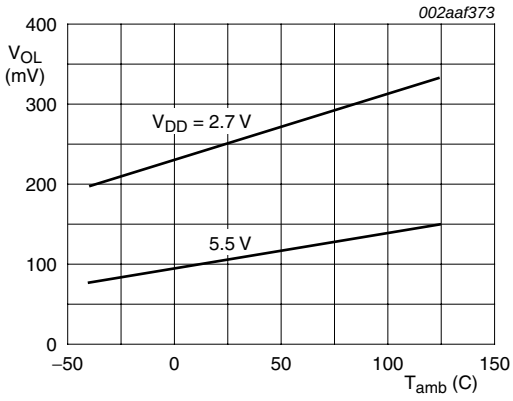
[2] Guaranteed by design, not subject to test.

[3] Time between STOP condition and output port (P0 to P7) being asserted.



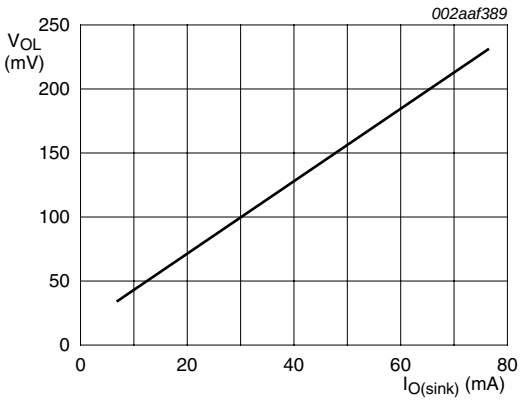
T_{amb} = 25 °C

Fig 8. Typical SDA LOW-level output voltage versus pull-up resistance



I_{OL} = 30 mA

Fig 9. Typical SDA LOW-level output voltage versus ambient temperature



T_{amb} = 25 °C; V_{DD} = 5.5 V

Fig 10. Typical output port (P0 to P7) LOW-level output voltage versus LOW-level output sink current

11. Application information

Figure 11 shows the PCA9621 in conjunction with the PCA9646 bus multiplexer in a LED drive application. Each PCA9621 can drive 8 LEDs, and using the address pins on the IC, up to 8 uniquely addressed devices can sit on one bus branch. The PCA9646 has four such outputs, giving 256 LEDs in the structure shown.

By additionally using the address pins on the PCA9646, the entire structure may be repeated 8 times, allowing 2048 LEDs to be uniquely driven. By additionally placing PCA9646's in series (refer to the PCA9646 data sheet), the structure may be further extensively multiplied into a huge array.

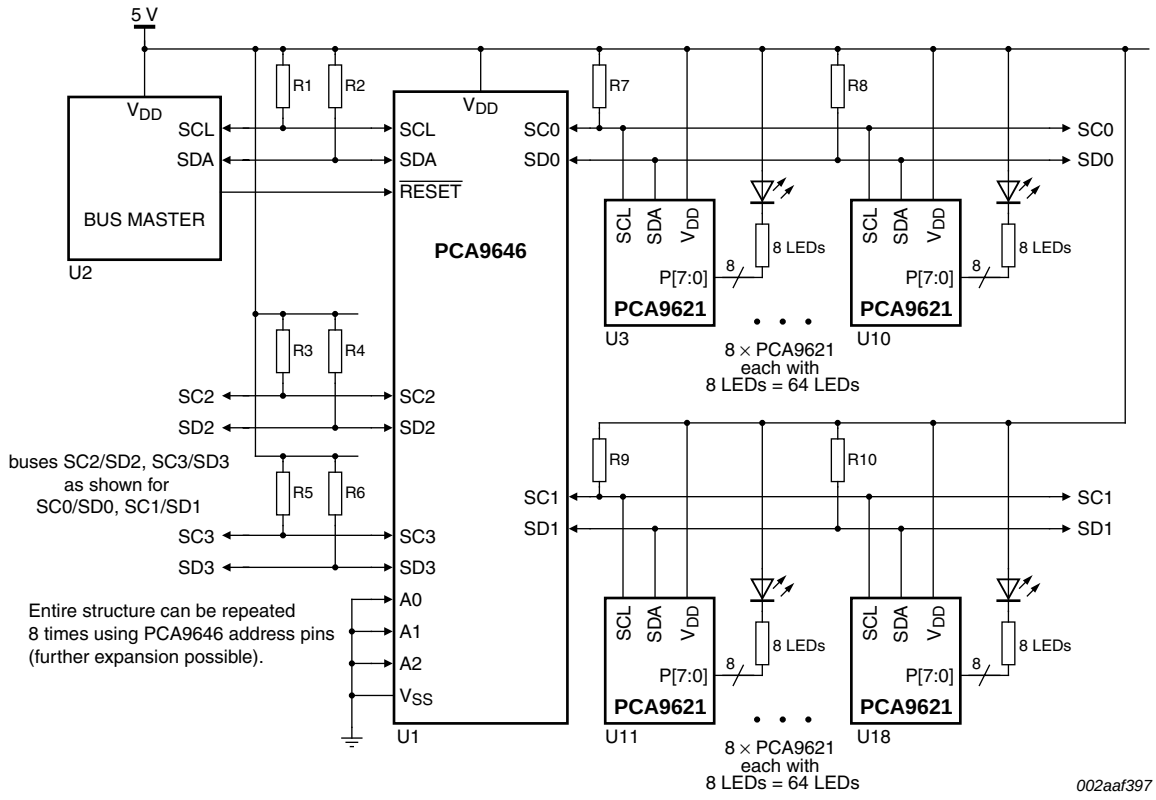


Fig 11. PCA9621 in a large LED array

Figure 12 shows a simple 7-segment display drive arrangement. All of the 7 segments plus decimal point can be driven from a single PCA9621. By using the address pins, up to 8 digits can be addressed from a single bus. When running at 1 MHz, all 8 digits can be updated in less than 0.2 ms.

Further, by using the arrangement described above and shown in Figure 11, the number of digits driven may be increased significantly.

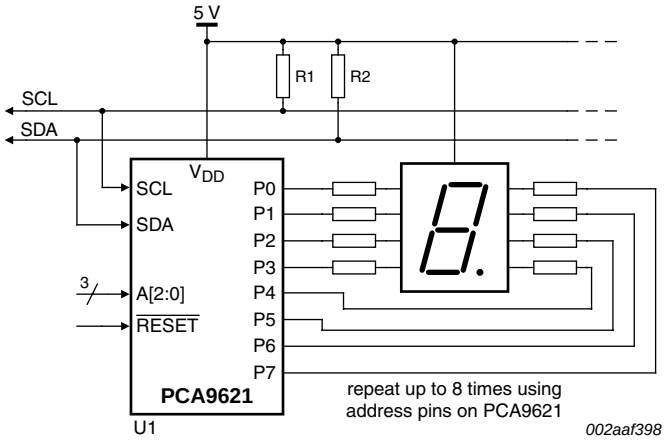
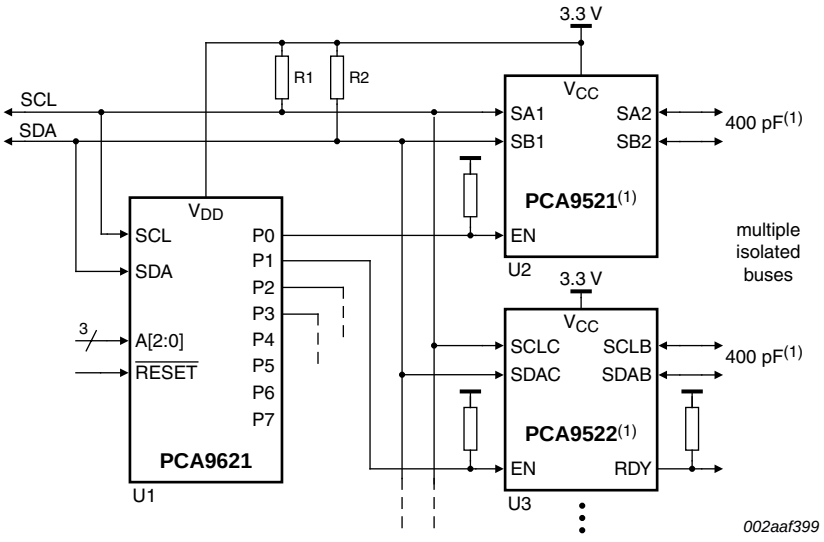


Fig 12. PCA9621 as 7-segment display driver

Figure 13 shows the PCA9621 used in conjunction with other NXP Semiconductors 2-wire bus buffers to form a multiplexer arrangement. Using the PCA9621 to control multiples of either PCA9521 or PCA9522 produces an isolating bus switch/multiplexer that has fully compliant I²C-bus I/O levels, low offset voltages, and large noise margins. Using PCA9522 in this arrangement additionally provides 'hot-swap' capability.



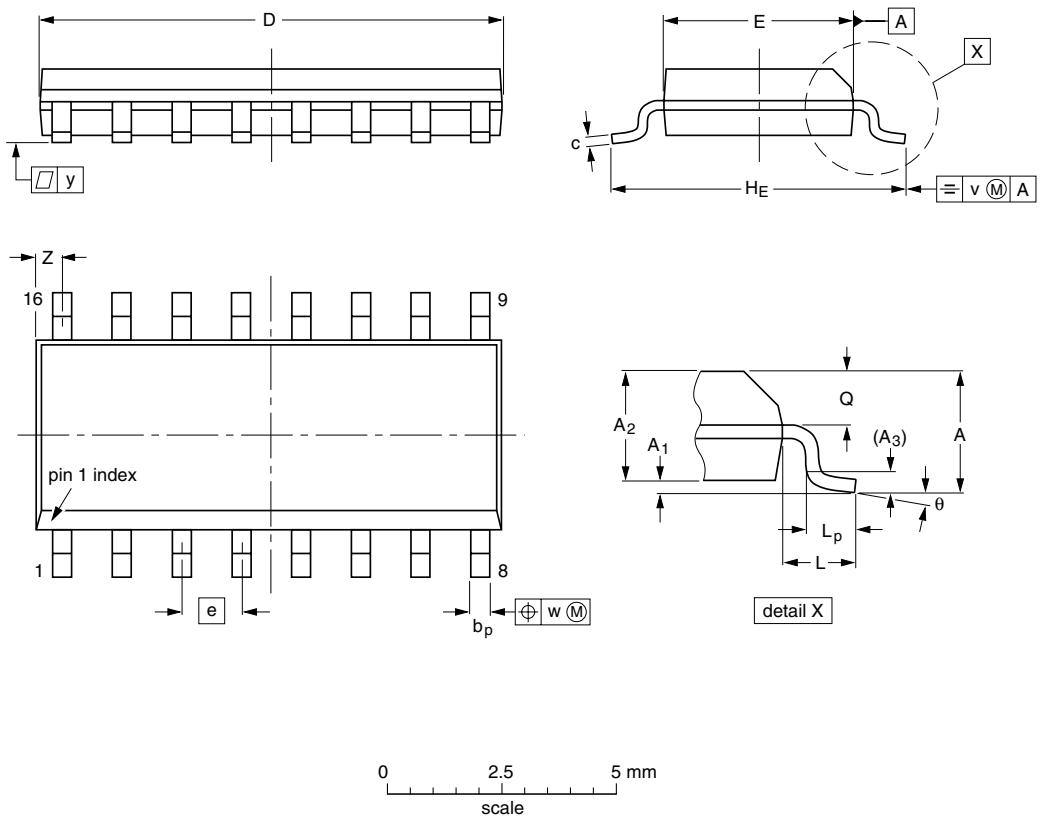
Address lines allow this structure to be repeated 8 more times.

(1) Or PCA9525 (400 pF), or PCA9605 (4000 pF), or PCA9646 (4 × 4000 pF).

Fig 13. PCA9621 as part of a fully isolating I²C-bus multiplexer

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

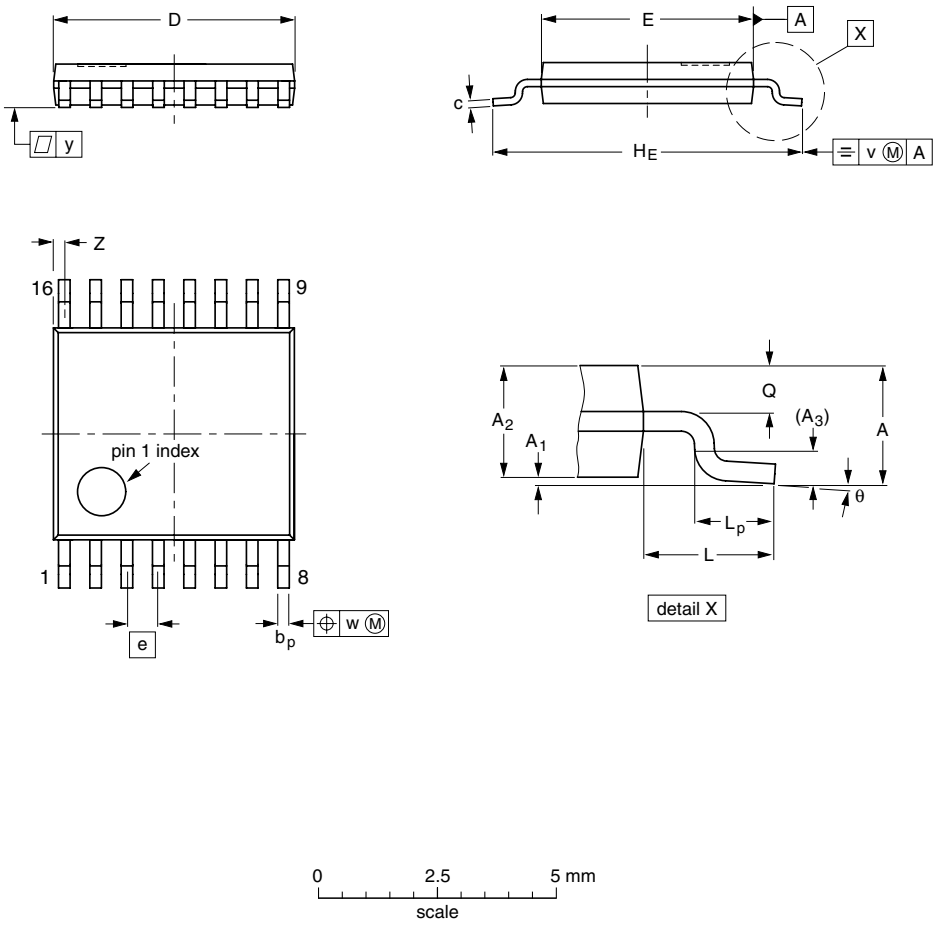
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 15. Package outline SOT403-1 (TSSOP16)

13. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 5 and 6

Table 5. SnPb eutectic process (from J-STD-020C)

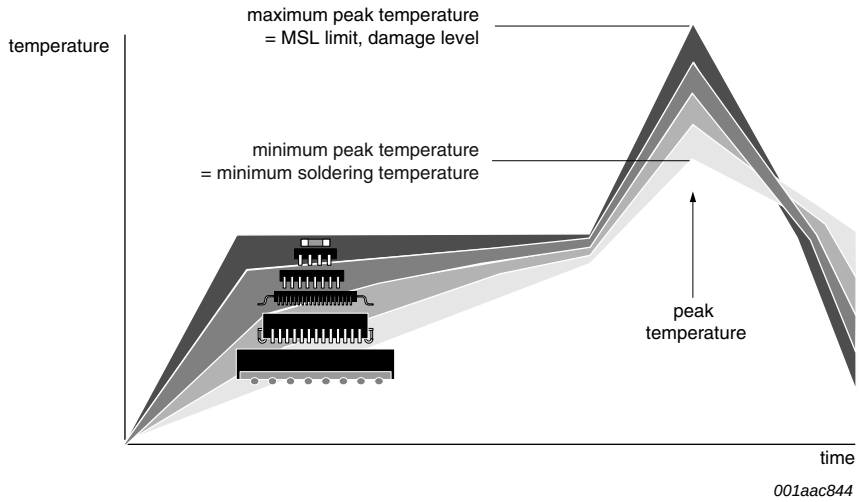
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 6. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Fig 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 7. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
IC	Integrated Circuit
LED	Light-Emitting Diode
PMBus	Power Management Bus
POR	Power-On Reset
SMBus	System Management Bus

16. References

[1] **UM10204, "I^2C-bus specification and user manual" —** NXP Semiconductors; www.nxp.com/documents/user_manual/UM10204.pdf

17. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9621 v.1	20110309	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

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19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

20. Contents

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