DATA SHEET

PCK3807A
1:10 LVTTL clock distribution device

Product data sheet
Supersedes data of 2003 Jun 27

2004 Aug 27

Philips
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1:10 LVTTL clock distribution device PCK3807A

DESCRIPTION

This low skew clock driver offers 1:10 fan-out. The large fan out from a single input reduces loading on the preceding driver and provides an efficient clock distribution network. The PCK3807A offers low capacitance inputs with hysteresis for improved noise margins. Multiple power and grounds reduce noise. Typical applications are clock and signal distribution.

The PCK3807A operates from a single 2.5 V or 3.3 V supply voltage and over the full industrial temperature range of –40 °C to +85 °C.

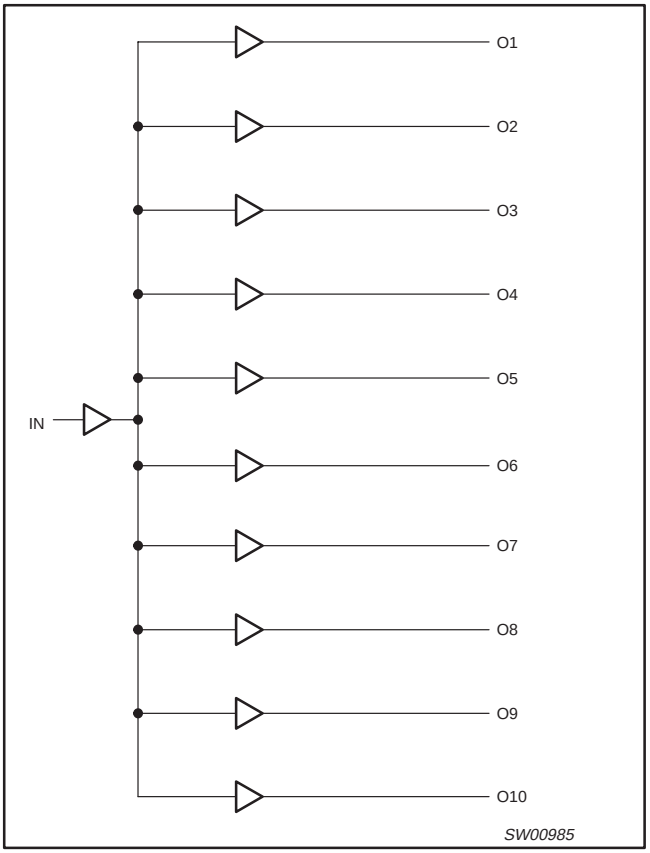
FEATURES

- Low output skew < 120 ps (max)
- Very low duty cycle distortion < 200 ps (max) for V_{CC} = 2.5 V
- High speed: propagation delay < 3.5 ns (max)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- 1:10 fanout
- Maximum output rise and fall times < 1.5 ns
- Low input capacitance: 2.5 pF typical
- V_{CC} = 2.3 V to 3.6 V
- Overvoltage tolerance on inputs
- Available in SSOP, TSSOP, SO and QSOP packages
- >150 MHz operation

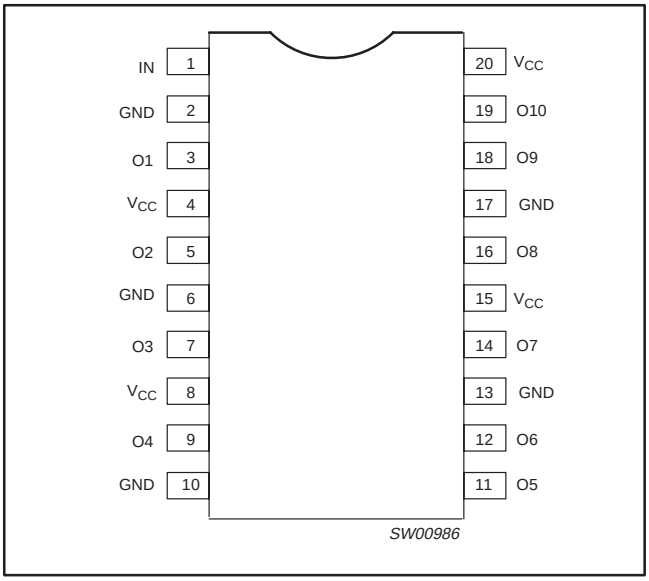
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin Plastic SO	–40 °C to +85 °C	PCK3807AD	SOT163-1
20-Pin Plastic SSOP	–40 °C to +85 °C	PCK3807ADB	SOT339-1
20-Pin Plastic TSSOP	–40 °C to +85 °C	PCK3807APW	SOT360-1
20-Pin Plastic SSOP (QSOP)	–40 °C to +85 °C	PCK3807ADS	SOT724-1

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Symbol	Pin	Description
IN	1	Clock input
O1 to O10	3, 5, 7, 9, 11, 12, 14, 16, 18, 19	Clock outputs
GND	2, 10, 13, 17	Ground
V_{CC}	20	Supply voltage

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
V_{TERM}[2]	Terminal voltage with respect to GND	–0.5	+4.6	V
V_{TERM}[3]	Terminal voltage with respect to GND	–0.5	+7	V
V_{TERM}[4]	Terminal voltage with respect to GND	–0.5	V_{CC} +0.5	V
T_{stg}	Storage temperature	–65	+150	°C
I_O	DC output current	–60	+60	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminal.
4. Outputs terminals.

CAPACITANCE

T_{amb} = +25 °C, f = 1.0 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNIT
C_i	Input capacitance	V_{IN} = 0 V	2.5	4	pF
C_o	Output capacitance	V_{OUT} = 0 V	5.5	6	pF

NOTE:
1. This parameter is measured at characterization but not tested.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.3	3.6	V
f_{IN}	Input signal frequency	0	150	MHz
T_{amb}	Operating free-air temperature range	–40	+85	°C
C_L	Output capacitance load	–	50	pF

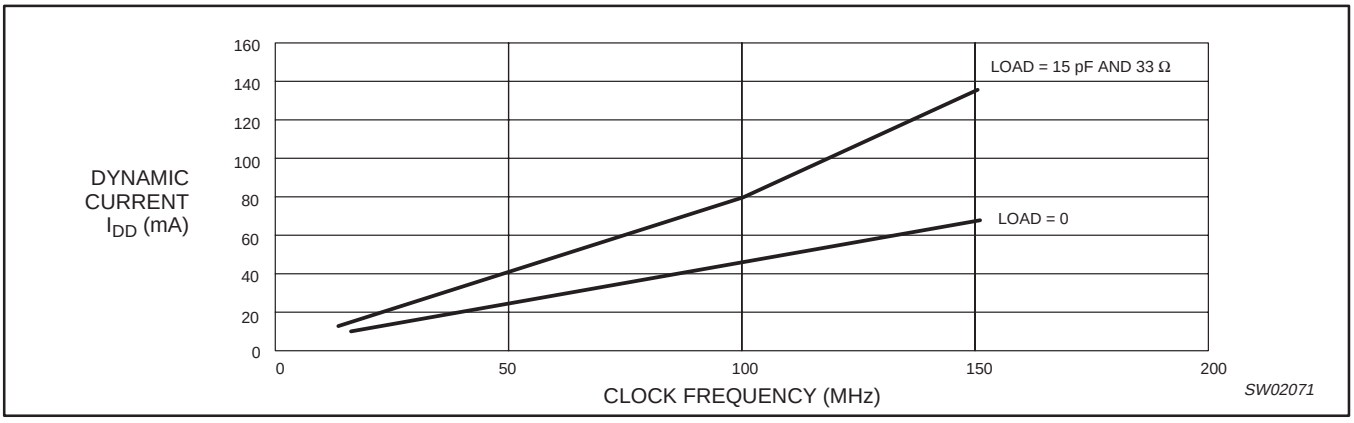


Figure 1. Dynamic current vs. clock frequency, V_{CC} = 3.3 V

POWER SUPPLY CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
ΔI_{CC}	Quiescent power supply current, TTL inputs HIGH	V_{CC} = max; V_{IN} = V_{CC} – 0.6 V		–	3	30	μA
I_{CCD}	Dynamic power supply current	V_{CC} = 2.7 V Input toggling 50% duty cycle V_{IN} = V_{CC} or GND	Outputs open	–	0.31	0.45	mA/MHz
			15 pF and 33 Ω load	–	1.0	–	
		V_{CC} = 3.6 V	Outputs open	–	0.5	0.75	
			15 pF and 33 Ω load	–	1.5	–	
I_C	Total power supply current Dynamic power supply current	V_{CC} = 2.7 V Input toggling 50% duty cycle Outputs open	V_{IN} = V_{CC} V_{IN} = GND f_i = 50 MHz	–	15.5	22.8	mA
			V_{IN} = V_{CC} V_{IN} = GND f_i = 150 MHz	–	50	75	
		V_{CC} = 3.6 V	f_i = 50 MHz	–	25	37	
			f_i = 150 MHz	–	75	115	

NOTES:
1. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3 V, +25°C ambient.
3. Per TTL driven input (V_{IN} = V_{CC} – 0.6 V).
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Ic formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (fi)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔIcc = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} – 0.6 V)
   DH = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Input Frequency
   All currents are in milliamps and all frequencies are in MHz

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

T_{amb} = –40 °C to +85 °C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IH}	HIGH-level input voltage (Input pins)	V_{CC} = 3.0 V to 3.6 V		2	–	5.5	V
	HIGH-level input voltage (I/O pins)	V_{CC} = 2.3 V to 2.7 V		1.7	–	3.6	
V_{IL}	LOW-level input voltage (Input pins)	V_{CC} = 3.0 V to 3.6 V		–0.5	–	0.8	V
	LOW-level input voltage (I/O pins)	V_{CC} = 2.3 V to 2.7 V		–0.5	–	0.7	
I_{IH}	HIGH-level input current (Input pins)	V_{CC} = Max	V_I = 5.5 V	–	–	± 1	µA
	HIGH-level input current (I/O pins)		V_I = V_{CC}	–	–	± 1	
I_{IL}	LOW-level input current (Input pins)	V_{CC} = Max	V_I = GND	–	–	± 1	µA
	LOW-level input current (I/O pins)		V_I = GND	–	–	± 1	
V_{IK}	Clamp diode voltage	V_{CC} = Min; I_{IN} = –18 mA		–	–0.7	–1.0	V
I_{ODH}	HIGH-level input current	V_{CC} = 3.3 V; V_{IN} = V_{IH} or V_{IL}; Vo =1.5 V[3]		–36	–120	–150	mA
I_{ODL}	LOW-level input current	V_{CC} = 3.3 V; V_{IN} = V_{IH} or V_{IL}; Vo =1.5 V[3]		50	150	200	mA
V_{OH}	HIGH-level output voltage	V_{CC} = 2.3 V to 3.6 V	I_{OH} = –0.1 mA	V_{CC} – 0.2	–	–	V
		V_{CC} = 2.3 V	I_{OH} = –8 mA	1.9	–	–	
		V_{CC} = 3.0 V	I_{OH} = –8 mA	2.4[6]	3	–	
V_{OL}	LOW-level output voltage	V_{CC} = 2.3 V to 3.6 V	I_{OL} = 0.1 mA	–	–	0.2	V
		V_{CC} = 2.3 V	I_{OL} = 8 mA	–	–	0.3	
		V_{CC} = 3.0 V	I_{OL} = 16 mA	–	0.2	0.4	
		V_{CC} = 3.0 V	I_{OL} = 24 mA	–	0.3	0.5	
I_{OFF}	Input power off leakage	V_{CC} = 0 V; V_{IN} = 4.5 V		–	–	± 1	µA
I_{OS}	Short circuit current[5]	V_{CC} = Max; V_O = GND[4]		0	–155	–240	mA
V_{hys}	Input hysteresis	–		–	150	–	mV
I_{CCL} I_{CCH}	Quiescent power supply current	V_{CC}= Max V_{IN} = GND or V_{CC}		–	0.1	10	µA

NOTES:

1. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3 V, +25 °C ambient.
3. Duration of the test should not exceed one second.
4. Not more than one output shorted at one time. Duration of the test should not exceed one second.
5. This parameter is guaranteed but not tested.
6. V_{OH} = V_{CC} – 0.6 V at rated current.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – INDUSTRIAL[3,4]

T_{amb} = –40 °C to +85 °C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS[1]	2.5 V ± 0.2 V		3.3 V ± 0.3 V		UNIT
			MIN[2]	MAX	MIN[2]	MAX	
t_{PLH} t_{PHL}	Propagation delay	50 Ω to V_{CC}/2; C_L = 10 pF (See Figure 2) or 50 Ω AC termination; C_L = 10 pF (See Figure 3); f ≤ 150 MHz; Outputs connected in groups of two	1.5	2.7	1.3	2.5	ns
t_R	Output rise time		–	1.0	–	1.0	ns
t_F	Output fall time		–	1.0		1.0	ns
$t_{SK(o)}$	Output skew: skew between outputs of same package (same transition)		–	0.12	–	0.12	ns
$t_{SK(p)}$	Pulse skew: skew between opposite transitions of same output ($\lvert t_{PHL} – t_{PLH} \rvert$)		–	0.3	–	0.45	ns
$t_{SK(t)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		–	0.6	–	0.6	ns
t_{PLH} t_{PHL}	Propagation delay	50 Ω to V_{CC}/2; C_L = 22 pF (See Figure 2) or 50 Ω AC termination; C_L = 22 pF (See Figure 3); f ≤ 150 MHz; Outputs connected in groups of two	1.5	3.5	1.5	3	ns
t_R	Output rise time		–	1.0	–	1.0	ns
t_F	Output fall time		–	1.0	–	1.0	ns
$t_{SK(o)}$	Output skew: skew between outputs of same package (same transition)		–	0.12	–	0.12	ns
$t_{SK(p)}$	Pulse skew: skew between opposite transitions of same output ($\lvert t_{PHL} – t_{PLH} \rvert$)		–	0.3	–	0.45	ns
$t_{SK(t)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		–	0.6	–	0.6	ns
t_{PLH} t_{PHL}	Propagation delay	C_L = 30 pF; f ≤ 67 MHz (See Figure 4)	1.5	4.0	1.5	4	ns
t_R	Output rise time		–	1.0	–	1.0	ns
t_F	Output fall time		–	1.0	–	1.0	ns
$t_{SK(o)}$	Output skew: skew between outputs of same package (same transition)		–	0.35	–	0.35	ns
$t_{SK(p)}$	Pulse skew: skew between opposite transitions of same output ($\lvert t_{PHL} – t_{PLH} \rvert$)		–	0.35	–	0.35	ns
$t_{SK(t)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		–	1.0	–	0.75	ns
t_{jitter}	RMS jitter		–	1.0	–	1.0	ps
f_{MAX}	Maximum output frequency	Functional to 400 MHz	–	400	–	400	MHz
t_{PLH} t_{PHL}	Propagation delay	C_L = 50 pF; f ≤ 40 MHz (See Figure 5)	1.5	4.5	1.5	4.0	ns
t_R	Output rise time		–	1.5	–	1.5	ns
t_F	Output fall time		–	1.5	–	1.5	ns
$t_{SK(o)}$	Output skew: skew between outputs of same package (same transition)		–	0.35	–	0.35	ns
$t_{SK(P)}$	Pulse skew: skew between opposite transitions of same output ($\lvert t_{PHL} – t_{PLH} \rvert$)		–	0.75	–	0.75	ns
$t_{SK(T)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		–	1	–	0.75	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, $t_{SK(t)}$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min and Max limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS

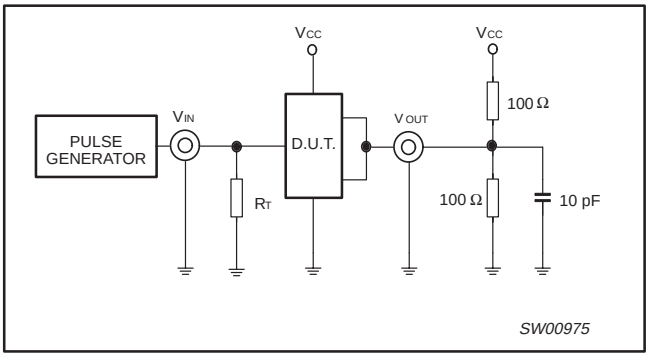
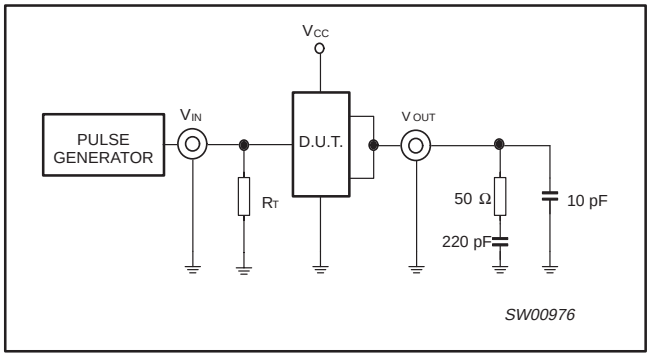


Figure 2. Z_O = 50 Ω TO $V_{CC}/2$, C_L = 10 pF



The capacitor value for ac termination is determined by the operating frequency. For very low frequencies a higher capacitor value should be selected.

Figure 3. Z_O = 50 Ω AC termination, C_L = 10 pF

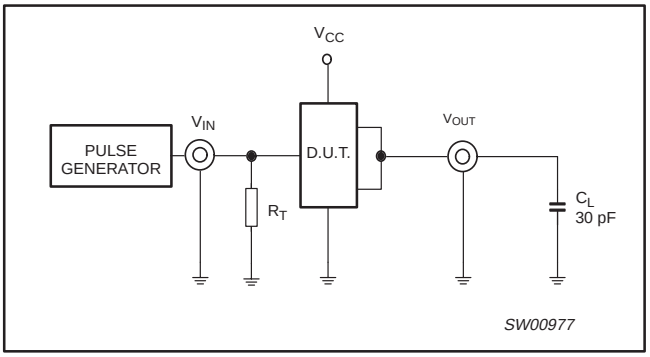


Figure 4. C_L = 30 pF circuit

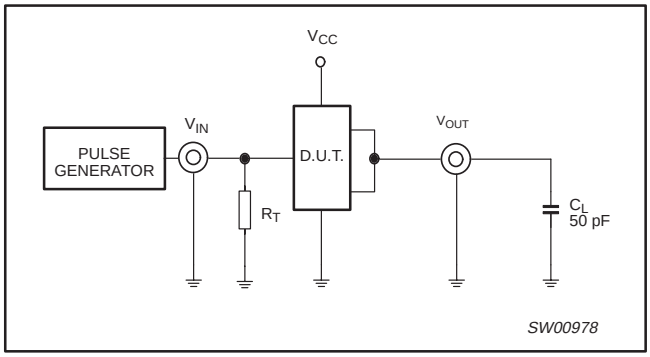


Figure 5. C_L = 50 pF circuit

TIMING DIAGRAMS

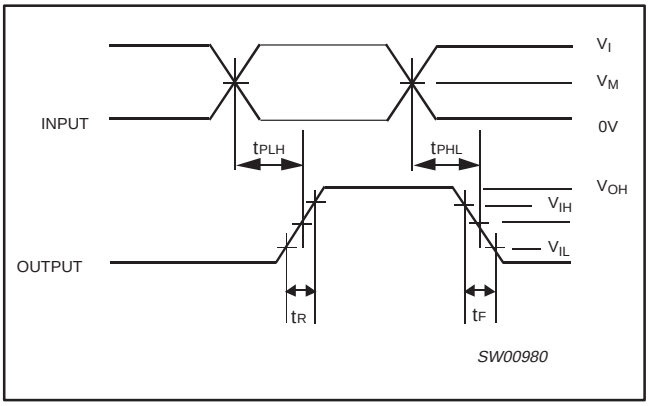


Figure 6. Package delay (see Table 1)

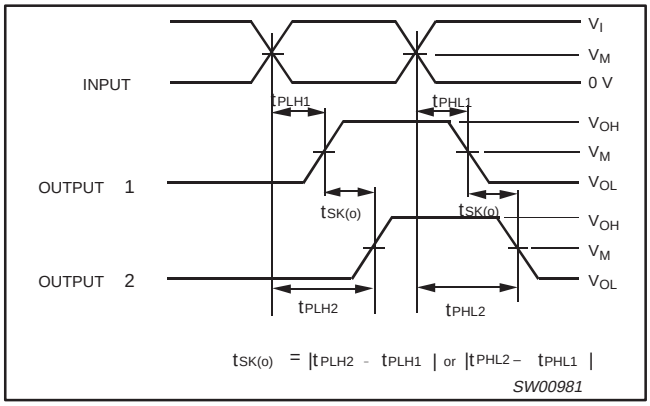


Figure 7. Output skew – $t_{SK(O)}$ (see Table 1)

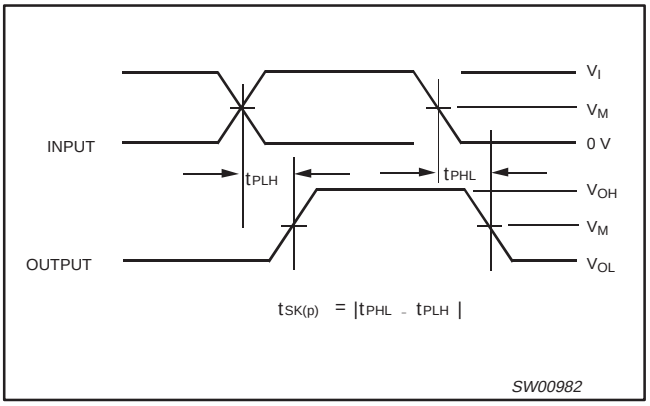


Figure 8. Pulse skew – $t_{SK(p)}$ (see Table 1)

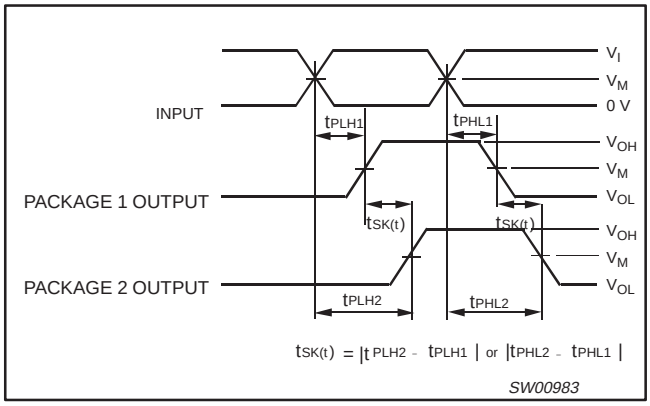
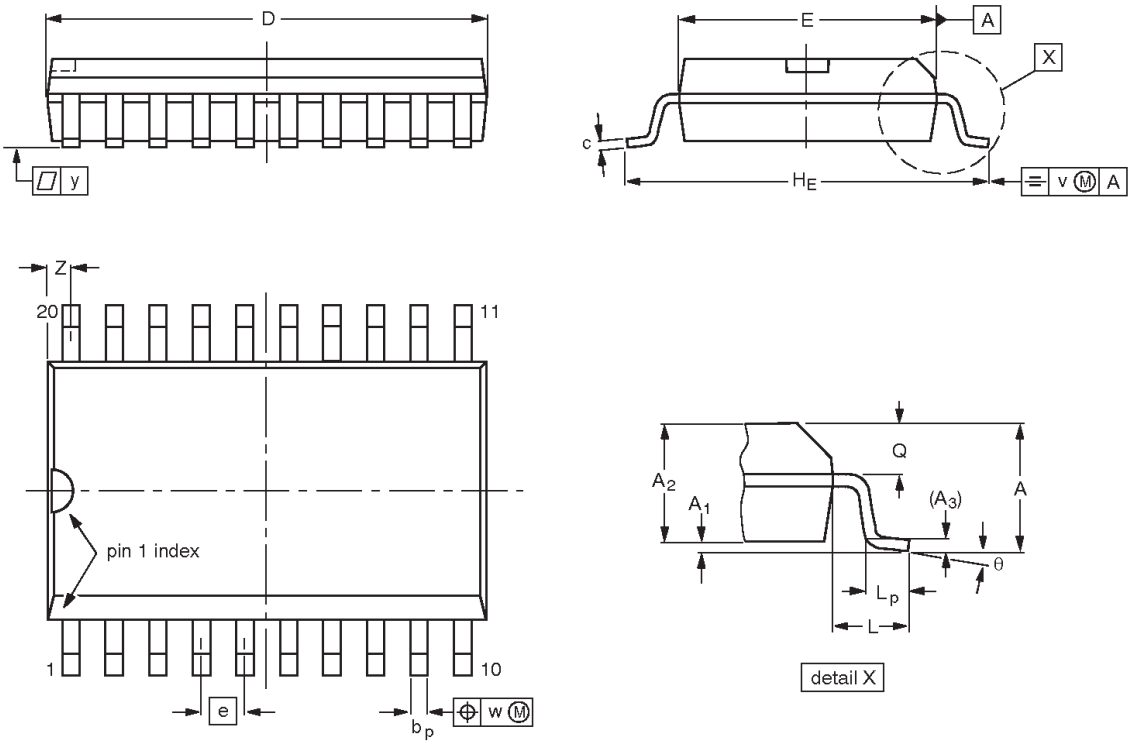


Figure 9. Package skew – $t_{SK(y)}$ (see Table 1)

Table 1. Reference levels

Reference level	V_I	V_M
For V_{CC} = 3.3 ± 0.3 V	3.0 V	1.5 V
For V_{CC} = 2.5 ± 0.2 V	V_{CC}	V_{CC}/2

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

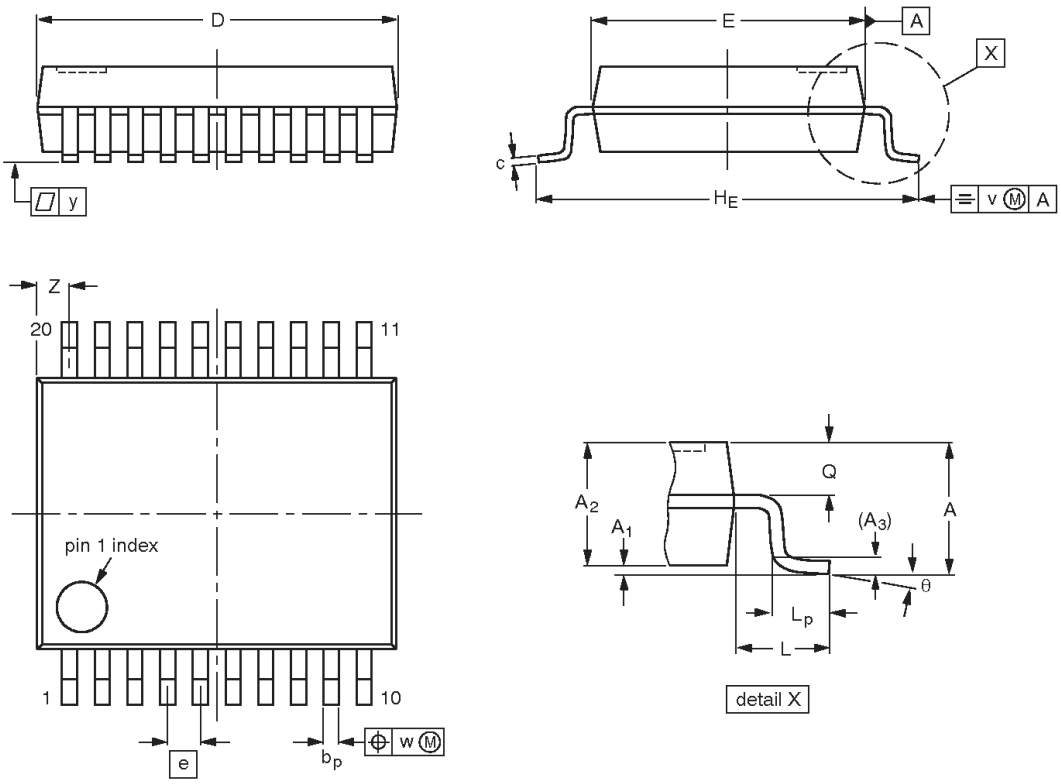
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

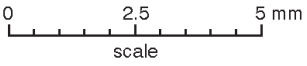
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**





DIMENSIONS (mm are the original dimensions)

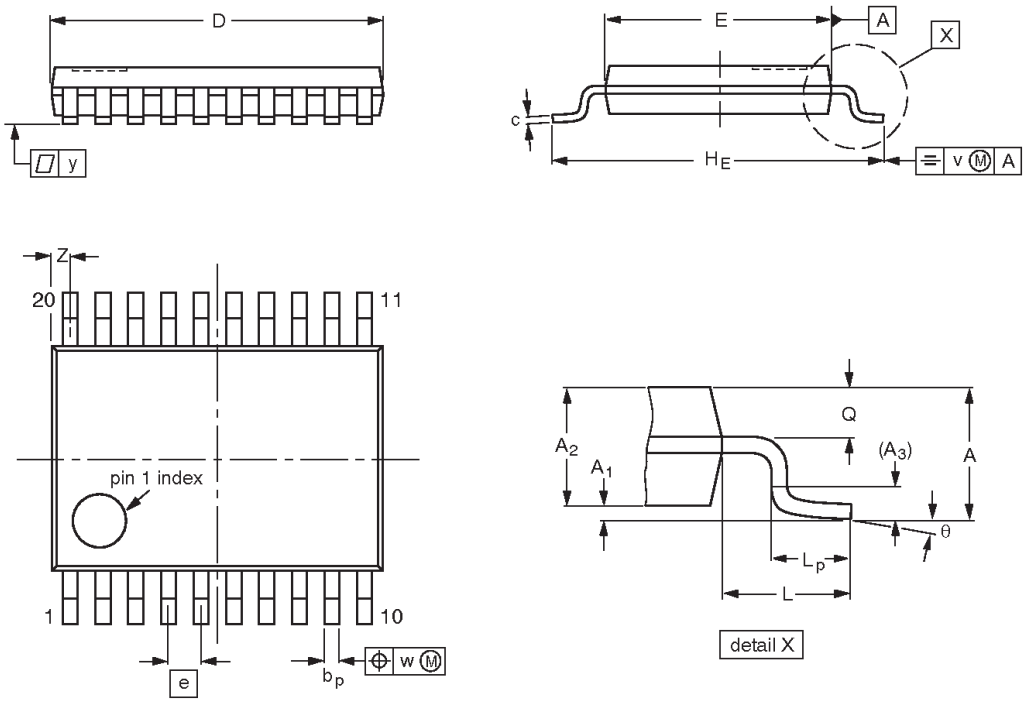
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

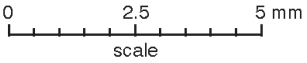
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

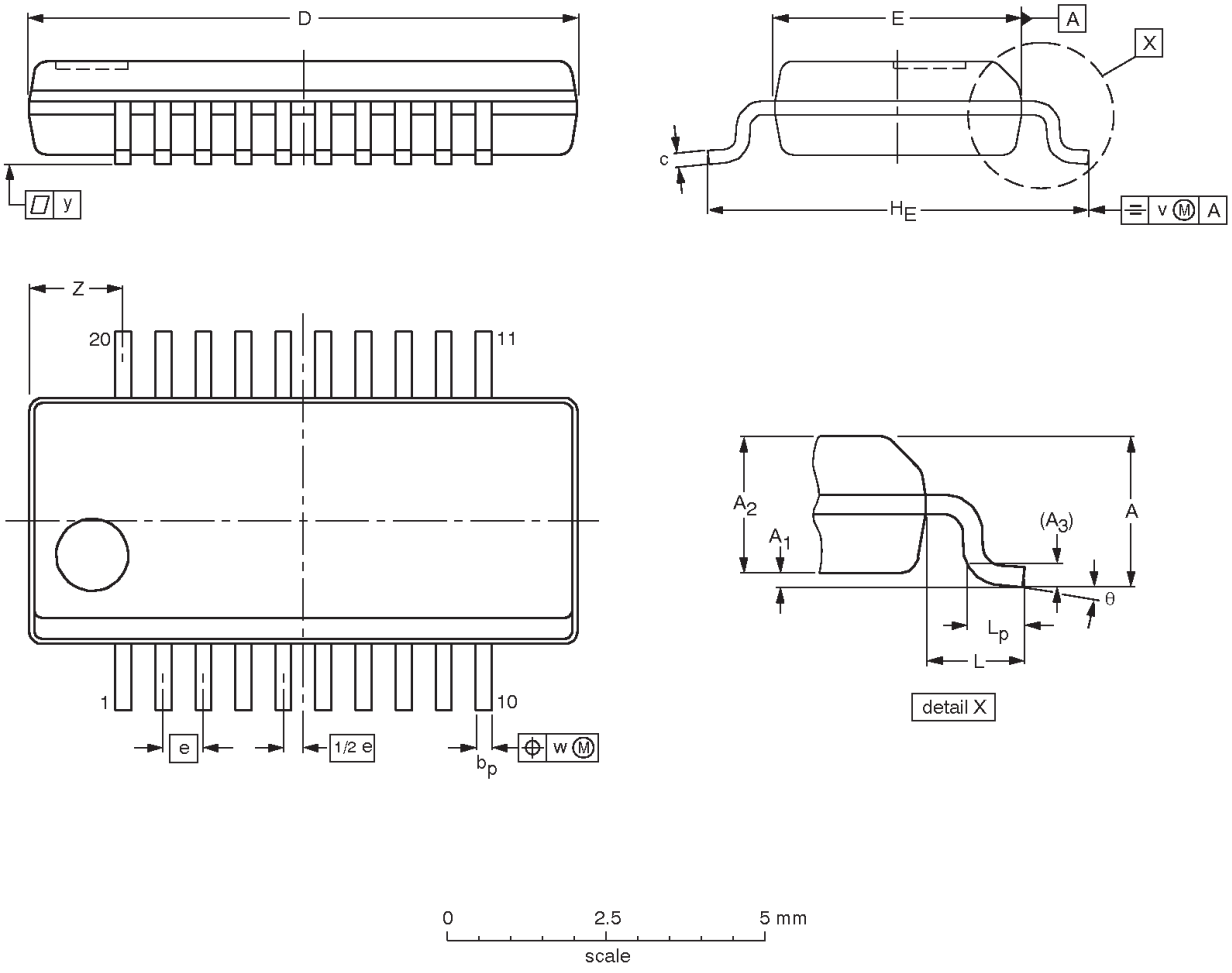
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

SSOP20: plastic shrink small outline package; 20 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT724-1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	8.8 8.6	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.25	0.18	0.1	1.67 1.28	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT724-1		MO-137				~~01-07-04~~ 03-02-18

REVISION HISTORY

Rev	Date	Description
_2	20040827	**Product data sheet (9397 750 14007). Supersedes data of 2003 Jun 27 (9397 750 11683).** Modifications: • Recommended Operating Conditions table on page 3: change V_{CC} Min. limit from 2.5 V to 2.3 V.
_1	20030627	**Product data (9397 750 11683); ECN 853-2431 30019 dated 18 June 2003. Initial version**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Definitions

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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