PCU9956A

24-channel UFm 5 MHz I²C-bus 57 mA/20 V constant current LED driver

Rev. 2 — 29 June 2015 Product data sheet

1. General description

The PCU9956A is an Ultra Fast-mode (UFm) I²C-bus controlled 24-channel constant current LED driver optimized for dimming and blinking 57 mA Red/Green/Blue/Amber (RGBA) LEDs in amusement products. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 31.25 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 122 Hz and an adjustable frequency between 15 Hz to once every 16.8 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCU9956A operates with a supply voltage range of 3 V to 5.5 V and the constant current sink LED outputs allow up to 20 V for the LED supply. The output peak current is adjustable with an 8-bit linear DAC from 225 μA to 57 mA.

A thermal shutdown feature protects the device when internal junction temperature exceeds the limit allowed for the process.

The PCU9956A device is the first LED controller device in a new Ultra Fast-mode (UFm) I²C-bus family. UFm I²C-bus devices offer higher frequency (up to 5 MHz). the UFm I²C-bus slave devices operate in receive-only mode. That is, only I²C writes to PCU9956A are supported. As such, there are no status registers in PCU9956A. The PCU9956A allows significantly higher data transfer rate compared to the Fast-mode Plus version (PCA9956A).

The active LOW output enable input pin ($\overline{OE}$) blinks all the LED outputs and can be used to externally PWM the outputs, which is useful when multiple devices need to be dimmed or blinked together without using software control.

Software programmable LED Group and three Sub Call I²C-bus addresses allow all or defined groups of PCU9956A devices to respond to a common I²C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I²C-bus commands. On power-up, PCU9956A will have a unique Sub Call address to identify it as a 24-channel LED driver. This allows mixing of devices with different channel widths. Three hardware address pins on PCU9956A allow up to 125 devices on the same bus.

The Software Reset (SWRST) function allows the master to perform a reset of the PCU9956A through the I²C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the output current switches to be OFF (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

2. Features and benefits

- 24 LED drivers. Each output programmable at:
  - Off
  - On
  - Programmable LED brightness
  - Programmable group dimming/blinking mixed with individual LED brightness
  - Programmable LED output delay to reduce EMI and surge currents
- 24 constant current output channels can sink up to 57 mA, tolerate up to 20 V when OFF
- Output current adjusted through an external resistor (REXT input)
- Output current accuracy
  - ±4 % between output channels
  - ±6 % between PCU9956A devices
- Thermal shut-down for overtemperature
- 5 MHz Ultra Fast-mode I²C-bus interface
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness using a 31.25 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 122 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 15 Hz to 16.8 s and duty cycle from 0 % to 99.6 %
- Output state change programmable on the Acknowledge (bit 9, this bit is always set to 1 by I²C-bus master) or the STOP Command to update outputs byte-by-byte or all at the same time (default to ‘Change on STOP’).
- Active LOW Output Enable ($\overline{OE}$) input pin allows for hardware blinking and dimming of the LEDs
- Three quinary hardware address pins allow 125 PCU9956A devices to be connected to the same I²C-bus and to be individually programmed
- 4 software programmable I²C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for ‘All Call’ so that all the PCU9956As on the I²C-bus can be addressed at the same time and the second register used for three different addresses so that 1/3 of all devices on the bus can be addressed at the same time in a group). Software enable and disable for each programmable I²C-bus address.
- Unique power-up default Sub Call address allows mixing of devices with different channel widths
- Software Reset feature (SWRST Call) allows the device to be reset through the I²C-bus
- 8 MHz internal oscillator requires no external components

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- Internal power-on reset
- Noise filter on USDA/USCL inputs
- No glitch on LED outputs on power-up
- Low standby current
- Operating power supply voltage (V_{DD}) range of 3 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins
- −40 °C to +85 °C operation
- ESD protection exceeds 3000 V HBM per JESD22-A114
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: HTSSOP38

3. Applications

- Amusement products
- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCU9956ATW	PCU9956ATW	HTSSOP38	plastic thermal enhanced thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm; exposed die pad	SOT1331-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCU9956ATW	PCU9956ATWY	HTSSOP38	Reel 13” Q1/T1 *standard mark SMD dry pack	2500	T_{amb} = −40 °C to +85 °C

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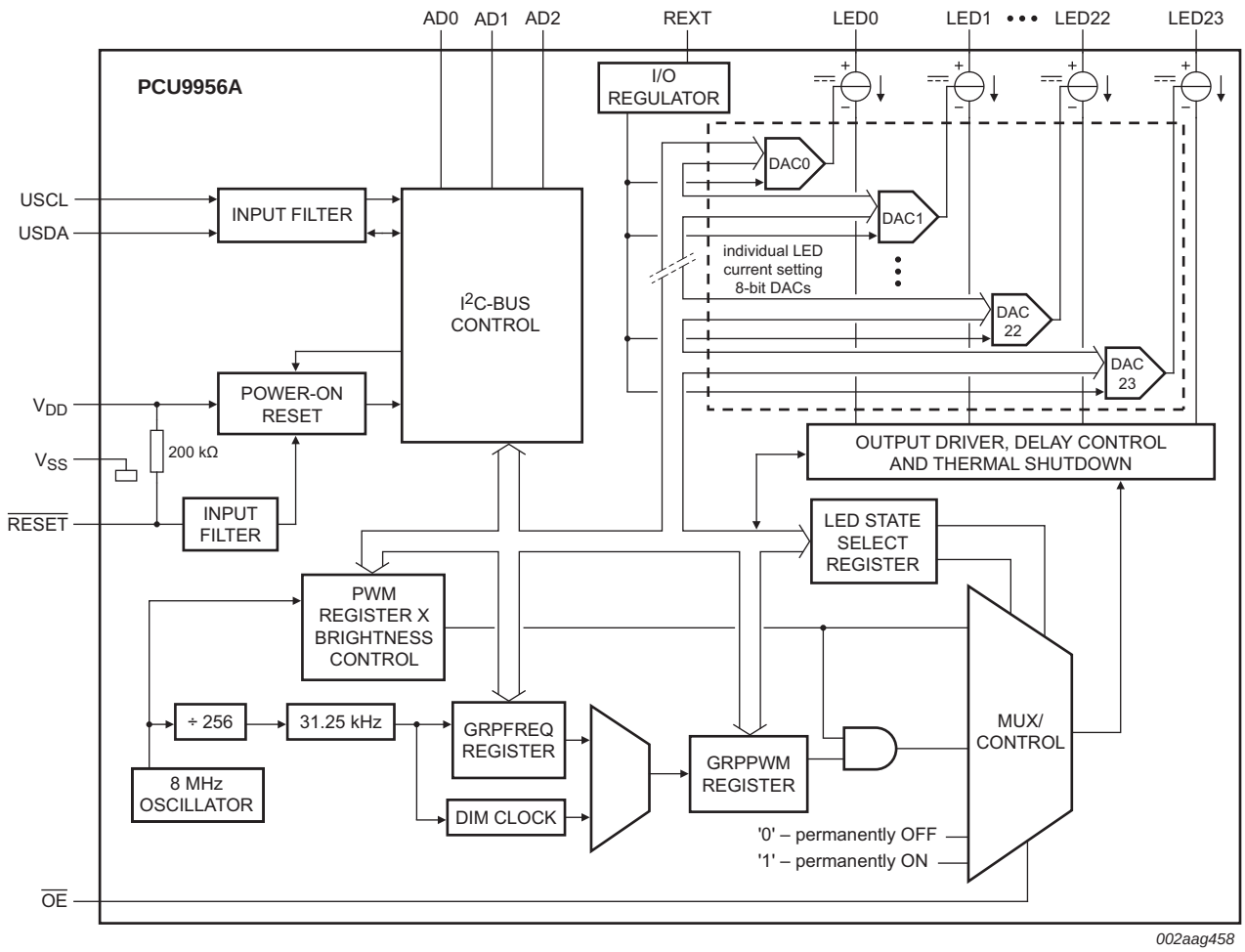
5. Block diagram



Dim repetition rate = 122 Hz.

Blink repetition rate = 15 Hz to every 16.8 seconds.

Fig 1. Block diagram of PCU9956A

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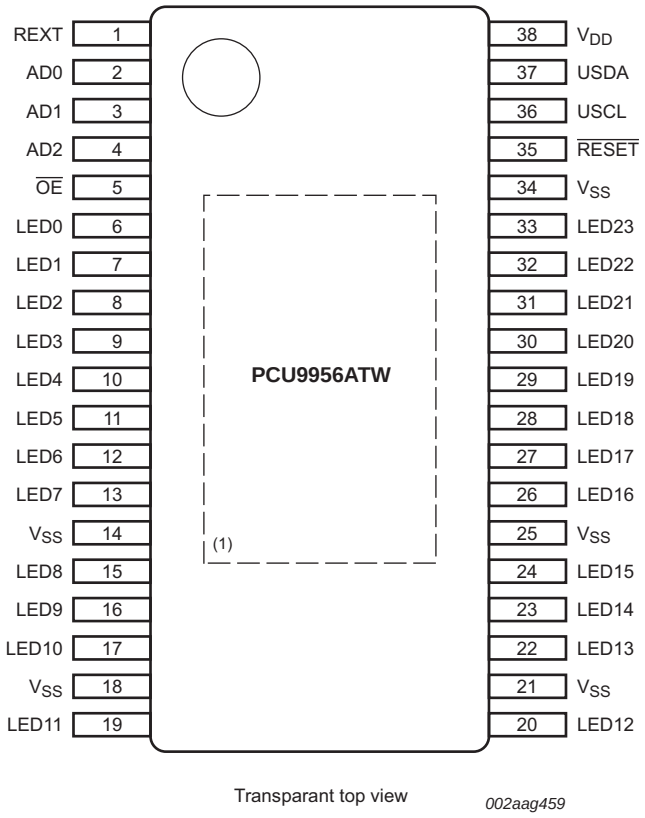
6. Pinning information

6.1 Pinning



(1) Thermal pad; connected to V_{SS}.

Fig 2. Pin configuration for HTSSOP38

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6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
REXT	1	I	current set resistor input; resistor to ground
AD0	2	I	address input 0
AD1	3	I	address input 1
AD2	4	I	address input 2
$\overline{OE}$	5	I	active LOW output enable for LEDs
LED0	6	O	LED driver 0
LED1	7	O	LED driver 1
LED2	8	O	LED driver 2
LED3	9	O	LED driver 3
LED4	10	O	LED driver 4
LED5	11	O	LED driver 5
LED6	12	O	LED driver 6
LED7	13	O	LED driver 7
LED8	15	O	LED driver 8
LED9	16	O	LED driver 9
LED10	17	O	LED driver 10
LED11	19	O	LED driver 11
LED12	20	O	LED driver 12
LED13	22	O	LED driver 13
LED14	23	O	LED driver 14
LED15	24	O	LED driver 15
LED16	26	O	LED driver 16
LED17	27	O	LED driver 17
LED18	28	O	LED driver 18
LED19	29	O	LED driver 19
LED20	30	O	LED driver 20
LED21	31	O	LED driver 21
LED22	32	O	LED driver 22
LED23	33	O	LED driver 23
$\overline{RESET}$	35	I	active LOW reset input
USCL	36	I	UFm serial clock line
USDA	37	I	UFm serial data line
V_{SS}	14, 18, 21, 25, 34[1]	ground	supply ground
V_{DD}	38	power supply	supply voltage

[1] HTSSOP38 package supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

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7. Functional description

Refer to Figure 1 “Block diagram of PCU9956A”.

7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

For PCU9956A there are a maximum of 125 possible programmable addresses using the three quinary hardware address pins.

7.1.1 Regular I²C-bus slave address

The I²C-bus slave address of the PCU9956A is shown in Figure 3. The 7-bit slave address is determined by the quinary input pads AD0, AD1 and AD2. Each pad can have one of five states (GND, pull-up, floating, pull-down, and V_{DD}) based on how the input pad is connected on the board. At power-up or hardware/software reset, the quinary input pads are sampled and set the slave address of the device internally. To conserve power, once the slave address is determined, the quinary input pads are turned off and will not be sampled until the next time the device is power cycled. Table 4 lists the five possible connections for the quinary input pads along with the external resistor values that must be used.

Table 4. Quinary input pad connection

Pad connection (pins AD2, AD1, AD0)[1]	Mnemonic	External resistor (kΩ)	
		Min.	Max.
tie to ground	GND	0	17.9
resistor pull-down to ground	PD	34.8	270
open (floating)	FLT	503	∞
resistor pull-up to V_{DD}	PU	31.7	340
tie to V_{DD}	V_{DD}	0	22.1

[1] These AD[2:0] inputs must be stable before the supply V_{DD} to chip.

Table 5 lists all 125 possible slave addresses of the device based on all combinations of the five states connected to three address input pins AD0, AD1 and AD2.

Table 5. I²C-bus slave address

Hardware selectable input pins			I²C-bus slave address for PCU9956A			
AD2	AD1	AD0	Decimal	Hex	Binary (A[6:0])	Address (R/$\overline{W}$ = 0)
GND	GND	GND	1	01	0000001[1]	02h
GND	GND	PD	2	02	0000010[1]	04h
GND	GND	FLT	3	03	0000011[1]	06h
GND	GND	PU	4	04	0000100[1]	08h
GND	GND	V_{DD}	5	05	0000101[1]	0Ah
GND	PD	GND	6	06	0000110[1]	0Ch
GND	PD	PD	7	07	0000111[1]	0Eh
GND	PD	FLT	8	08	0001000	10h
GND	PD	PU	9	09	0001001	12h

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Table 5. I²C-bus slave address *...continued*

Hardware selectable input pins			I²C-bus slave address for PCU9956A			
AD2	**AD1**	**AD0**	**Decimal**	**Hex**	**Binary (A[6:0])**	**Address (R/$\overline{W}$ = 0)**
GND	PD	V_{DD}	10	0A	0001010	14h
GND	FLT	GND	11	0B	0001011	16h
GND	FLT	PD	12	0C	0001100	18h
GND	FLT	FLT	13	0D	0001101	1Ah
GND	FLT	PU	14	0E	0001110	1Ch
GND	FLT	V_{DD}	15	0F	0001111	1Eh
GND	PU	GND	16	10	0010000	20h
GND	PU	PD	17	11	0010001	22h
GND	PU	FLT	18	12	0010010	24h
GND	PU	PU	19	13	0010011	26h
GND	PU	V_{DD}	20	14	0010100	28h
GND	V_{DD}	GND	21	15	0010101	2Ah
GND	V_{DD}	PD	22	16	0010110	2Ch
GND	V_{DD}	FLT	23	17	0010111	2Eh
GND	V_{DD}	PU	24	18	0011000	30h
GND	V_{DD}	V_{DD}	25	19	0011001	32h
PD	GND	GND	26	1A	0011010	34h
PD	GND	PD	27	1B	0011011	36h
PD	GND	FLT	28	1C	0011100	38h
PD	GND	PU	29	1D	0011101	3Ah
PD	GND	V_{DD}	30	1E	0011110	3Ch
PD	PD	GND	31	1F	0011111	3Eh
PD	PD	PD	32	20	0100000	40h
PD	PD	FLT	33	21	0100001	42h
PD	PD	PU	34	22	0100010	44h
PD	PD	V_{DD}	35	23	0100011	46h
PD	FLT	GND	36	24	0100100	48h
PD	FLT	PD	37	25	0100101	4Ah
PD	FLT	FLT	38	26	0100110	4Ch
PD	FLT	PU	39	27	0100111	4Eh
PD	FLT	V_{DD}	40	28	0101000	50h
PD	PU	GND	41	29	0101001	52h
PD	PU	PD	42	2A	0101010	54h
PD	PU	FLT	43	2B	0101011	56h
PD	PU	PU	44	2C	0101100	58h
PD	PU	V_{DD}	45	2D	0101101	5Ah

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Table 5. I²C-bus slave address *...continued*

Hardware selectable input pins			I²C-bus slave address for PCU9956A			
AD2	**AD1**	**AD0**	**Decimal**	**Hex**	**Binary (A[6:0])**	**Address (R/$\overline{W}$ = 0)**
PD	V_{DD}	GND	46	2E	0101110	5Ch
PD	V_{DD}	PD	47	2F	0101111	5Eh
PD	V_{DD}	FLT	48	30	0110000	60h
PD	V_{DD}	PU	49	31	0110001	62h
PD	V_{DD}	V_{DD}	50	32	0110010	64h
FLT	GND	GND	51	33	0110011	66h
FLT	GND	PD	52	34	0110100	68h
FLT	GND	FLT	53	35	0110101	6Ah
FLT	GND	PU	54	36	0110110	6Ch
FLT	GND	V_{DD}	55	37	0110111	6Eh
FLT	PD	GND	56	38	0111000	70h
FLT	PD	PD	57	39	0111001	72h
FLT	PD	FLT	58	3A	0111010	74h
FLT	PD	PU	59	3B	0111011	76h
FLT	PD	V_{DD}	60	3C	0111100	78h
FLT	FLT	GND	61	3D	0111101	7Ah
FLT	FLT	PD	62	3E	0111110	7Ch
FLT	FLT	FLT	63	3F	0111111	7Eh
FLT	FLT	PU	64	40	1000000	80h
FLT	FLT	V_{DD}	65	41	1000001	82h
FLT	PU	GND	66	42	1000010	84h
FLT	PU	PD	67	43	1000011	86h
FLT	PU	FLT	68	44	1000100	88h
FLT	PU	PU	69	45	1000101	8Ah
FLT	PU	V_{DD}	70	46	1000110	8Ch
FLT	V_{DD}	GND	71	47	1000111	8Eh
FLT	V_{DD}	PD	72	48	1001000	90h
FLT	V_{DD}	FLT	73	49	1001001	92h
FLT	V_{DD}	PU	74	4A	1001010	94h
FLT	V_{DD}	V_{DD}	75	4B	1001011	96h
PU	GND	GND	76	4C	1001100	98h
PU	GND	PD	77	4D	1001101	9Ah
PU	GND	FLT	78	4E	1001110	9Ch
PU	GND	PU	79	4F	1001111	9Eh
PU	GND	V_{DD}	80	50	1010000	A0h

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Table 5. I²C-bus slave address *...continued*

Hardware selectable input pins			I²C-bus slave address for PCU9956A			
AD2	**AD1**	**AD0**	**Decimal**	**Hex**	**Binary (A[6:0])**	**Address (R/$\overline{W}$ = 0)**
PU	PD	GND	81	51	1010001	A2h
PU	PD	PD	82	52	1010010	A4h
PU	PD	FLT	83	53	1010011	A6h
PU	PD	PU	84	54	1010100	A8h
PU	PD	V_{DD}	85	55	1010101	AAh
PU	FLT	GND	86	56	1010110	ACh
PU	FLT	PD	87	57	1010111	AEh
PU	FLT	FLT	88	58	1011000	B0h
PU	FLT	PU	89	59	1011001	B2h
PU	FLT	V_{DD}	90	5A	1011010	B4h
PU	PU	GND	91	5B	1011011	B6h
PU	PU	PD	92	5C	1011100	B8h
PU	PU	FLT	93	5D	1011101	BAh
PU	PU	PU	94	5E	1011110	BCh
PU	PU	V_{DD}	95	5F	1011111	BEh
PU	V_{DD}	GND	96	60	1100000	C0h
PU	V_{DD}	PD	97	61	1100001	C2h
PU	V_{DD}	FLT	98	62	1100010	C4h
PU	V_{DD}	PU	99	63	1100011	C6h
PU	V_{DD}	V_{DD}	100	64	1100100	C8h
V_{DD}	GND	GND	101	65	1100101	CAh
V_{DD}	GND	PD	102	66	1100110	CCh
V_{DD}	GND	FLT	103	67	1100111	CEh
V_{DD}	GND	PU	104	68	1101000	D0h
V_{DD}	GND	V_{DD}	105	69	1101001	D2h
V_{DD}	PD	GND	106	6A	1101010	D4h
V_{DD}	PD	PD	107	6B	1101011	D6h
V_{DD}	PD	FLT	108	6C	1101100	D8h
V_{DD}	PD	PU	109	6D	1101101	DAh
V_{DD}	PD	V_{DD}	110	6E	1101110	DCh
V_{DD}	FLT	GND	111	6F	1101111	DEh
V_{DD}	FLT	PD	112	70	1110000	E0h
V_{DD}	FLT	FLT	113	71	1110001	E2h
V_{DD}	FLT	PU	114	72	1110010	E4h
V_{DD}	FLT	V_{DD}	115	73	1110011	E6h
V_{DD}	PU	GND	116	74	1110100	E8h
V_{DD}	PU	PD	117	75	1110101	EAh
V_{DD}	PU	FLT	118	76	1110110	ECh
V_{DD}	PU	PU	119	77	1110111	EEh
V_{DD}	PU	V_{DD}	120	78	1111000[1]	F0h

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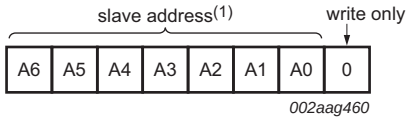
Table 5. I²C-bus slave address *...continued*

Hardware selectable input pins			I²C-bus slave address for PCU9956A			
AD2	**AD1**	**AD0**	**Decimal**	**Hex**	**Binary (A[6:0])**	**Address (R/$\overline{W}$ = 0)**
V_{DD}	V_{DD}	GND	121	79	1111001[1]	F2h
V_{DD}	V_{DD}	PD	122	7A	1111010[1]	F4h
V_{DD}	V_{DD}	FLT	123	7B	1111011[1]	F6h
V_{DD}	V_{DD}	PU	124	7C	1111100[1]	F8h
V_{DD}	V_{DD}	V_{DD}	125	7D	1111101[1]	FAh

[1] See ‘Remark’ below.

Remark: Reserved I²C-bus addresses must be used with caution since they can interfere with:

- ‘reserved for future use’ I²C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)
- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)



(1) This slave address must match one of the 125 internal addresses as shown in Table 5.

Fig 3. PCU9956A slave address

The last bit of the address byte defines the operation to be performed. Only writes to PCU9956A are supported, therefore the last bit is set to 0. No Read available with UFm I²C-bus.

7.1.2 LED All Call I²C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000X
- Programmable through I²C-bus (volatile programming)
- At power-up, LED All Call I²C-bus address is enabled.

See Section 7.3.10 “ALLCALLADR, LED All Call I²C-bus address” for more detail.

Remark: The default LED All Call I²C-bus address (E0h or 1110 000X) must not be used as a regular I²C-bus slave address since this address is enabled at power-up. All of the PCU9956As on the I²C-bus will recognize the address if sent by the I²C-bus master.

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7.1.3 LED Sub Call I²C-bus addresses

- 3 different I²C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: EEh or 1110 111X
  - SUBADR2 register: EEh or 1110 111X
  - SUBADR3 register: EEh or 1110 111X
- Programmable through I²C-bus (volatile programming)
- At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 I²C-bus addresses are disabled.

Remark: At power-up SUBADR1 identifies this device as a 24-channel driver.

See Section 7.3.9 “LED Sub Call I²C-bus addresses for PCU9956A” for more detail.

Remark: The default LED Sub Call I²C-bus addresses may be used as regular I²C-bus slave addresses as long as they are disabled.

7.2 Control register

Following the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the PCU9956A, which will be stored in the Control register.

The lowest 7 bits are used as a pointer to determine which register will be accessed (D[6:0]). The highest bit is used as Auto-Increment Flag (AIF).

This bit along with the MODE1 register bit 5 and bit 6 provide the Auto-Increment feature.

reset state = 80h

Remark: The Control register does not apply to the Software Reset I²C-bus address.

Fig 4. Control register

When the Auto-Increment Flag is set (AIF = logic 1), the seven low order bits of the Control register are automatically incremented after a write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values of MODE1 register.

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Table 6. Auto-Increment options

AIF	AI1[1]	AI0[1]	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for registers (00h to 3Eh). D[6:0] roll over to 00h after the last register 3Eh is accessed.
1	0	1	Auto-Increment for individual brightness registers only (0Ah to 21h). D[6:0] roll over to 0Ah after the last register (21h) is accessed.
1	1	0	Auto-Increment for MODE1 to IREF23 control registers (00h to 39h). D[6:0] roll over to 00h after the last register (39h) is accessed.
1	1	1	Auto-Increment for global control registers and individual brightness registers (08h to 21h). D[6:0] roll over to 08h after the last register (21h) is accessed.

[1] AI1 and AI0 come from MODE1 register.

Remark: Other combinations not shown in Table 6 (AIF + AI[1:0] = 001b, 010b and 011b) are reserved and must not be used for proper device operation.

AIF + AI[1:0] = 000b is used when the same register must be accessed several times during a single I²C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AIF + AI[1:0] = 100b is used when all the registers must be sequentially accessed, for example, power-up programming.

AIF + AI[1:0] = 101b is used when the 24 LED drivers must be individually programmed with different values during the same I²C-bus communication, for example, changing color setting to another color setting.

AIF + AI[1:0] = 110b is used when MODE1 to IREF23 registers must be programmed with different settings during the same I²C-bus communication.

AIF + AI[1:0] = 111b is used when the 24 LED drivers must be individually programmed with different values in addition to global programming.

Only the 7 least significant bits D[6:0] are affected by the AIF, AI1 and AI0 bits.

When the Control register is written, the register entry point determined by D[6:0] is the first register that will be addressed (write operation), and can be anywhere between 00h and 3Eh (as defined in Table 7). When AIF = 1, the Auto-Increment Flag is set and the rollover value at which the register increment stops and goes to the next one is determined by AIF, AI1 and AI0. See Table 6 for rollover values. For example, if MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1001 0000, then the register addressing sequence will be (in hex):
10 → 11 → … → 21 → 0A → 0B → … → 21 → 0A → 0B → … as long as the master keeps sending data.

If MODE1 register bit AI1 = 0 and AI0 = 0 and if the Control register = 1010 0010, then the register addressing sequence will be (in hex):
22 → 23 → … → 3E → 00 → 01 → … → 21 → 0A → 0B → … as long as the master keeps sending data.

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If MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1000 0101, then the register addressing sequence will be (in hex):
05 → 06 → … → 21 → 0A → 0B → … → 21 → 0A → 0B → … as long as the master keeps sending data.

Remark: Writing to registers marked 'not used' will be ignored.

7.3 Register definitions

Table 7. Register summary

Register number (hex)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	0	0	0	MODE1	write only	Mode register 1
01h	0	0	0	0	0	0	1	MODE2	write only	Mode register 2
02h	0	0	0	0	0	1	0	LEDOUT0	write only	LED output state 0
03h	0	0	0	0	0	1	1	LEDOUT1	write only	LED output state 1
04h	0	0	0	0	1	0	0	LEDOUT2	write only	LED output state 2
05h	0	0	0	0	1	0	1	LEDOUT3	write only	LED output state 3
06h	0	0	0	0	1	1	0	LEDOUT4	write only	LED output state 4
07h	0	0	0	0	1	1	1	LEDOUT5	write only	LED output state 5
08h	0	0	0	1	0	0	0	GRPPWM	write only	group duty cycle control
09h	0	0	0	1	0	0	1	GRPFREQ	write only	group frequency
0Ah	0	0	0	1	0	1	0	PWM0	write only	brightness control LED0
0Bh	0	0	0	1	0	1	1	PWM1	write only	brightness control LED1
0Ch	0	0	0	1	1	0	0	PWM2	write only	brightness control LED2
0Dh	0	0	0	1	1	0	1	PWM3	write only	brightness control LED3
0Eh	0	0	0	1	1	1	0	PWM4	write only	brightness control LED4
0Fh	0	0	0	1	1	1	1	PWM5	write only	brightness control LED5
10h	0	0	1	0	0	0	0	PWM6	write only	brightness control LED6
11h	0	0	1	0	0	0	1	PWM7	write only	brightness control LED7
12h	0	0	1	0	0	1	0	PWM8	write only	brightness control LED8
13h	0	0	1	0	0	1	1	PWM9	write only	brightness control LED9
14h	0	0	1	0	1	0	0	PWM10	write only	brightness control LED10
15h	0	0	1	0	1	0	1	PWM11	write only	brightness control LED11
16h	0	0	1	0	1	1	0	PWM12	write only	brightness control LED12
17h	0	0	1	0	1	1	1	PWM13	write only	brightness control LED13
18h	0	0	1	1	0	0	0	PWM14	write only	brightness control LED14
19h	0	0	1	1	0	0	1	PWM15	write only	brightness control LED15
1Ah	0	0	1	1	0	1	0	PWM16	write only	brightness control LED16
1Bh	0	0	1	1	0	1	1	PWM17	write only	brightness control LED17
1Ch	0	0	1	1	1	0	0	PWM18	write only	brightness control LED18
1Dh	0	0	1	1	1	0	1	PWM19	write only	brightness control LED19
1Eh	0	0	1	1	1	1	0	PWM20	write only	brightness control LED20
1Fh	0	0	1	1	1	1	1	PWM21	write only	brightness control LED21

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Table 7. Register summary *...continued*

Register number (hex)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
20h	0	1	1	0	0	0	0	PWM22	write only	brightness control LED22
21h	0	1	1	0	0	0	1	PWM23	write only	brightness control LED23
22h	0	1	0	0	0	1	0	IREF0	write only	output gain control register 0
23h	0	1	0	0	0	1	1	IREF1	write only	output gain control register 1
24h	0	1	0	0	1	0	0	IREF2	write only	output gain control register 2
25h	0	1	0	0	1	0	1	IREF3	write only	output gain control register 3
26h	0	1	0	0	1	1	0	IREF4	write only	output gain control register 4
27h	0	1	0	0	1	1	1	IREF5	write only	output gain control register 5
28h	0	1	0	1	0	0	0	IREF6	write only	output gain control register 6
29h	0	1	0	1	0	0	1	IREF7	write only	output gain control register 7
2Ah	0	1	0	1	0	1	0	IREF8	write only	output gain control register 8
2Bh	0	1	0	1	0	1	1	IREF9	write only	output gain control register 9
2Ch	0	1	0	1	1	0	0	IREF10	write only	output gain control register 10
2Dh	0	1	0	1	1	0	1	IREF11	write only	output gain control register 11
2Eh	0	1	0	1	1	1	0	IREF12	write only	output gain control register 12
2Fh	0	1	0	1	1	1	1	IREF13	write only	output gain control register 13
30h	0	1	1	0	0	0	0	IREF14	write only	output gain control register 14
31h	0	1	1	0	0	0	1	IREF15	write only	output gain control register 15
32h	0	1	1	0	0	1	0	IREF16	write only	output gain control register 16
33h	0	1	1	0	0	1	1	IREF17	write only	output gain control register 17
34h	0	1	1	0	1	0	0	IREF18	write only	output gain control register 18
35h	0	1	1	0	1	0	1	IREF19	write only	output gain control register 19
36h	0	1	1	0	1	1	0	IREF20	write only	output gain control register 20
37h	0	1	1	0	1	1	1	IREF21	write only	output gain control register 21
38h	0	1	1	1	0	0	0	IREF22	write only	output gain control register 22
39h	0	1	1	1	0	0	1	IREF23	write only	output gain control register 23
3Ah	0	1	1	1	0	1	0	OFFSET	write only	Offset/delay on LEDn outputs
3Bh	0	1	1	1	0	1	1	SUBADR1	write only	I²C-bus subaddress 1
3Ch	0	1	1	1	1	0	0	SUBADR2	write only	I²C-bus subaddress 2
3Dh	0	1	1	1	1	0	1	SUBADR3	write only	I²C-bus subaddress 3
3Eh	0	1	1	1	1	1	0	ALLCALLADR	write only	All Call I²C-bus address
3Fh	0	1	1	1	1	1	1	PWMALL	write only	brightness control for all LEDn
40h	1	0	0	0	0	0	0	IREFALL	write only	output gain control for all registers IREF0 to IREF23
41h to 7Fh	-	-	-	-	-	-	-	reserved	write only	not used[1]

[1] Writing to registers marked ‘not used’ will be ignored.

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7.3.1 MODE1 — Mode register 1

Table 8. MODE1 - Mode register 1 (address 00h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	AIF	write only	0	Register Auto-Increment disabled.
			1*	Register Auto-Increment enabled (write default logic 1).
6	AI1	write only	0*	Auto-Increment bit 1 = 0. Auto-increment range as defined in Table 6.
			1	Auto-Increment bit 1 = 1. Auto-increment range as defined in Table 6.
5	AI0	write only	0*	Auto-Increment bit 0 = 0. Auto-increment range as defined in Table 6.
			1	Auto-Increment bit 0 = 1. Auto-increment range as defined in Table 6.
4	SLEEP	write only	0*	Normal mode[1].
			1	Low power mode. Oscillator off[2][3].
3	SUB1	write only	0	PCU9956A does not respond to I²C-bus subaddress 1.
			1*	PCU9956A responds to I²C-bus subaddress 1.
2	SUB2	write only	0*	PCU9956A does not respond to I²C-bus subaddress 2.
			1	PCU9956A responds to I²C-bus subaddress 2.
1	SUB3	write only	0*	PCU9956A does not respond to I²C-bus subaddress 3.
			1	PCU9956A responds to I²C-bus subaddress 3.
0	ALLCALL	write only	0	PCU9956A does not respond to LED All Call I²C-bus address.
			1*	PCU9956A responds to LED All Call I²C-bus address.

[1] It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μs window.

[2] No blinking or dimming is possible when the oscillator is off.

[3] The device must be reset if the LED driver output state is set to LDRx=11 after the device is set back to Normal mode.

7.3.2 MODE2 — Mode register 2

Table 9. MODE2 - Mode register 2 (address 01h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	-	-	0*	not used (must write a logic 0)
6	-	-	0*	not used (must write a logic 0)
5	DMBLNK	write only	0*	group control = dimming.
			1	group control = blinking.
4	-	-	0*	reserved (must write a logic 0)
3	OCH	write only	0*	outputs change on STOP command
			1	outputs change on ACK; this ninth bit is always set to 1 by UFm I²C-bus master
2	-	-	1*	reserved (must write a logic 1)
1	-	-	0*	reserved (must write a logic 0)
0	-	-	1*	reserved (must write a logic 1)

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7.3.3 LEDOUT0 to LEDOUT5, LED driver output state

Table 10. LEDOUT0 to LEDOUT5 - LED driver output state registers (address 02h to 07h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	LEDOUT0	7:6	LDR3	write only	10*	LED3 output state control
		5:4	LDR2	write only	10*	LED2 output state control
		3:2	LDR1	write only	10*	LED1 output state control
		1:0	LDR0	write only	10*	LED0 output state control
03h	LEDOUT1	7:6	LDR7	write only	10*	LED7 output state control
		5:4	LDR6	write only	10*	LED6 output state control
		3:2	LDR5	write only	10*	LED5 output state control
		1:0	LDR4	write only	10*	LED4 output state control
04h	LEDOUT2	7:6	LDR11	write only	10*	LED11 output state control
		5:4	LDR10	write only	10*	LED10 output state control
		3:2	LDR9	write only	10*	LED9 output state control
		1:0	LDR8	write only	10*	LED8 output state control
05h	LEDOUT3	7:6	LDR15	write only	10*	LED15 output state control
		5:4	LDR14	write only	10*	LED14 output state control
		3:2	LDR13	write only	10*	LED13 output state control
		1:0	LDR12	write only	10*	LED12 output state control
06h	LEDOUT4	7:6	LDR19	write only	10*	LED19 output state control
		5:4	LDR18	write only	10*	LED18 output state control
		3:2	LDR17	write only	10*	LED17 output state control
		1:0	LDR16	write only	10*	LED16 output state control
07h	LEDOUT5	7:6	LDR23	write only	10*	LED23 output state control
		5:4	LDR22	write only	10*	LED22 output state control
		3:2	LDR21	write only	10*	LED21 output state control
		1:0	LDR20	write only	10*	LED20 output state control

LDRx = 00 — LED driver x is off (x = 0 to 23).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled). The $\overline{OE}$ pin can be used as external dimming/blinking control in this state.

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register (default power-up state).

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

Remark: Setting the device in low power mode while being on group dimming/blinking mode may cause the LED output state to be in an unknown state after the device is set back to normal mode. The device must be reset and all register values reprogrammed.

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7.3.4 GRPPWM, group duty cycle control

Table 11. GRPPWM - Group brightness control register (address 08h) bit description

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
08h	GRPPWM	7:0	GDC[7:0]	write only	1111 1111*	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 122 Hz fixed frequency signal is superimposed with the 31.25 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a 'Don't care'.

General brightness for the 24 outputs is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT5 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 67 ms to 16.8 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle = \frac{GDC[7:0]}{256} \quad (1)$$

7.3.5 GRPFREQ, group frequency

Table 12. GRPFREQ - Group frequency register (address 09h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
09h	GRPFREQ	7:0	GFRQ[7:0]	write only	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a 'Don't care' when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT5 registers).

Blinking period is controlled through 256 linear steps from 00h (67 ms, frequency 15 Hz) to FFh (16.8 s).

$$global\ blinking\ period = \frac{GFRQ[7:0] + 1}{15.26}(s) \quad (2)$$

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7.3.6 PWM0 to PWM23, individual brightness control

Table 13. PWM0 to PWM23 - PWM registers 0 to 23 (address 0Ah to 21h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Ah	PWM0	7:0	IDC0[7:0]	write only	0000 0000*	PWM0 Individual Duty Cycle
0Bh	PWM1	7:0	IDC1[7:0]	write only	0000 0000*	PWM1 Individual Duty Cycle
0Ch	PWM2	7:0	IDC2[7:0]	write only	0000 0000*	PWM2 Individual Duty Cycle
0Dh	PWM3	7:0	IDC3[7:0]	write only	0000 0000*	PWM3 Individual Duty Cycle
0Eh	PWM4	7:0	IDC4[7:0]	write only	0000 0000*	PWM4 Individual Duty Cycle
0Fh	PWM5	7:0	IDC5[7:0]	write only	0000 0000*	PWM5 Individual Duty Cycle
10h	PWM6	7:0	IDC6[7:0]	write only	0000 0000*	PWM6 Individual Duty Cycle
11h	PWM7	7:0	IDC7[7:0]	write only	0000 0000*	PWM7 Individual Duty Cycle
12h	PWM8	7:0	IDC8[7:0]	write only	0000 0000*	PWM8 Individual Duty Cycle
13h	PWM9	7:0	IDC9[7:0]	write only	0000 0000*	PWM9 Individual Duty Cycle
14h	PWM10	7:0	IDC10[7:0]	write only	0000 0000*	PWM10 Individual Duty Cycle
15h	PWM11	7:0	IDC11[7:0]	write only	0000 0000*	PWM11 Individual Duty Cycle
16h	PWM12	7:0	IDC12[7:0]	write only	0000 0000*	PWM12 Individual Duty Cycle
17h	PWM13	7:0	IDC13[7:0]	write only	0000 0000*	PWM13 Individual Duty Cycle
18h	PWM14	7:0	IDC14[7:0]	write only	0000 0000*	PWM14 Individual Duty Cycle
19h	PWM15	7:0	IDC15[7:0]	write only	0000 0000*	PWM15 Individual Duty Cycle
1Ah	PWM16	7:0	IDC16[7:0]	write only	0000 0000*	PWM16 Individual Duty Cycle
1Bh	PWM17	7:0	IDC17[7:0]	write only	0000 0000*	PWM17 Individual Duty Cycle
1Ch	PWM18	7:0	IDC18[7:0]	write only	0000 0000*	PWM18 Individual Duty Cycle
1Dh	PWM19	7:0	IDC19[7:0]	write only	0000 0000*	PWM19 Individual Duty Cycle
1Eh	PWM20	7:0	IDC20[7:0]	write only	0000 0000*	PWM20 Individual Duty Cycle
1Fh	PWM21	7:0	IDC21[7:0]	write only	0000 0000*	PWM21 Individual Duty Cycle
20h	PWM22	7:0	IDC22[7:0]	write only	0000 0000*	PWM22 Individual Duty Cycle
21h	PWM23	7:0	IDC23[7:0]	write only	0000 0000*	PWM23 Individual Duty Cycle

A 31.25 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT5 registers).

$$duty\ cycle = \frac{IDCx[7:0]}{256} \quad (3)$$

Remark: The first lower end 8 steps of PWM and the last (higher end) steps of PWM will not have effective brightness control of LEDs due to edge rate control of LED output pins.

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7.3.7 IREF0 to IREF23, LED output current value registers

These registers reflect the gain settings for output current for LED0 to LED23.

Table 14. IREF0 to IREF23 - LED output gain control registers (address 22h to 39h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
22h	IREF0	7:0	write only	00h*	LED0 output current setting
23h	IREF1	7:0	write only	00h*	LED1 output current setting
24h	IREF2	7:0	write only	00h*	LED2 output current setting
25h	IREF3	7:0	write only	00h*	LED3 output current setting
26h	IREF4	7:0	write only	00h*	LED4 output current setting
27h	IREF5	7:0	write only	00h*	LED5 output current setting
28h	IREF6	7:0	write only	00h*	LED6 output current setting
29h	IREF7	7:0	write only	00h*	LED7 output current setting
2Ah	IREF8	7:0	write only	00h*	LED8 output current setting
2Bh	IREF9	7:0	write only	00h*	LED9 output current setting
2Ch	IREF10	7:0	write only	00h*	LED10 output current setting
2Dh	IREF11	7:0	write only	00h*	LED11 output current setting
2Eh	IREF12	7:0	write only	00h*	LED12 output current setting
2Fh	IREF13	7:0	write only	00h*	LED13 output current setting
30h	IREF14	7:0	write only	00h*	LED14 output current setting
31h	IREF15	7:0	write only	00h*	LED15 output current setting
32h	IREF16	7:0	write only	00h*	LED16 output current setting
33h	IREF17	7:0	write only	00h*	LED17 output current setting
34h	IREF18	7:0	write only	00h*	LED18 output current setting
35h	IREF19	7:0	write only	00h*	LED19 output current setting
36h	IREF20	7:0	write only	00h*	LED20 output current setting
37h	IREF21	7:0	write only	00h*	LED21 output current setting
38h	IREF22	7:0	write only	00h*	LED22 output current setting
39h	IREF23	7:0	write only	00h*	LED23 output current setting

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7.3.8 OFFSET — LEDn output delay offset register

Table 15. OFFSET - LEDn output delay offset register (address 3Ah) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
3Ah	OFFSET	7:4	-	0000*	not used (must write a logic 0)
		3:0	write only	1000*	LEDn output delay offset factor

The PCU9956A can be programmed to have turn-on delay between LED outputs. This helps to reduce peak current for the V_{DD} supply and reduces EMI.

The order in which the LED outputs are enabled will always be the same (channel 0 will enable first and channel 23 will enable last).

OFFSET control register bits [3:0] determine the delay used between the turn-on times as follows:

0000 = no delay between outputs (all on, all off at the same time)

0001 = delay of 1 clock cycle (125 ns) between successive outputs

0010 = delay of 2 clock cycles (250 ns) between successive outputs

0011 = delay of 3 clock cycles (375 ns) between successive outputs

:

0111 = delay of 7 clock cycles (875 ns) between successive outputs

1000 = delay of 8 clock cycles (1 μs) between successive outputs

1001 = delay of 9 clock cycles (1.125 μs) between successive outputs

1010 = delay of 10 clock cycles (1.25 μs) between successive outputs

1011 = delay of 11 clock cycles (1.375 μs) between successive outputs

1100 to 1111 = reserved and do not use

Example: If the value in the OFFSET register is 1000 the corresponding delay = 8 × 125 ns = 1 μs delay between successive outputs.

channel 0 turns on at time 0 μs

channel 1 turns on at time 1 μs

channel 2 turns on at time 2 μs

channel 3 turns on at time 3 μs

channel 4 turns on at time 4 μs

channel 5 turns on at time 5 μs

channel 6 turns on at time 6 μs

channel 7 turns on at time 7 μs

channel 8 turns on at time 8 μs

channel 9 turns on at time 9 μs

channel 10 turns on at time 10 μs

channel 11 turns on at time 11 μs

channel 12 turns on at time 12 μs

channel 13 turns on at time 13 μs

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channel 14 turns on at time 14 µs

channel 15 turns on at time 15 µs

channel 16 turns on at time 16 µs

channel 17 turns on at time 17 µs

channel 18 turns on at time 18 µs

channel 19 turns on at time 19 µs

channel 20 turns on at time 20 µs

channel 21 turns on at time 21 µs

channel 22 turns on at time 22 µs

channel 23 turns on at time 23 µs

7.3.9 LED Sub Call I²C-bus addresses for PCU9956A

Table 16. SUBADR1 to SUBADR3 - I²C-bus subaddress registers 1 to 3 (address 3Bh to 3Dh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
3Bh	SUBADR1	7:1	A1[7:1]	write only	1110 111*	I²C-bus subaddress 1
		0	A1[0]	write only	0*	reserved
3Ch	SUBADR2	7:1	A2[7:1]	write only	1110 111*	I²C-bus subaddress 2
		0	A2[0]	write only	0*	reserved
3Dh	SUBADR3	7:1	A3[7:1]	write only	1110 111*	I²C-bus subaddress 3
		0	A3[0]	write only	0*	reserved

Default power-up values are EEh, EEh, EEh. At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 are disabled. The power-up default bit subaddress of EEh indicates that this device is a 24-channel LED driver.

All three subaddresses are programmable. Once subaddresses have been programmed to their right values, SUBx bits need to be set to logic 1 in order to have the device respond to these addresses (MODE1 register) (0). When SUBx is set to logic 1, the corresponding I²C-bus subaddress can be used during a UFm I²C-bus write sequence.

7.3.10 ALLCALLADR, LED All Call I²C-bus address

Table 17. ALLCALLADR - LED All Call I²C-bus address register (address 3Eh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
3Eh	ALLCALLADR	7:1	AC[7:1]	write only	1110 000*	ALLCALL I²C-bus address register
		0	AC[0]	write only	0*	reserved

The LED All Call I²C-bus address allows all the PCU9956As on the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to logic 1 [power-up default state]). This address is programmable through the I²C-bus and can be used during an I²C-bus write sequence. The register address can also be programmed as a Sub Call.

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Only the 7 MSBs representing the All Call I²C-bus address are valid. The LSB in ALLCALLADR register must write a logic 0.

If ALLCALL bit = 0 in MODE1 register, the device does not recognize the address programmed in register ALLCALLADR.

7.3.11 PWMALL — brightness control for all LEDn outputs

When programmed, the value in this register will be used for PWM duty cycle for all the LEDn outputs and will be reflected in PWM 0 through PWM23 registers.

Table 18. PWMALL - brightness control for all LEDn outputs register (address 3Fh) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
3Fh	PWMALL	7:0	write only	0000 0000*	duty cycle for all LEDn outputs

Remark: Write to any of the PWM0 to PWM23 registers will overwrite the value in corresponding PWMn register programmed by PWMALL.

7.3.12 IREFALL register: output current value for all LED outputs

The output current setting for all outputs is held in this register. When this register is written to or updated, all LED outputs will be set to a current corresponding to this register value.

Writes to IREF0 to IREF23 will overwrite the output current settings.

Table 19. IREFALL - Output gain control for all LED outputs (address 40h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
40h	IREFALL	7:0	write only	00h*	current gain setting for all LED outputs

7.3.13 LED driver constant current outputs

In LED display applications, PCU9956A provides nearly no current variations from channel to channel and from device to device. The maximum current skew between channels is less than ±4 % and less than ±6 % between devices.

7.3.13.1 Adjusting output current

The PCU9956A scales up the reference current (I_{ref}) set by the external resistor (R_{ext}) to sink the output current (I_O) at each output port. The maximum output current for the outputs can be set using R_{ext}. In addition, the constant value for current drive at each of the outputs is independently programmable using command registers IREF0 to IREF23. Alternatively, programming the IREFALL register allows all outputs to be set at one current value determined by the value in IREFALL register.

Equation 4 and Equation 5 can be used to calculate the minimum and maximum constant current values that can be programmed for the outputs for a chosen R_{ext}.

$$I_O_LED_MIN = \frac{900\ mV}{R_{ext}} \times \frac{1}{4}\ (\text{minimum constant current}) \quad (4)$$

$$I_O_LED_MAX = (255 \times I_O_LED_MIN) = \left(\frac{900\ mV}{R_{ext}} \times \frac{255}{4}\right) \quad (5)$$

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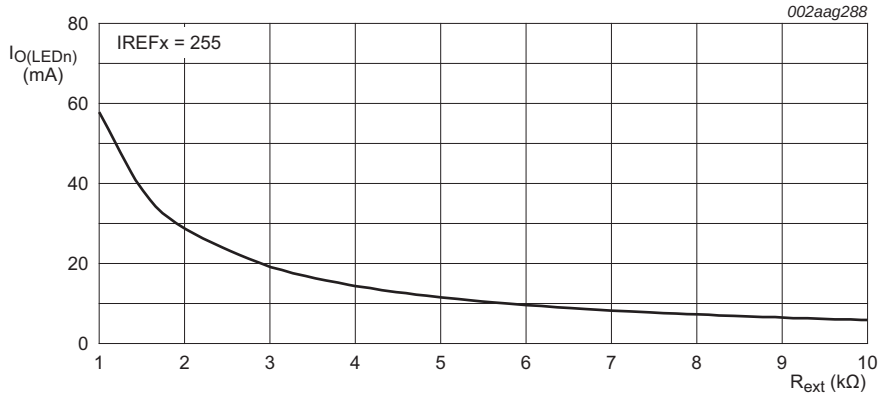
For a given IREFx setting, $I_{O}_LED = IREFx \times \frac{900\ mV}{R_{ext}} \times \frac{1}{4}$.



$I_{O(LEDn)}$ (mA) = IREFx × (0.9 / 4) / R_{ext} (kΩ)

maximum $I_{O(LEDn)}$ (mA) = 255 × (0.9 / 4) / R_{ext} (kΩ)

Remark: Default IREFx at power-up = 0.

Fig 5. Maximum I_{LED} versus R_{ext}

Example 1: If R_{ext} = 1 kΩ, I_O_LED_MIN = 225 μA, I_O_LED_MAX = 57.375 mA (as shown in Figure 6).

So each channel can be programmed with its individual IREFx in 256 steps and in 225 μA increments to a maximum output current of 57.375 mA independently.

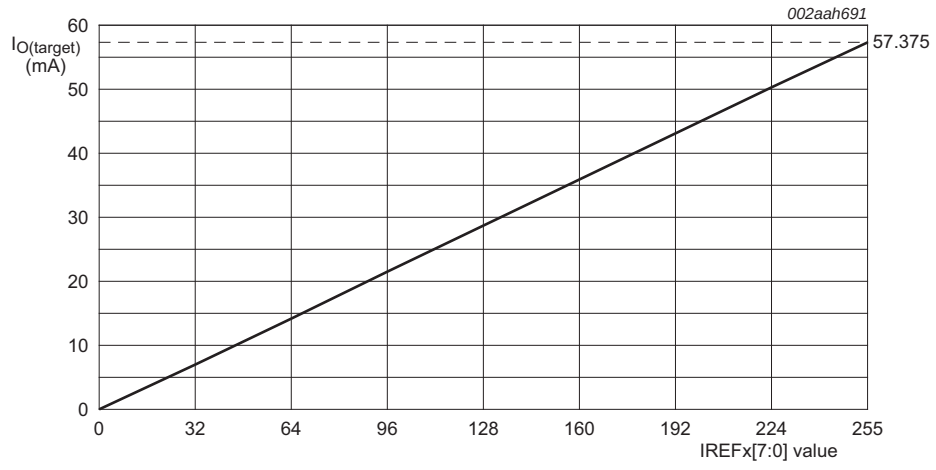


Fig 6. $I_{O(target)}$ versus IREFx value with R_{ext} = 1 kΩ

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Example 2: If R_{ext} = 2 kΩ, I_{O}_LED_MIN = 112.5 μA, I_{O}_LED_MAX = 28.687 mA (as shown in Figure 7).

So each channel can be programmed with its individual IREFx in 256 steps and in 112.5 μA increments to a maximum output channel of 28.687 mA independently.

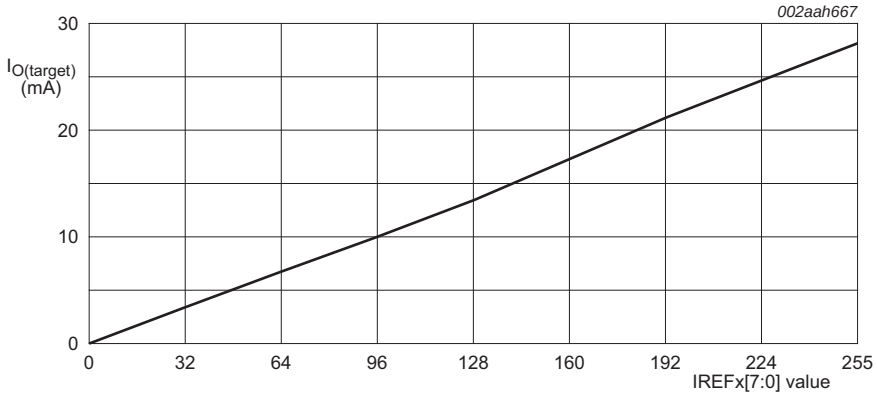

Fig 7. $I_{O(target)}$ versus IREFx value with R_{ext} = 2 kΩ

7.3.14 Overtemperature protection

If the PCU9956A chip temperature exceeds its limit (T_{max}, see Table 22), all output channels will be disabled until the temperature drops below its limit minus a small hysteresis (T_{hys}, see Table 22). Once the die temperature reduces below the $T_{max} - T_{hys}$, the chip will return to the same condition it was prior to the overtemperature event.

7.4 Active LOW output enable input

The active LOW output enable ($\overline{OE}$) pin on PCU9956A allows to enable or disable all the LED outputs at the same time.

- When a LOW level is applied to $\overline{OE}$ pin, all the LED outputs are enabled.
- When a HIGH level is applied to $\overline{OE}$ pin, all the LED outputs are high-impedance.

The $\overline{OE}$ pin can be used as a synchronization signal to switch on/off several PCU9956A devices at the same time when LED drive output state is set fully ON (LDRx = 01 in LEDOUTx register) in these devices. This requires an external clock reference that provides blinking period and the duty cycle.

The $\overline{OE}$ pin can also be used as an external dimming control signal. The frequency of the external clock must be high enough not to be seen by the human eye, and the duty cycle value determines the brightness of the LEDs.

Remark: Do not use $\overline{OE}$ as an external blinking control signal when internal global blinking is selected (DMBLNK = 1, MODE2 register) since it will result in an undefined blinking pattern. Do not use $\overline{OE}$ as an external dimming control signal when internal global dimming is selected (DMBLNK = 0, MODE2 register) since it will result in an undefined dimming pattern.

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7.5 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCU9956A in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCU9956A registers and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be pulled lower than 1 V and stay LOW for longer than 20 μs. The device will reset itself, and allow 2 ms for the device to fully wake up.

Remark: In order to guarantee a proper Power-On Reset operation for device, the rising rate of V_{DD} must be less than 3 ms per 1 V or less than 10 ms from 0 V to 3.3 V. Also, V_{DD} must return to 0 V for a minimum of 10 ms before rising again while V_{DD} power is re-cycling.

7.6 Hardware reset recovery

When a reset of PCU9956A is activated using an active LOW input on the $\overline{\text{RESET}}$ pin, a reset pulse width of 2.5 μs minimum is required. The maximum wait time after $\overline{\text{RESET}}$ pin is released is 1.5 ms.

7.7 Software reset

The Software Reset Call (SWRST Call) allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The maximum wait time after software reset is 1 ms.

The SWRST Call function is defined as the following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call address ‘0000 000’ with the R/$\overline{\text{W}}$ bit set to ‘0’ (write) is sent by the I²C-bus master.
3. Since PCU9956A is a UFm I²C-bus device, no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent, the master sends 1 byte with 1 specific value (SWRST data byte 1): Byte 1 = 06h.

   If more than 1 byte of data is sent, they will be ignored by the PCU9956A.
5. Once the correct byte (SWRST data byte 1) has been sent, the master sends a STOP command to end the SWRST function: the PCU9956A then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

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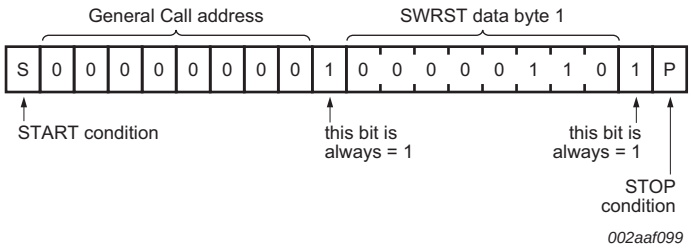

Fig 8. SWRST Call

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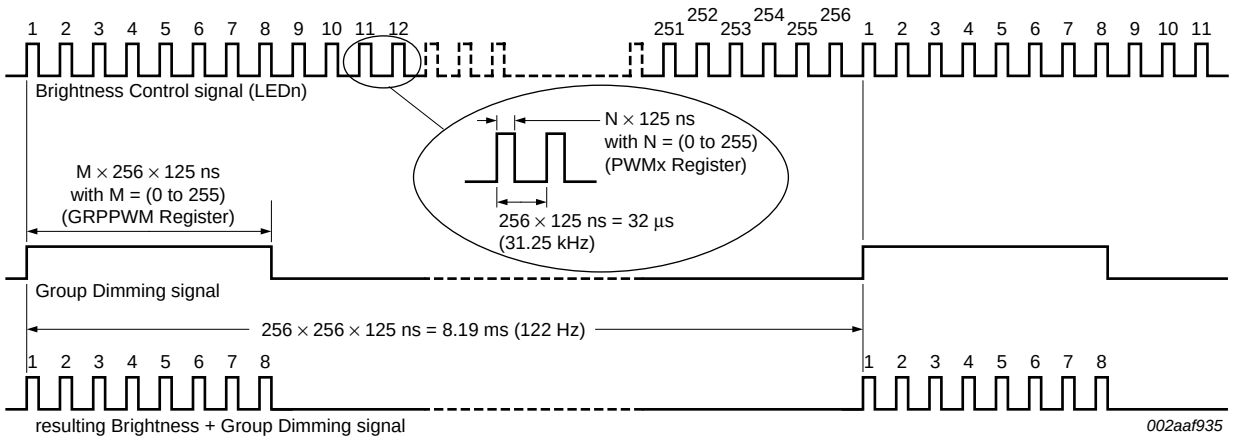
7.8 Individual brightness control with group dimming/blinking

A 31.25 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 24 LED outputs LED0 to LED23).

- A lower 122 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 15 Hz to every 16.8 seconds (8 bits, 256 steps) with programmable duty cycle (8 bits, 256 steps) is used to provide a global blinking control.



Minimum pulse width for LEDn Brightness Control is 125 ns.

Minimum pulse width for Group Dimming is 32 µs.

When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal will have 1 pulse of the LED Brightness Control signal (pulse width = N × 125 ns, with 'N' defined in PWMx register).

This resulting Brightness + Group Dimming signal above shows a resulting Control signal with M = 8.

Fig 9. Brightness + Group Dimming signals

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8. Characteristics of the PCU9956A Ultra Fast-mode I²C-bus

The PCU9956A LED controller uses the new Ultra Fast-mode (UFm) I²C-bus to communicate with the UFm I²C-bus capable host controller. Like the Standard mode and Fast-mode Plus (Fm+) I²C-bus, it uses two lines for communication. They are a serial data line (USDA) and a serial clock line (USCL). The UFm is a unidirectional bus that is capable of higher frequency (up to 5 MHz). The UFm I²C-bus slave devices operate in receive-only mode. That is, only I²C writes to PCU9956A are supported.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the USDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 10).

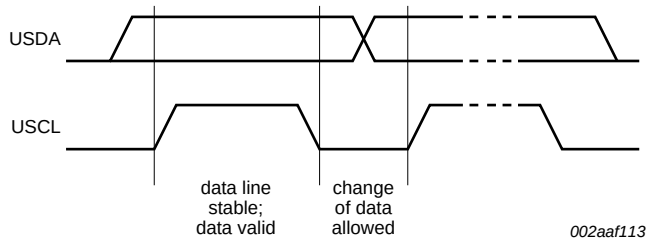

Fig 10. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 11).

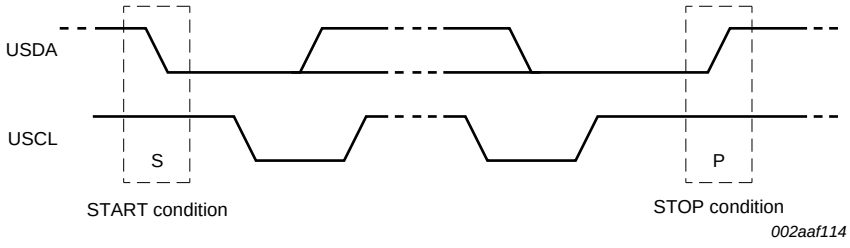

Fig 11. Definition of START and STOP conditions

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8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 12).

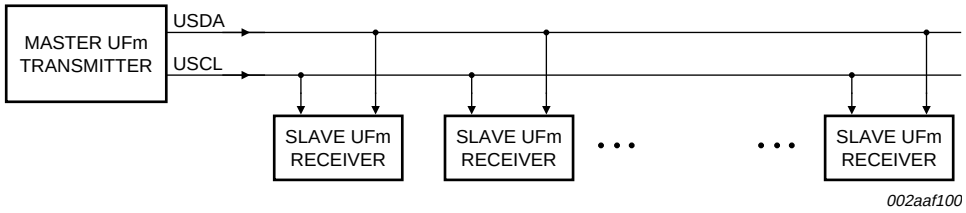

Fig 12. System configuration

8.3 Data transfer

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one bit that is always set to 1. The master generates an extra related clock pulse.

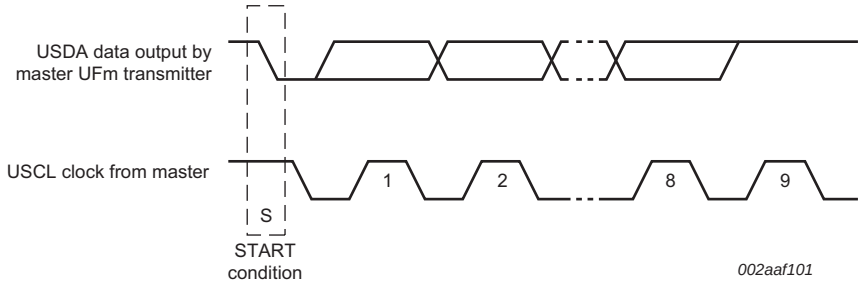

Fig 13. Data transfer

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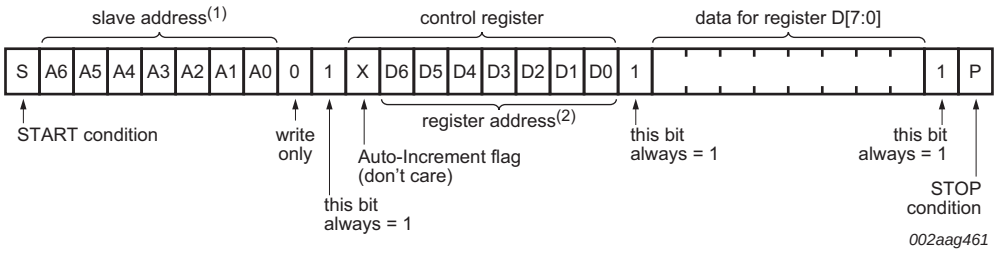
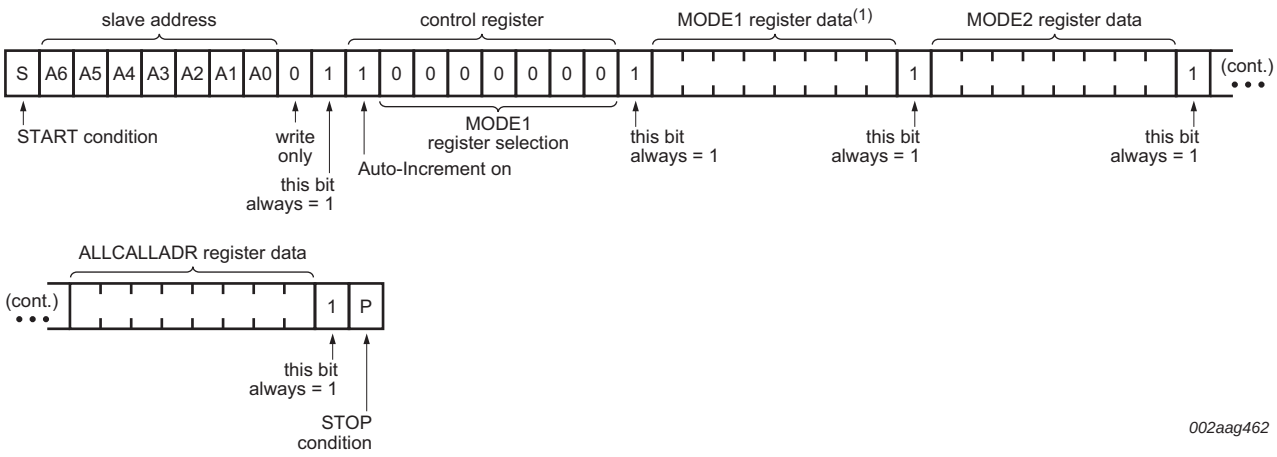
9. Bus transactions



(1) See Table 5 for I²C-bus slave address.

(2) See Table 7 for register definition.

Fig 14. Write to a specific register



(1) AI1, AI0 = 00. See Table 6 for Auto-Increment options.

Remark: Care should be taken to load the appropriate value here in the AI1 and AI0 bits of the MODE1 register for programming the part with the required Auto-Increment options.

Fig 15. Write to all registers using the Auto-Increment feature

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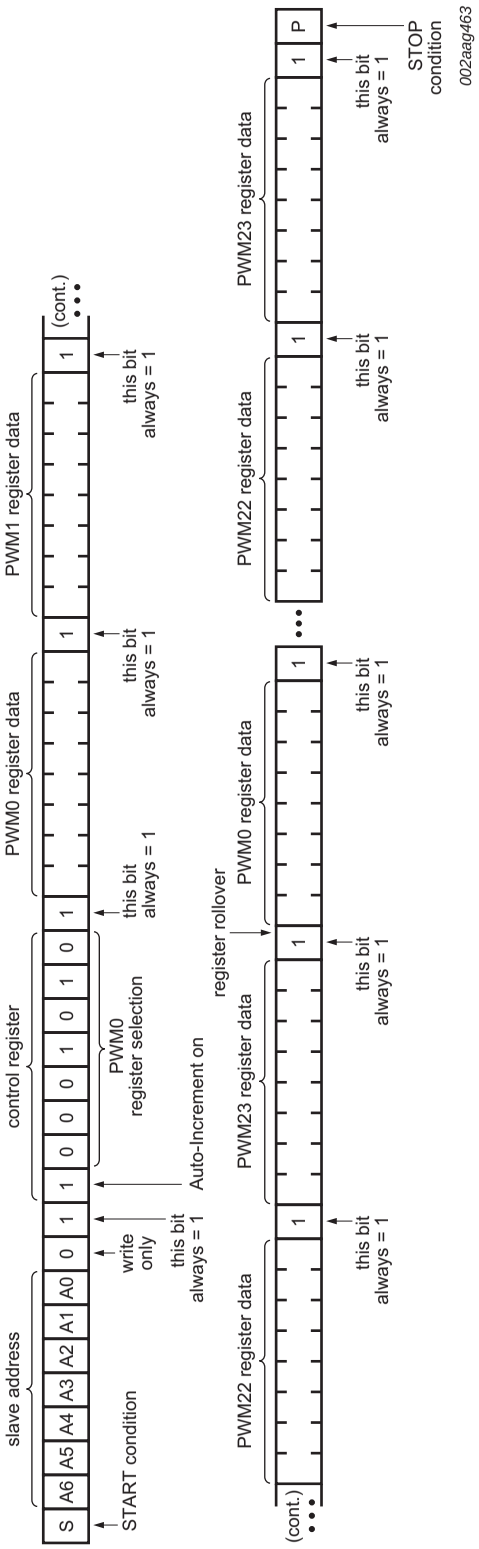
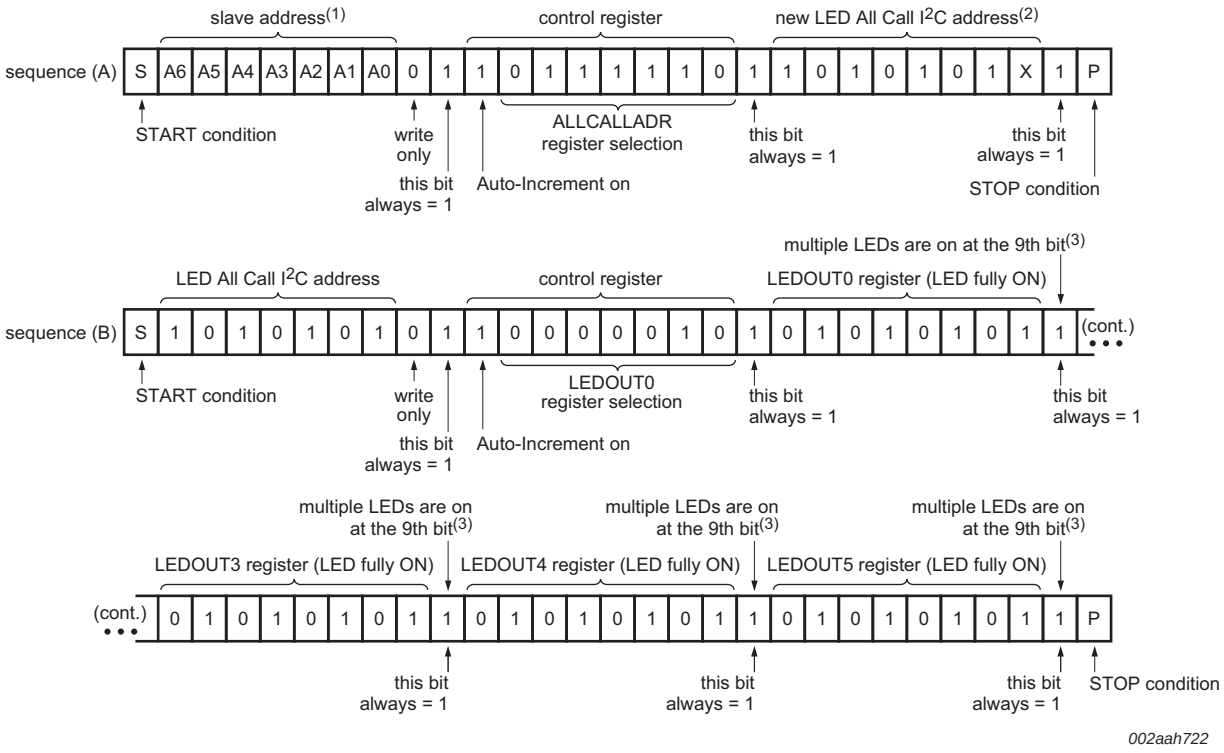

slave address
control register
PWM1 register data
PWM0 register data
PWM23 register data
PWM22 register data
S
A6
A5
A4
A3
A2
A1
A0
0
1
1
0
0
0
1
0
1
0
1
0
1
1
1



(1) In this example, several PCU9956As are used and the same sequence (A) (above) is sent to each of them.

(2) ALLCALL bit in MODE1 register is previously set to 1 for this example.

(3) OCH bit in MODE2 register is previously set to 1 for this example.

Fig 17. LED All Call I²C-bus address programming and LED All Call sequence example

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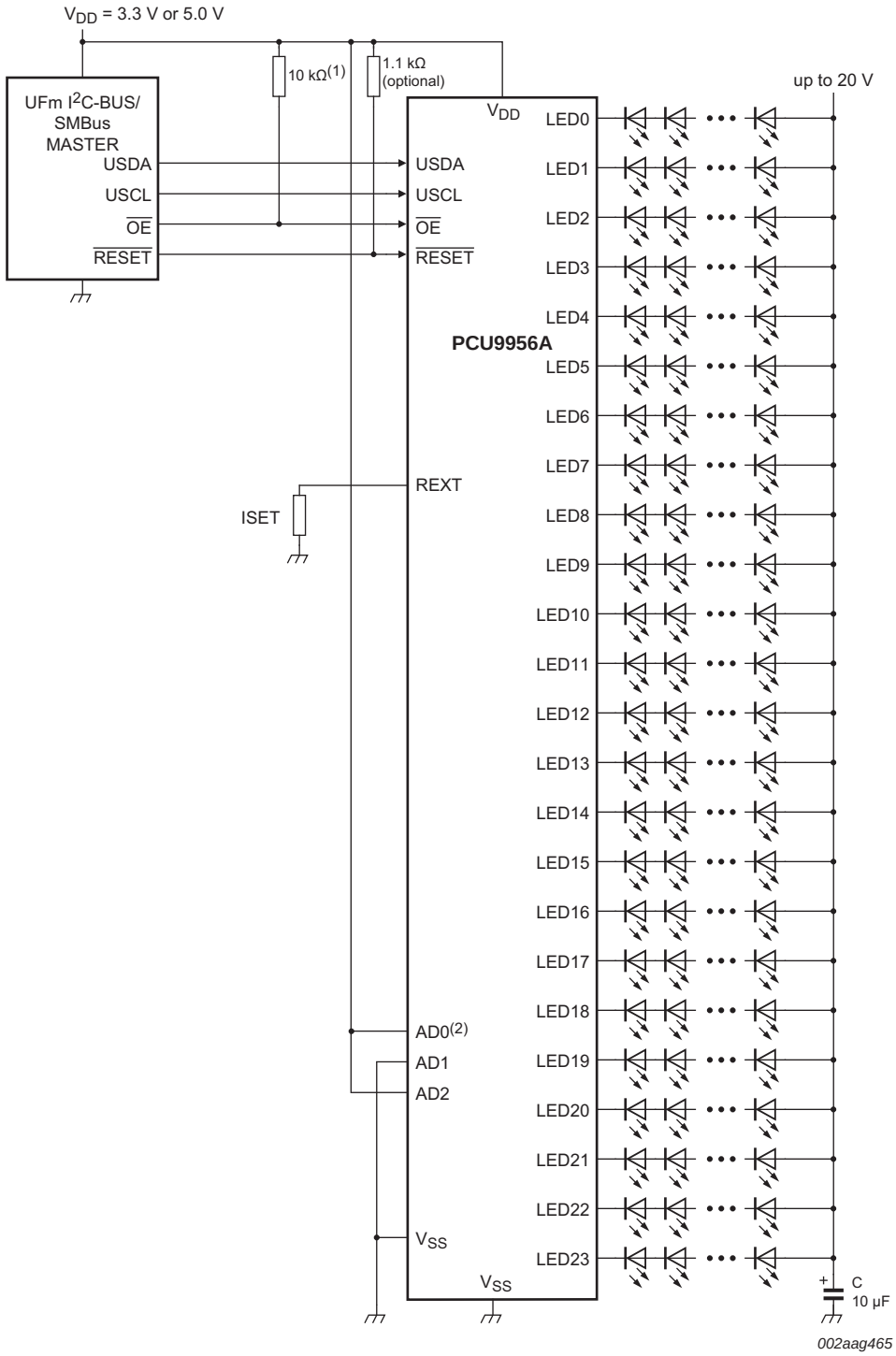
10. Application design-in information



(1) $\overline{OE}$ requires pull-up resistor if control signal from the master is open-drain.

(2) I²C-bus address = 1101001 when AD0, AD2 tied to V_{DD} and AD1 tied to V_{SS} (see Table 5).

Fig 18. Typical application

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10.1 Thermal considerations

Since the PCU9956A device integrates 24 linear current sources, thermal considerations should be taken into account to prevent overheating, which can cause the device to go into thermal shutdown.

Perhaps the major contributor for device's overheating is the LED forward voltage mismatch. This is because it can cause significant voltage differences between the LED strings of the same type (e.g., 2 V to 3 V), which ultimately translates into higher power dissipation in the device. The voltage drop across the LED channels of the device is given by the difference between the supply voltage and the LED forward voltage of each LED string. Reducing this to a minimum (e.g., 0.8 V) helps to keep the power dissipation down. Therefore LEDs binning is recommended to minimize LED voltage forward variation and reduce power dissipation in the device.

In order to ensure that the device will not go into thermal shutdown when operating under certain application conditions, its junction temperature (T_j) should be calculated to ensure that is below the overtemperature threshold limit (130 °C). The T_j of the device depends on the ambient temperature (T_{amb}), device's total power dissipation (P_{tot}), and thermal resistance.

The device junction temperature can be calculated by using the following equation:

$$T_j = T_{amb} + R_{th(j\text{-}a)} \times P_{tot} \quad (6)$$

where:

T_j = junction temperature

T_{amb} = ambient temperature

$R_{th(j\text{-}a)}$ = junction to ambient thermal resistance

P_{tot} = (device) total power dissipation

An example of this calculation is show below:

Conditions:

T_{amb} = 50 °C

$R_{th(j\text{-}a)}$ = 33.9 °C/W (per JEDEC 51 standard for multilayer PCB)

I_{LED} = 30 mA / channel

$I_{DD(max)}$ = 20 mA

V_{DD} = 5 V

LEDs per channel = 5 LEDs / channel

LED $V_{F(typ)}$ = 3 V per LED (15 V total for 5 LEDs in series)

LED V_F mismatch = 0.2 V per LED (1 V total for 5 LEDs in series)

$V_{reg(drv)}$ = 0.8 V (This will be present only in the LED string with the highest LED forward voltage.)

V_{sup} = LED $V_{F(typ)}$ + LED V_F mismatch + $V_{reg(drv)}$ = 15 V + 1 V + 0.8 V = 16.8 V

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P_{tot} calculation:

P_{tot} = IC_power + LED drivers_power;

IC_power = ($I_{DD} \times V_{DD}$)

IC_power = (0.02 A × 5 V) = 0.1 W

LED drivers_power = [(24 − 1) × (I_{LED}) × (LED V_F mismatch + $V_{reg(drv)}$)] + ($I_{LED} \times V_{reg(drv)}$)

LED drivers_power = [23 × 0.03 A × (1 V + 0.8 V)] + (0.03 A × 0.8 V)] = 1.266 W

P_{tot} = 0.1 W + 1.266 W = 1.366 W

T_j calculation:

$T_j = T_{amb} + R_{th(j-a)} \times P_{tot}$

T_j = 50 °C + (33.9 °C/W × 1.366 W) = 96.31 °C

This confirms that the junction temperature is below the minimum overtemperature threshold of 130 °C, which ensures the device will not go into thermal shutdown under these conditions.

It is important to mention that the value of the thermal resistance junction-to-ambient ($R_{th(j-a)}$) strongly depends in the PCB design. Therefore, the thermal pad of the device should be attached to a big enough PCB copper area to ensure proper thermal dissipation (similar to JEDEC 51 standard). Several thermal vias in the PCB thermal pad should be used as well to increase the effectiveness of the heat dissipation (for example, 15 thermal vias). The thermal vias should be distributed evenly in the PCB thermal pad.

Finally, it is important to point out that this calculation should be taken as a reference only and therefore evaluations should still be performed under the application environment and conditions to confirm proper system operation.

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11. Limiting values

Table 20. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin			V_{SS} − 0.5	5.5	V
$V_{drv(LED)}$	LED driver voltage			V_{SS} − 0.5	20	V
$I_{O(LEDn)}$	output current on pin LEDn			-	65	mA
I_{SS}	ground supply current			-	2.5	A
P_{tot}	total power dissipation	T_{amb} = 25 °C		-	2.95	W
		T_{amb} = 85 °C		-	1.18	W
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature	operating		–40	+85	°C
T_j	junction temperature			–40	+125	°C

12. Thermal characteristics

Table 21. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HTSSOP38	[1]	33.9	°C/W

[1] Per JEDEC 51 standard for multilayer PCB and wind speed (nm/s) = 0.

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13. Static characteristics

Table 22. Static characteristics

V_{DD} = 3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply							
V_{DD}	supply voltage			3	-	5.5	V
I_{DD}	supply current	on pin V_{DD}; operating mode; f_{SCL} = 1 MHz					
		R_{ext} = 2 kΩ; LED[23:0] = off; IREFx = 00h		-	11	12	mA
		R_{ext} = 1 kΩ; LED[23:0] = off; IREFx = 00h		-	13	14	mA
		R_{ext} = 2 kΩ; LED[23:0] = on; IREFx = FFh		-	15	19	mA
		R_{ext} = 1 kΩ; LED[23:0] = on; IREFx = FFh		-	17	21	mA
I_{stb}	standby current	on pin V_{DD}; no load; f_{SCL} = 0 Hz; MODE1[4] = 1; $V_I = V_{DD}$					
		V_{DD} = 3.3 V		-	100	600	µA
		V_{DD} = 5.5 V		-	100	700	µA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS}		-	2	-	V
V_{PDR}	power-down reset voltage	no load; $V_I = V_{DD}$ or V_{SS}	[2]	-	1	-	V
Inputs USCL, USDA							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}		−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$		-	6	10	pF
Current controlled outputs (LED[23:0])							
$I_{O(LEDn)}$	output current on pin LEDn	V_O = 0.8 V; IREFx = 80h; R_{ext} = 1 kΩ		25	-	30	mA
		V_O = 0.8 V; IREFx = FFh; R_{ext} = 1 kΩ		50	-	60	mA
ΔI_O	output current variation	V_{DD} = 3.0 V; T_{amb} = 25 °C; V_O = 0.8 V; IREFx = 80h; R_{ext} = 1 kΩ; guaranteed by design					
		between bits (different ICs, same channel)	[3]	-	-	±6	%
		between bits (2 channels, same IC)	[4]	-	-	±4	%
$V_{reg(drv)}$	driver regulation voltage	minimum regulation voltage; IREFx = FFh; R_{ext} = 1 kΩ		0.8	1	20	V
$I_{L(off)}$	off-state leakage current	V_O = 20 V		-	-	1	µA
$\overline{OE}$ input, $\overline{RESET}$ input							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
I_{LI}	input leakage current			−1	-	+1	µA
C_i	input capacitance			-	3.7	5	pF

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Table 22. Static characteristics *...continued*

V_{DD} = 3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Address inputs AD2, AD1, AD0							
V_I	input voltage	voltage on an input pin		−0.5	-	+5.5	V
I_{LI}	input leakage current			−1	-	+1	μA
C_i	input capacitance			-	3.7	5	pF
Overtemperature protection							
$T_{th(otp)}$	overtemperature protection threshold temperature	rising		130	-	150	°C
		hysteresis		15	-	30	°C

[1] Typical limits at V_{DD} = 3.3 V, T_{amb} = 25 °C.

[2] V_{DD} must be lowered to 0.8 V in order to reset part.

[3] Part-to-part mismatch is calculated:

$$\Delta\% = \left(\frac{\left(\frac{I_{O(LED0)} + I_{O(LED1)} + \ldots + I_{O(LED22)} + I_{O(LED23)}}{24} - ideal\ output\ current\right)}{ideal\ output\ current}\right) \times 100$$

where 'ideal output current' = 28.68 mA (R_{ext} = 1 kΩ, IREFx = 80h).

[4] Channel-to-channel mismatch is calculated:

$$\Delta\% = \left(\frac{I_{O(LEDn)}\ (\text{where n} = 0 \text{ to } 23)}{\left(\frac{I_{O(LED0)} + I_{O(LED1)} + \ldots + I_{O(LED22)} + I_{O(LED23)}}{24}\right)} - 1\right) \times 100$$

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14. Dynamic characteristics

Table 23. Dynamic characteristics

All the timing limits are valid within the operating supply voltage and ambient temperature range; V_{DD} = 3 V ± 0.2 V and 5.5 V ± 0.3 V; T_{amb} = −40 °C to +85 °C; and refer to V_{IL} and V_{IH} with an input voltage of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{USCL}	USCL clock frequency		[1]	0	-	5000	kHz
t_{BUF}	bus free time between a STOP and START condition			0.08	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.05	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.05	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.05	-	-	µs
$t_{HD;DAT}$	data hold time			10	-	-	ns
$t_{VD;DAT}$	data valid time		[2]	-	-	-	ns
$t_{SU;DAT}$	data set-up time			30	-	-	ns
t_{LOW}	LOW period of the USCL clock			50	-	-	ns
t_{HIGH}	HIGH period of the USCL clock			50	-	-	ns
t_f	fall time of both USDA and USCL signals			-	-	50	ns
t_r	rise time of both USDA and USCL signals			-	-	50	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	-	10	ns

[1] Minimum USCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either USDA or USCL is held LOW for a minimum of 25 ms. Disable bus time-out feature for DC operation.

[2] $t_{VD;DAT}$ is not applicable to the UFm I²C-bus slave device.

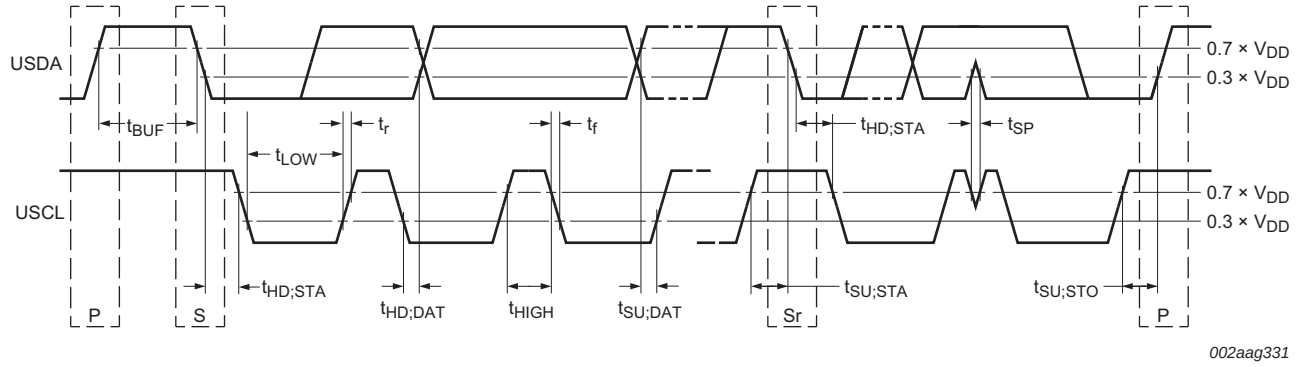

Fig 19. Definition of timing

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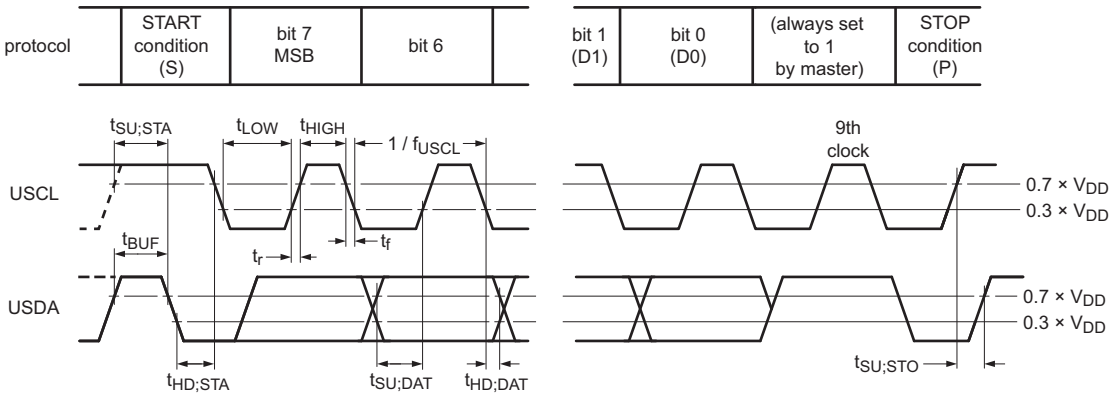
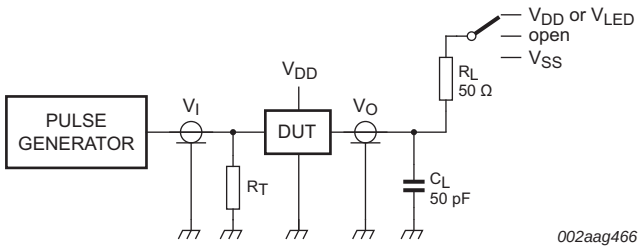


Rise and fall times refer to V_{IL} and V_{IH}.

Fig 20. UFm I²C-bus timing diagram

15. Test information



R_L = Load resistor for LEDn.

C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generators.

Fig 21. Test circuitry for switching times

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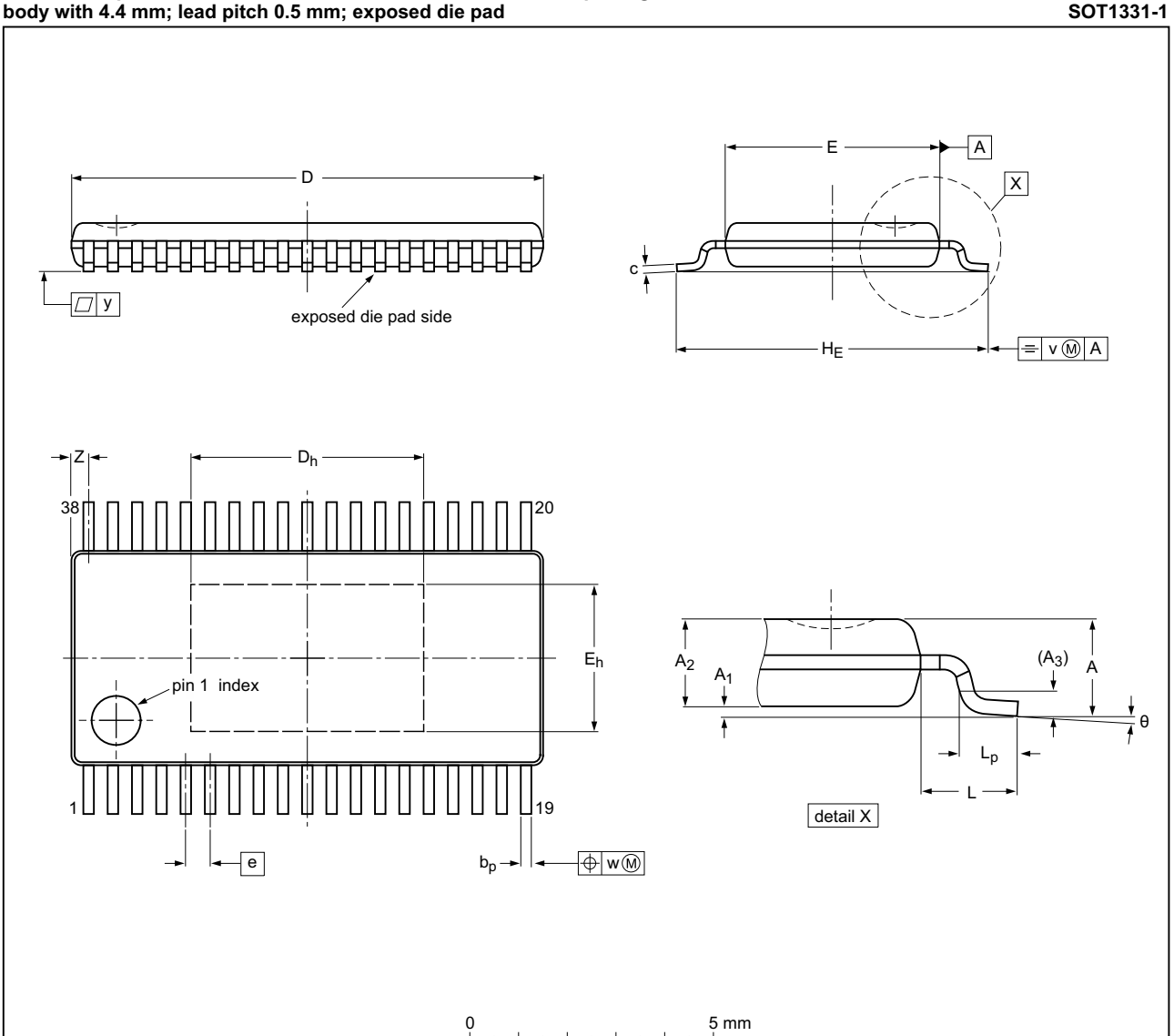
16. Package outline

HTSSOP38: plastic thermal enhanced thin shrink small outline package; 38 leads; body with 4.4 mm; lead pitch 0.5 mm; exposed die pad **SOT1331-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	A_3	b_p	c	D[1]	D_h	E[1]	E_h	e	H_e	L	L_p	v	w	y	Z	θ
	max	1.1	0.15	0.95		0.27	0.20	9.8	4.9	4.5	3.1				0.7				0.49	8°
mm	nom		0.10	0.90	0.25	0.21	0.15	9.7	4.8	4.4	3.0	0.5	6.4	1.0	0.6	0.2	0.08	0.08	0.35	4°
	min		0.05	0.85		0.17	0.09	9.6	4.7	4.3	2.9				0.5				0.21	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot1331-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1331-1						~~12-07-30~~ 12-08-20

Fig 22. Package outline SOT1331-1 (HTSSOP38)

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17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

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- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 23) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 24 and 25

Table 24. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 25. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 23.

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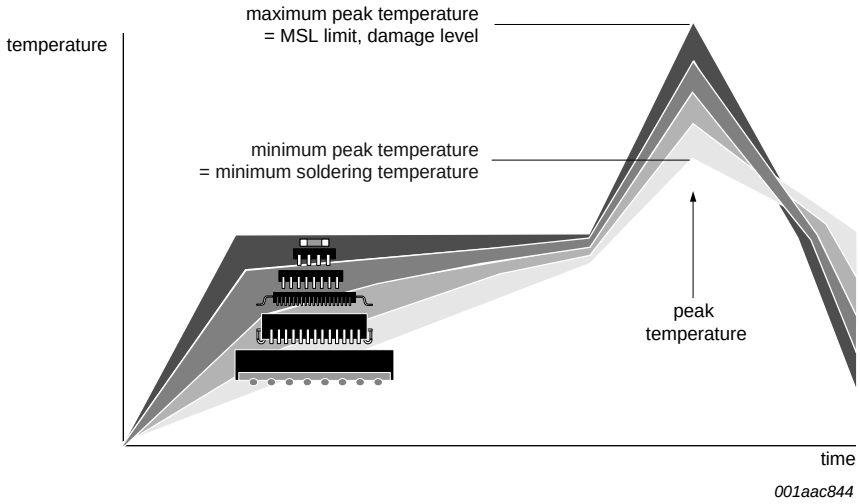

MSL: Moisture Sensitivity Level

Fig 23. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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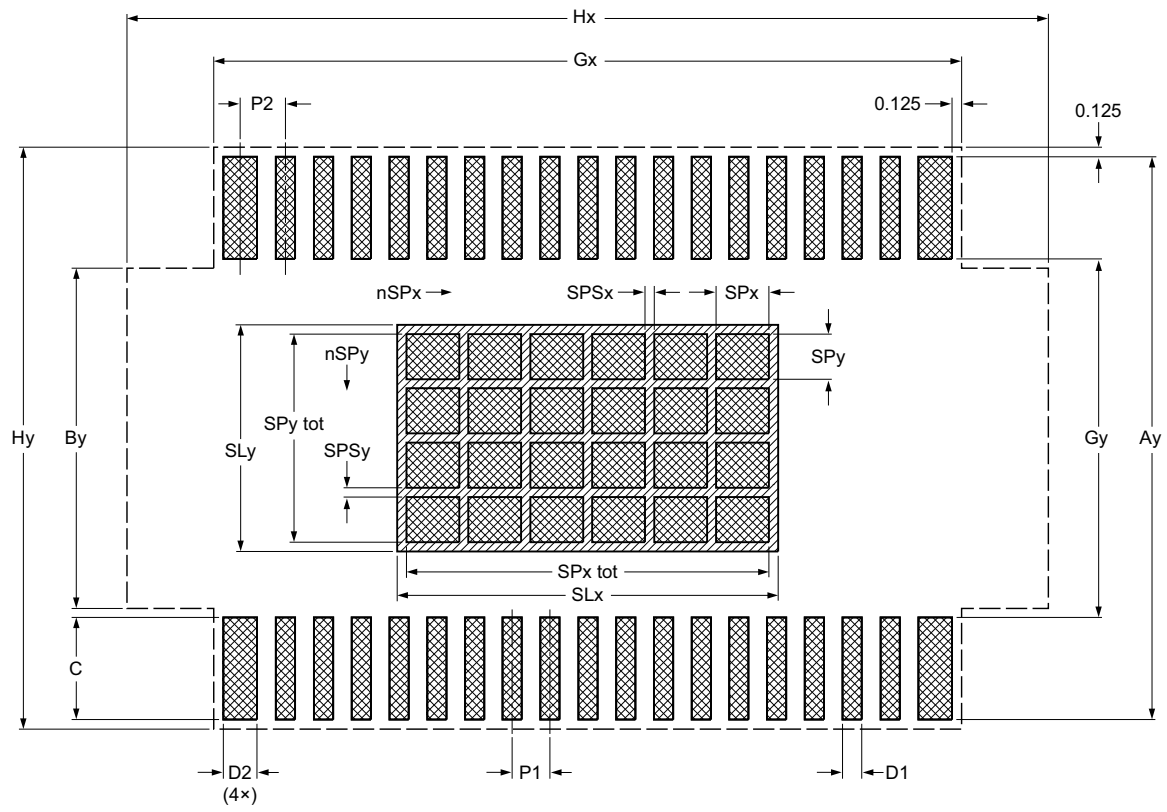
19. Soldering: PCB footprints

Footprint information for reflow soldering of HTSSOP38 package **SOT1331-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

solder land plus solder paste

occupied area

SPSx	SPSy	SPx tot	SPy tot
0.12	0.12	4.8	2.76

Dimensions in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy	nSPx	nSPy	SLx	SLy	SPx	SPy
0.5	0.6	7.45	4.5	1.35	0.25	0.45	9.9	4.75	12.2	7.7	6	4	5.040	3	0.7	0.6

Issue date ~~13-11-15~~ 14-01-20 *sot1331-1_fr*

Fig 24. PCB footprint for SOT1331-1 (HTSSOP38); reflow soldering

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20. Abbreviations

Table 26. Abbreviations

Acronym	Description
ACK	Acknowledge
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
LED	Light Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
NMOS	Negative-channel Metal-Oxide Semiconductor
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal-Oxide Semiconductor
PWM	Pulse Width Modulation
RGB	Red/Green/Blue
RGBA	Red/Green/Blue/Amber
SMBus	System Management Bus

21. Revision history

Table 27. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCU9956A v.2.1	20150629	Product data sheet	-	PCU9956A v.2
Modifications:	• Section 7.3.3 “LEDOUT0 to LEDOUT5, LED driver output state”: added remark. • Table 8 “MODE1 - Mode register 1 (address 00h) bit description”: Added Table note [3].			
PCU9956A v.2	20141014	Product data sheet	-	PCU9956A v.1
Modifications:	• Section 7.5 “Power-on reset”: added remark.			
PCU9956A v.1	20140124	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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