

PMN38EN

N-channel TrenchMOS logic level FET

Rev. 02 — 3 October 2007

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features

- Logic level threshold
- Surface-mounted package
- Low threshold voltage
- Very fast switching

1.3 Applications

- Battery powered motor control
- High speed switch in set top box power supplies
- Driver FET in DC-to-DC converters
- Load switch in notebook computers

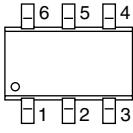
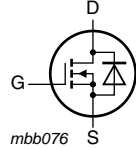
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	30	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 and 3	-	-	5.4	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 2	-	-	1.75	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 2.8\text{ A}$; $T_j = 25\text{ °C}$; see Figure 8 and 9	-	38	46	m Ω

2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic Symbol
1	D	drain	 <p>SOT457 (TSOP6)</p>	 <p>mbb076 S</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMN38EN	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Limiting values

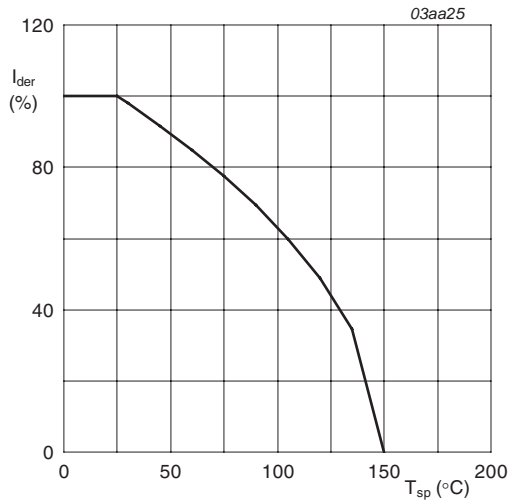
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{sp} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	3.4	A
		$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 and 3	-	5.4	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed; see Figure 3	-	21.6	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 2	-	1.75	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C

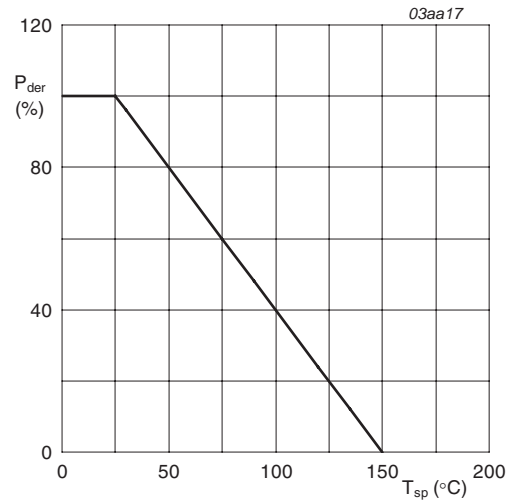
Source-drain diode

I_S	source current	$T_{sp} = 25\text{ °C}$	-	1.45	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; $t_p = 10\text{ }\mu\text{s}$; pulsed	-	5.8	A



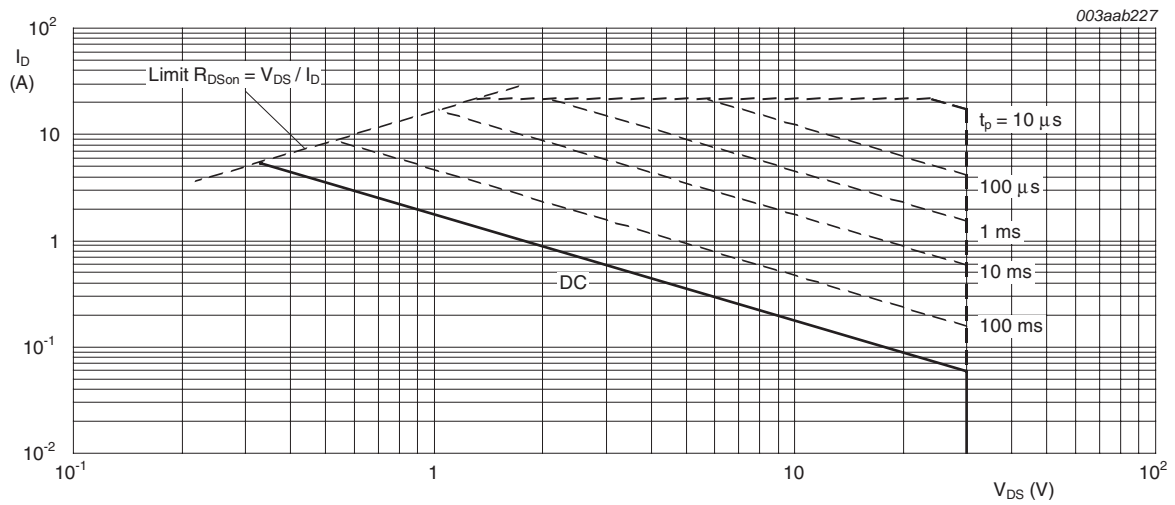
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$T_{sp} = 25^\circ\text{C}$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	[1] -	-	70	K/W

[1] Mounted on a metal clad board

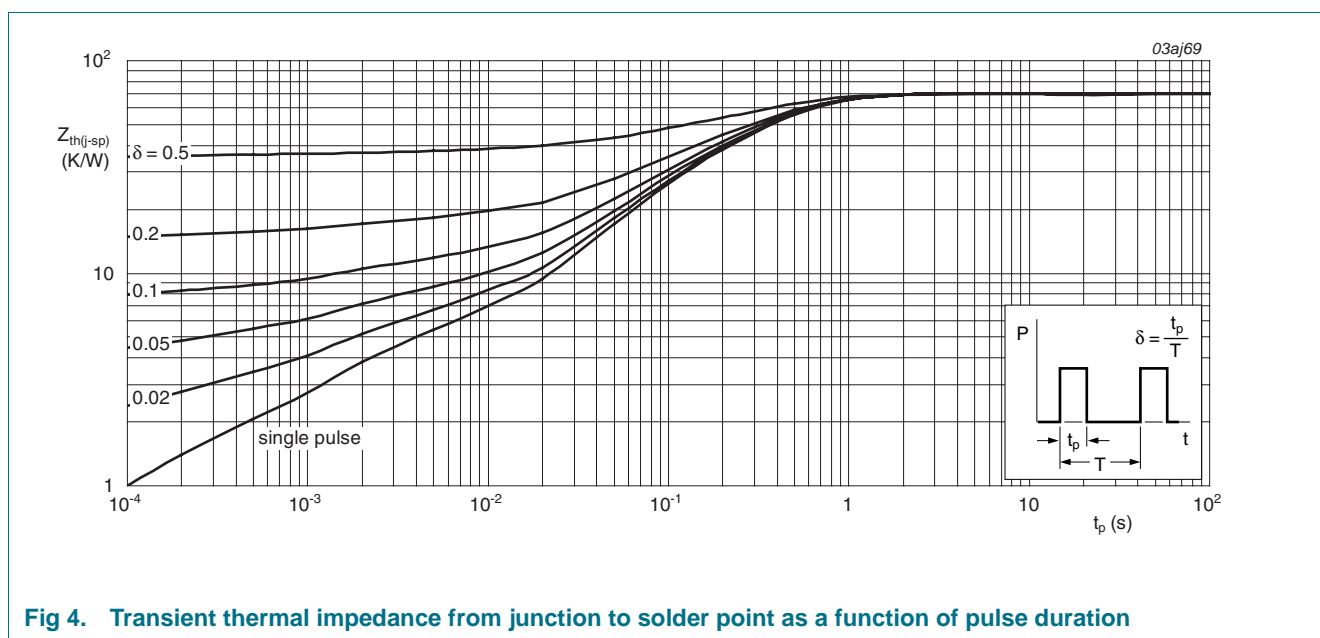


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$	0.6	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$	-	-	2.2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 7	1	1.5	2	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.01	0.1	μA
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	10	μA

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{GSS}	gate leakage current	V _{GS} = +20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 3 A; T _j = 150 °C	-	49.6	60.9	mΩ
		V _{GS} = 4.5 V; I _D = 2.8 A; T _j = 25 °C; see Figure 8 and 9	-	38	46	mΩ
		V _{GS} = 10 V; I _D = 3 A; T _j = 25 °C; see Figure 8 and 9	-	31	38	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 5 A; V _{DS} = 15 V; V _{GS} = 4.5 V; T _j = 25 °C; see Figure 10 and 11	-	6.1	-	nC
Q _{GS}	gate-source charge	I _D = 5 A; V _{DS} = 15 V; V _{GS} = 4.5 V; T _j = 25 °C; see Figure 10 and 11	-	1.7	-	nC
Q _{GD}	gate-drain charge	I _D = 5 A; V _{DS} = 15 V; V _{GS} = 4.5 V; T _j = 25 °C; see Figure 10 and 11	-	2.35	-	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 12	-	495	-	pF
C _{oss}	output capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; see Figure 12	-	100	-	pF
C _{rss}	reverse transfer capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 12	-	70	-	pF
t _{d(on)}	turn-on delay time	R _{G(ext)} = 6 Ω; R _L = 12 Ω; V _{DS} = 15 V; V _{GS} = 4.5 V; T _j = 25 °C	-	14	-	ns
t _r	rise time	R _{G(ext)} = 6 Ω; R _L = 12 Ω; V _{DS} = 15 V; V _{GS} = 4.5 V; T _j = 25 °C	-	19	-	ns
t _{d(off)}	turn-off delay time	V _{DS} = 15 V; R _L = 12 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C	-	28	-	ns
t _f	fall time	R _{G(ext)} = 6 Ω; R _L = 12 Ω; V _{DS} = 15 V; V _{GS} = 4.5 V; T _j = 25 °C	-	16	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 1.7 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 13	-	0.75	1.2	V
t _{rr}	reverse recovery time	I _S = 2.3 A; dI _S /dt = 100 A/μs; V _{GS} = 0 V; V _{DS} = 30 V; T _j = 25 °C	-	22	-	ns

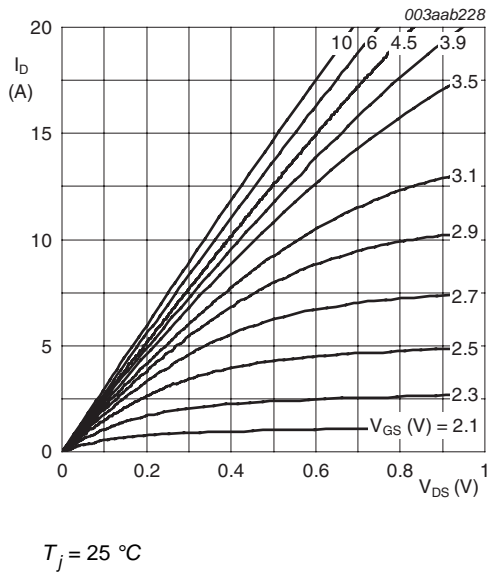


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

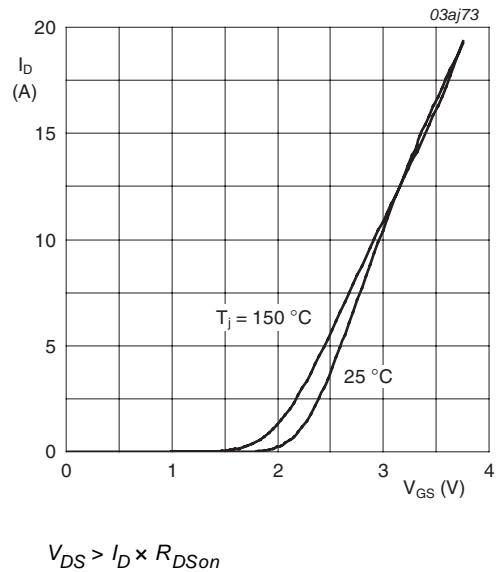


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

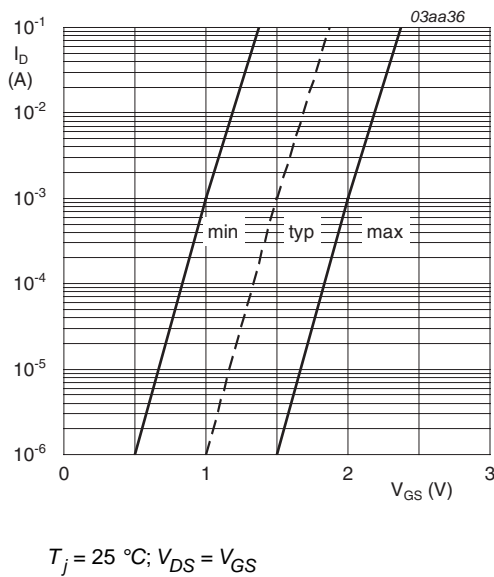


Fig 7. Sub-threshold drain current as a function of gate-source voltage

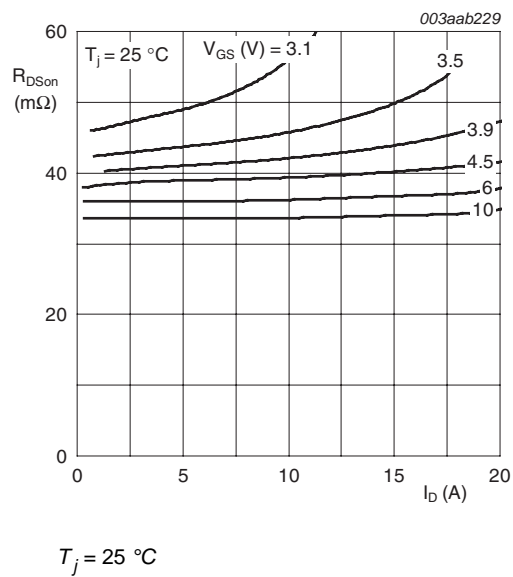
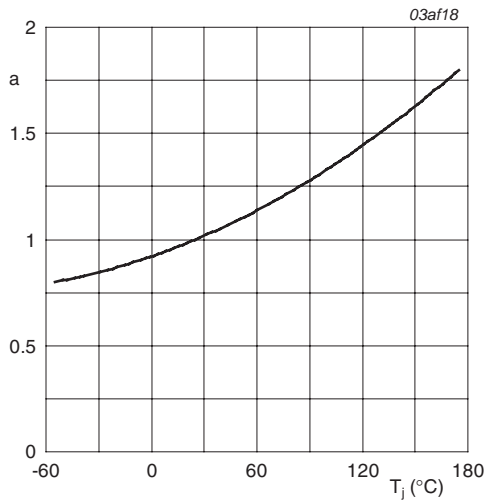
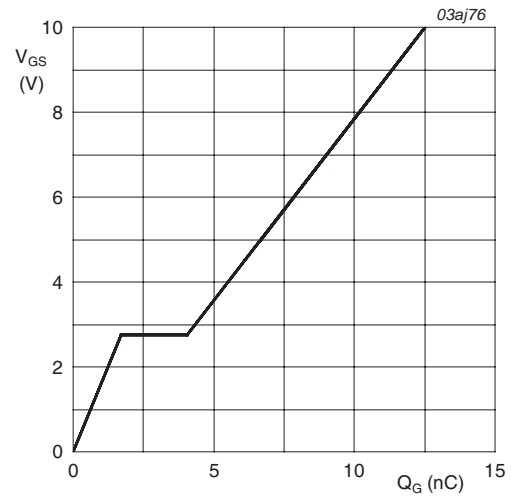


Fig 8. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



$I_D = 5 \text{ A}; T_j = 25^\circ\text{C}; V_{DS} = 15 \text{ V}$

Fig 10. Gate-source voltage as a function of gate charge; typical values

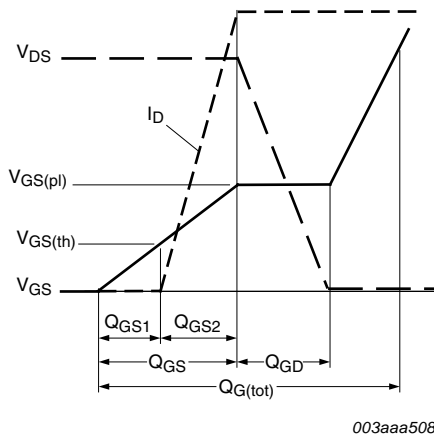
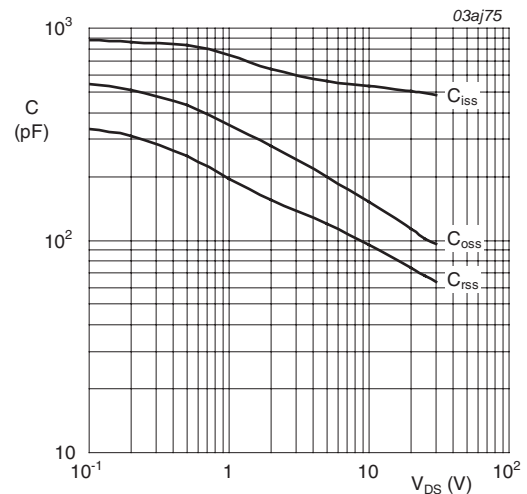
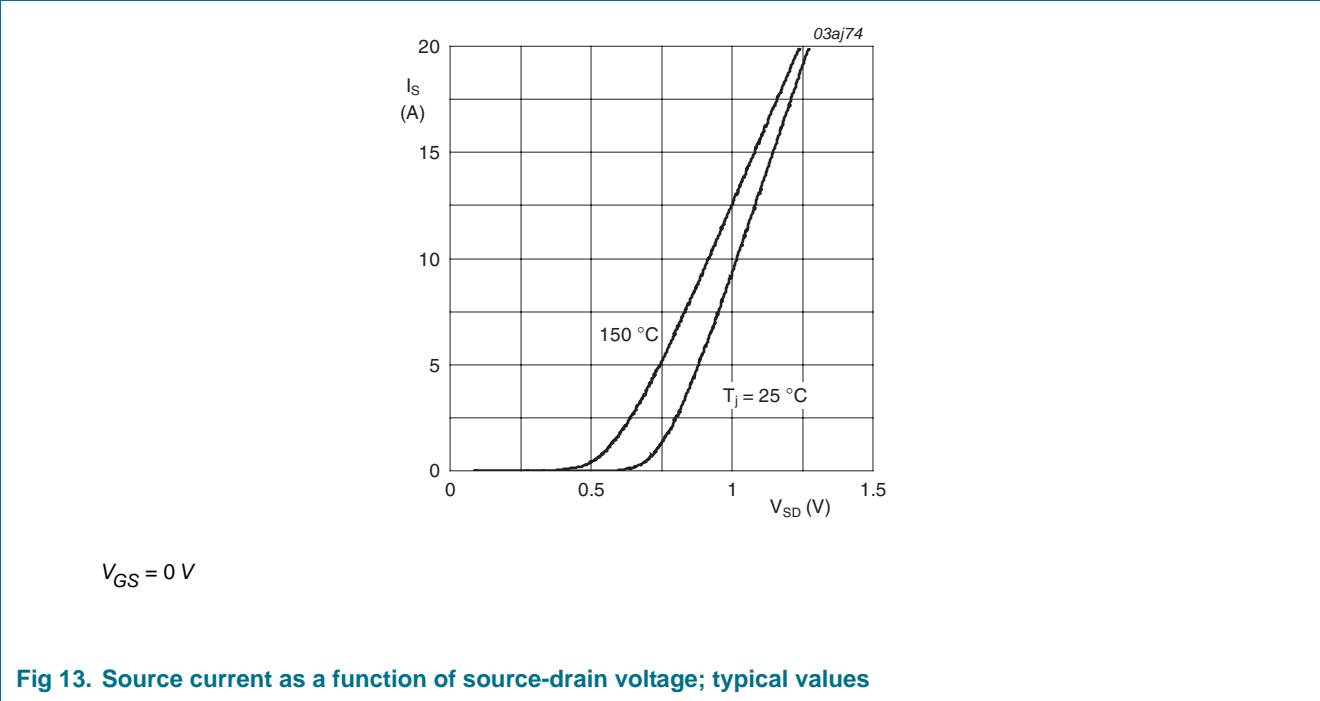


Fig 11. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



7. Package outline

Plastic surface-mounted package (TSOP6); 6 leads

SOT457

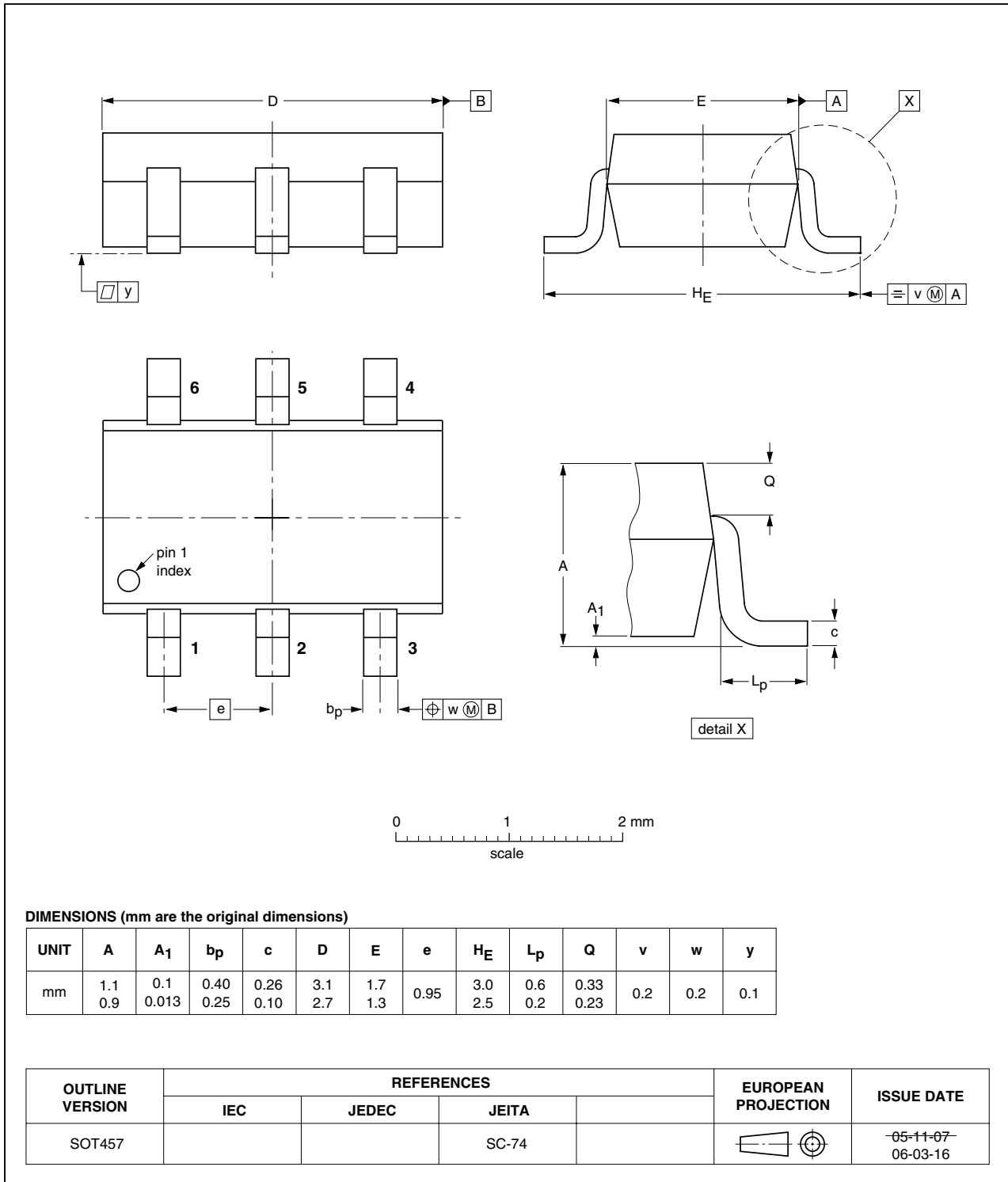


Fig 14. Package outline SOT457 (TSOP6)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMN38EN_2	20071003	Product data sheet	-	PMN38EN_1
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the company name where appropriate.			
PMN38EN_1	20060113	Product data sheet	-	-

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9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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