

# PSMN013-30LL

N-channel DFN3333-8 30 V 13 mΩ logic level MOSFET

Rev. 5 — 8 December 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel MOSFET in DFN3333-8 package qualified to 150 °C. This product is designed and qualified for use in a wide range of industrial, communications and power supply equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources
- Small footprint for compact designs

### 1.3 Applications

- Battery protection
- Load switching
- DC-to-DC converters
- Power ORing

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a>	-	-	21	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	41	W
$T_j$	junction temperature		-55	-	150	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C};$ see <a href="#">Figure 12</a>	-	15.5	19	mΩ
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 100\text{ °C};$ see <a href="#">Figure 13</a>	-	-	17.9	mΩ
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C};$ see <a href="#">Figure 12</a>	-	11	13	mΩ
$I_{DSS}$	drain leakage current	$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ °C}$	-	-	50	μA

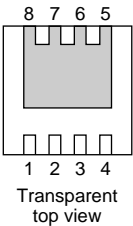
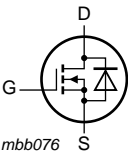


Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 8\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	1.7	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 8\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	6	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 40\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; unclamped; $R_{GS} = 50\text{ }\Omega$	-	-	13	mJ

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>Transparent top view</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
5,6,7,8	D	mounting base; connected to drain		

**SOT873-1 (DFN3333-8)**

## 3. Ordering information

Table 3. Ordering information

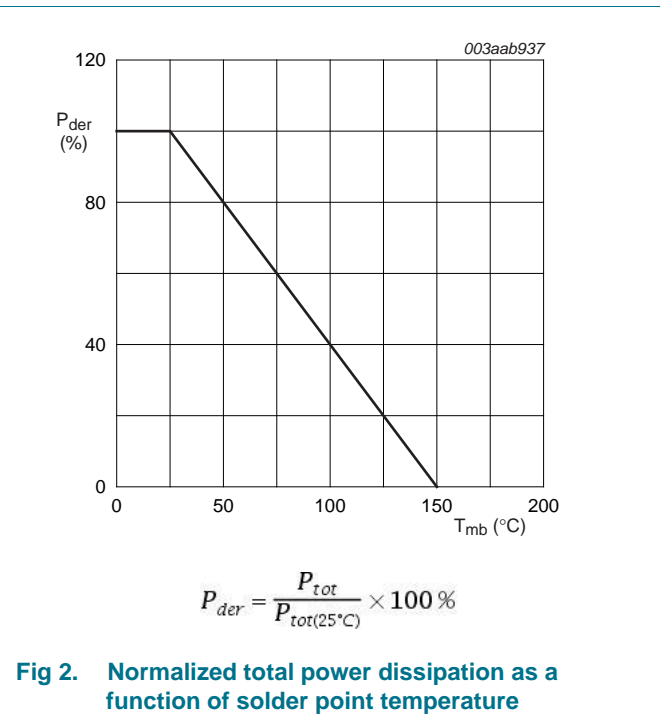
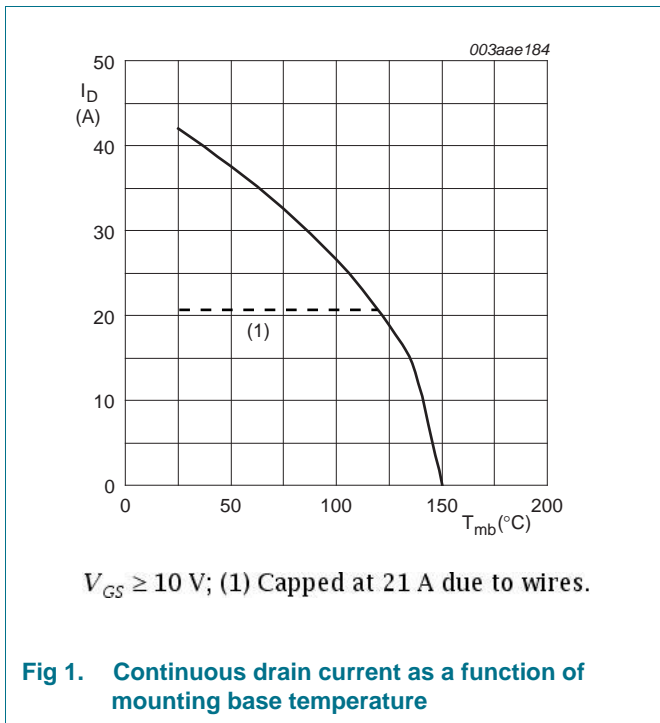
Type number	Package		Version
	Name	Description	
PSMN013-30LL	DFN3333-8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals	SOT873-1

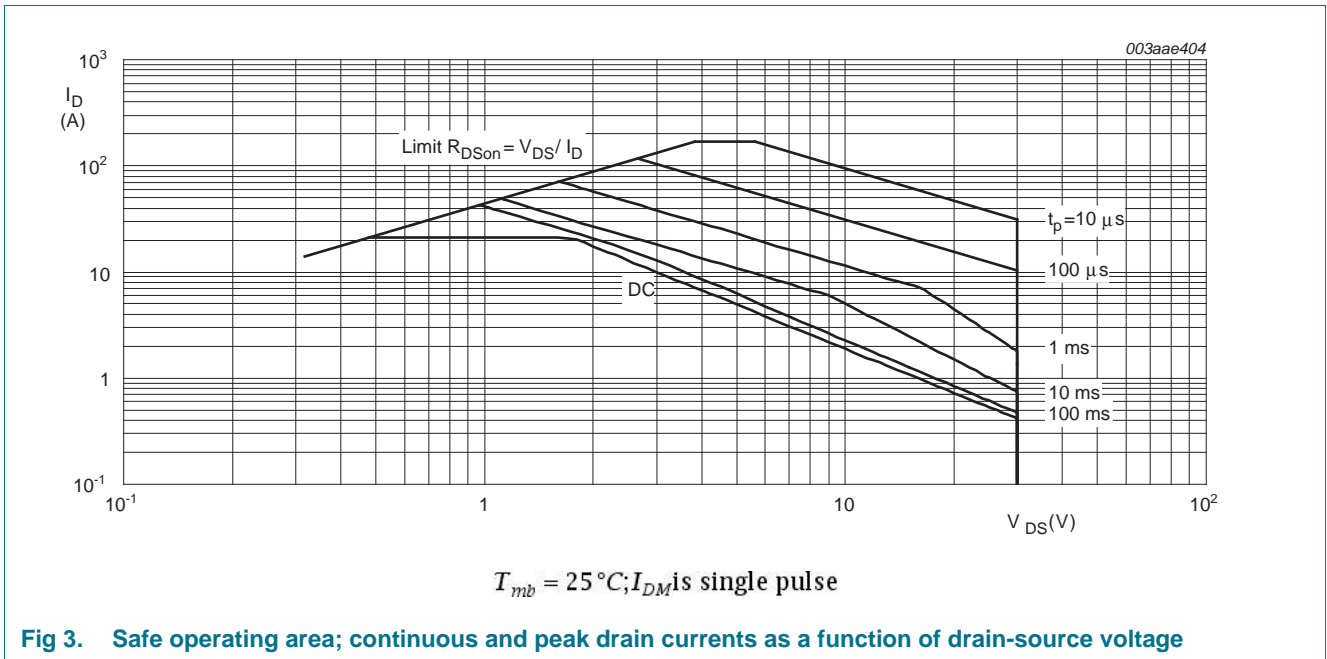
### 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C	-	30	V
V <sub>DGR</sub>	drain-gate voltage	T <sub>j</sub> ≤ 150 °C; T <sub>j</sub> ≥ 25 °C; R <sub>GS</sub> = 20 kΩ	-	30	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see <a href="#">Figure 1</a>	-	21	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 1</a>	-	21	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 3</a>	-	169	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	41	W
T <sub>stg</sub>	storage temperature		-55	150	°C
T <sub>j</sub>	junction temperature		-55	150	°C
T <sub>sld(M)</sub>	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	42	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	169	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 40 A; V <sub>sup</sub> ≤ 30 V; unclamped; R <sub>GS</sub> = 50 Ω	-	13	mJ





### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	2.8	6.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	56	60	K/W

[1]  $R_{th(j-a)}$  is guaranteed by design and assumes that the device is mounted on a 40mm x 40mm x 70 μm copper pad at 20°C ambient temperature. In practice  $R_{th(j-a)}$  will be determined by the customer's PCB characteristics

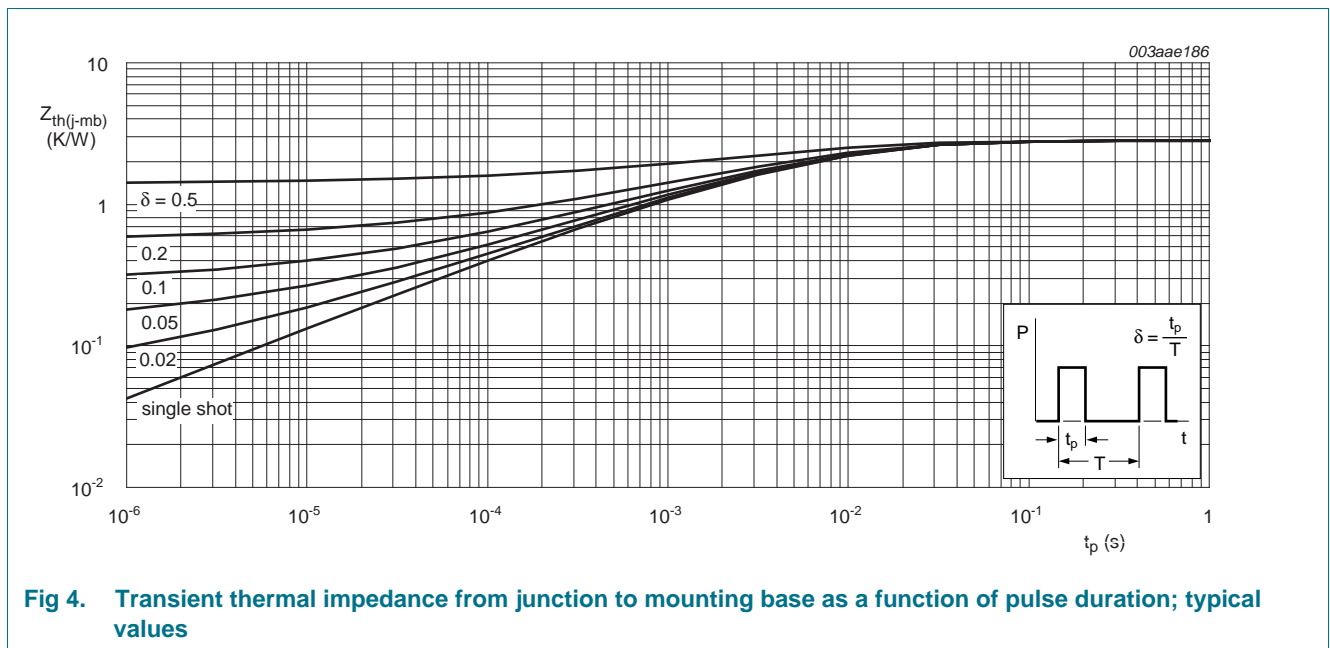


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a> ; see <a href="#">Figure 10</a>	1.3	1.7	2.15	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	-	2.55	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	50	μA
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	5	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	5	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	15.5	19	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	-	17.9	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	19.8	23.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	11	13	mΩ
$R_G$	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	1.37	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 8 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	12.2	-	nC
		$I_D = 8 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	6	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	11.4	-	nC
$Q_{GS}$	gate-source charge	$I_D = 8 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a>	-	2.3	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1.3	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 8 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	1.7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 8 \text{ A}; V_{DS} = 15 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	2.7	-	V
$C_{iss}$	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 16</a>	-	768	-	pF
$C_{oss}$	output capacitance		-	144	-	pF
$C_{riss}$	reverse transfer capacitance		-	67	-	pF

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 2\ \Omega; V_{GS} = 10\text{ V};$	-	13	-	ns
$t_r$	rise time	$R_{G(ext)} = 4.7\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	9	-	ns
$t_{d(off)}$	turn-off delay time		-	15	-	ns
$t_f$	fall time		-	5.1	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 17</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 8\text{ A}; di_S/dt = 100\text{ A}/\mu\text{s};$	-	20.7	-	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}$	-	10.6	-	nC

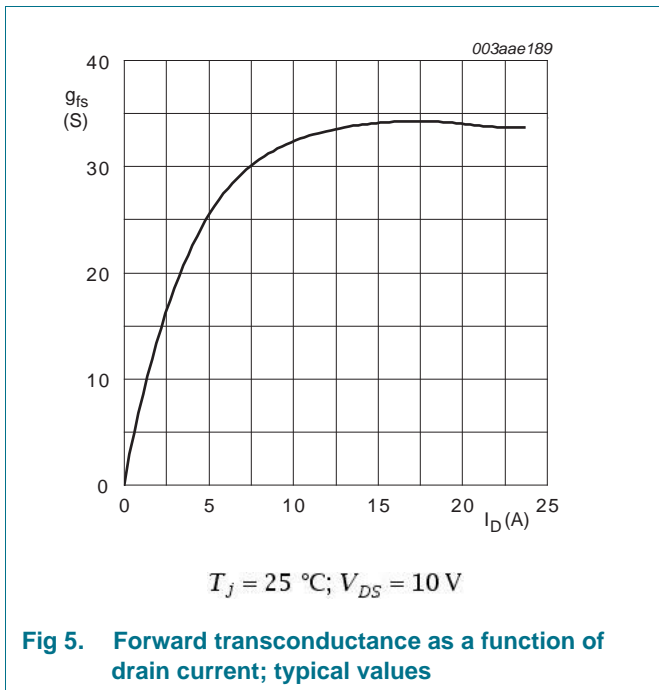


Fig 5. Forward transconductance as a function of drain current; typical values

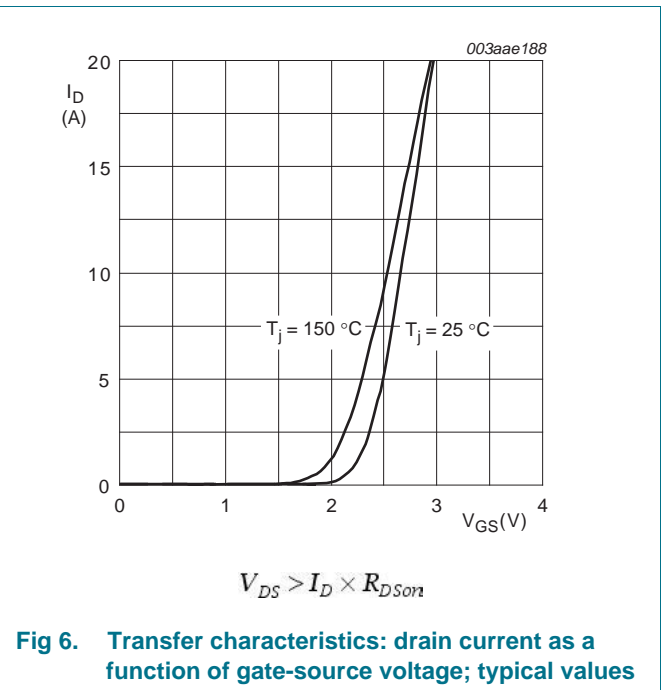
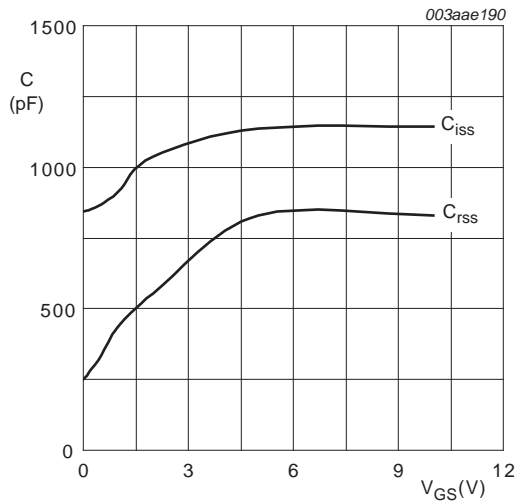
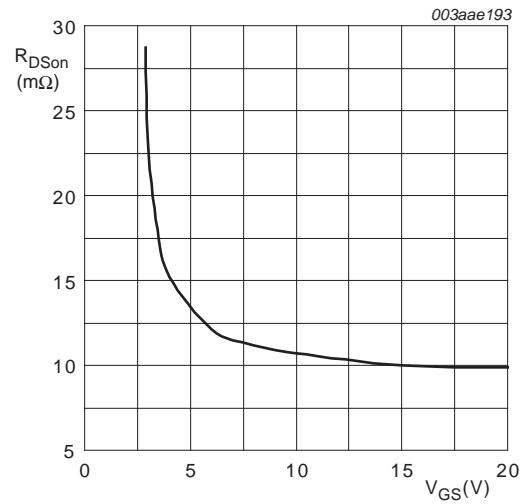


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



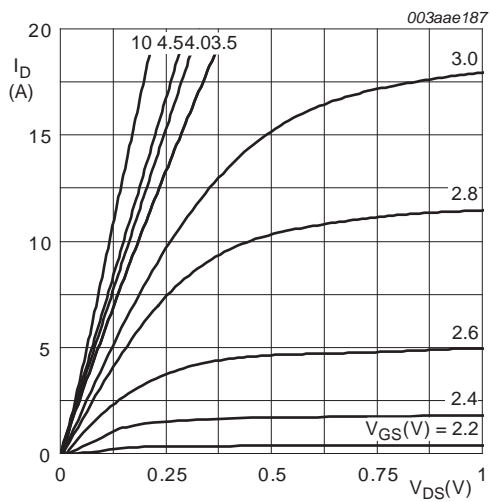
$V_{DS} = 0$  V;  $f = 1$  MHz

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage, typical values



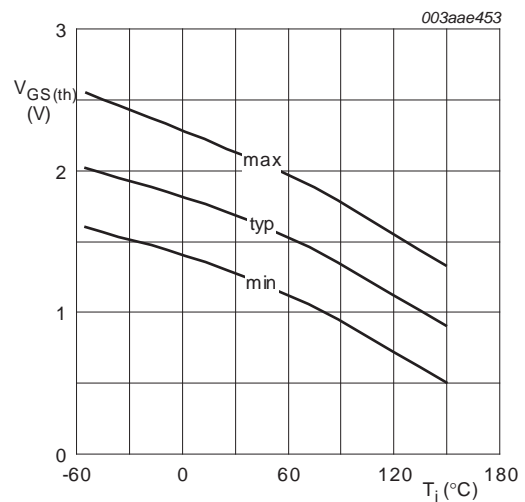
$T_j = 25$  °C;  $I_D = 8$  A

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



$T_j = 25$  °C

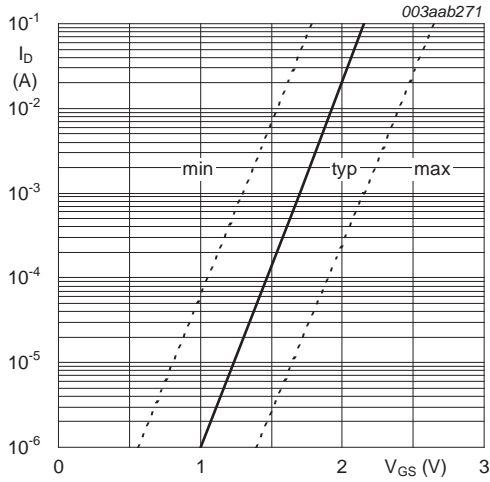
Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values



$I_D = 1$  mA;  $V_{DS} = V_{GS}$

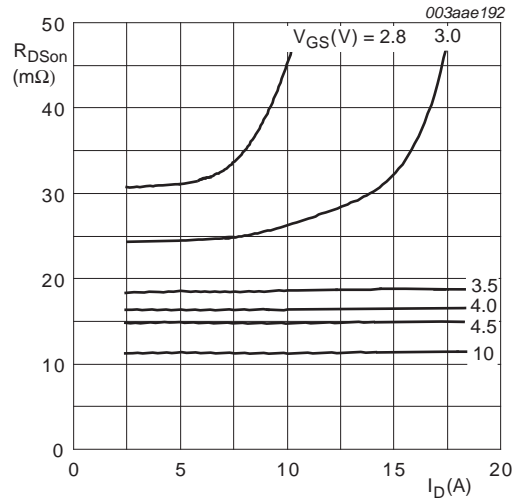
Fig 10. Gate-source threshold voltage as a function of junction temperature





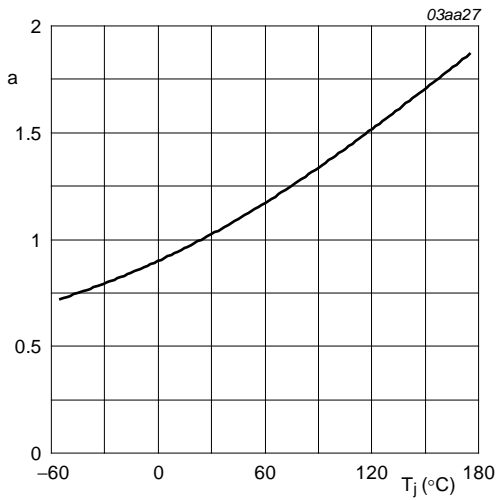
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25^\circ\text{C}$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

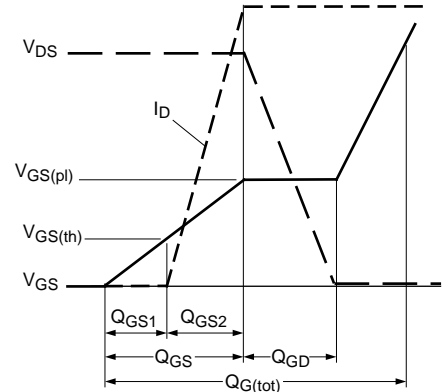
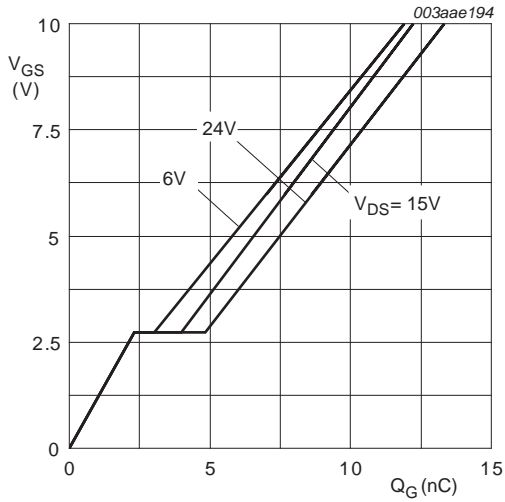
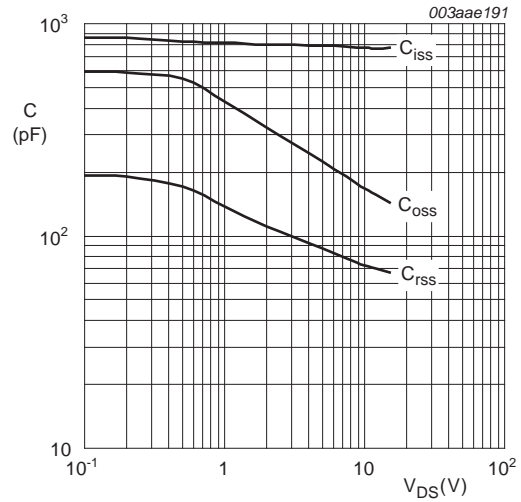


Fig 14. Gate charge waveform definitions



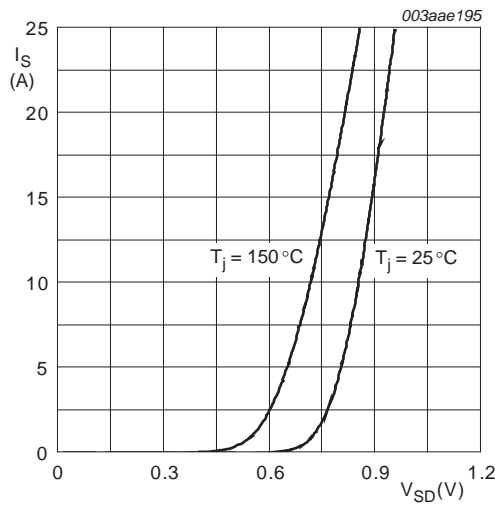
$T_j = 25\text{ °C}; I_D = 8\text{ A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

## 7. Package outline

DFN3333-8: plastic thermal enhanced very thin small outline package; no leads;  
8 terminals; body 3.3 x 3.3 x 1.0 mm

SOT873-1

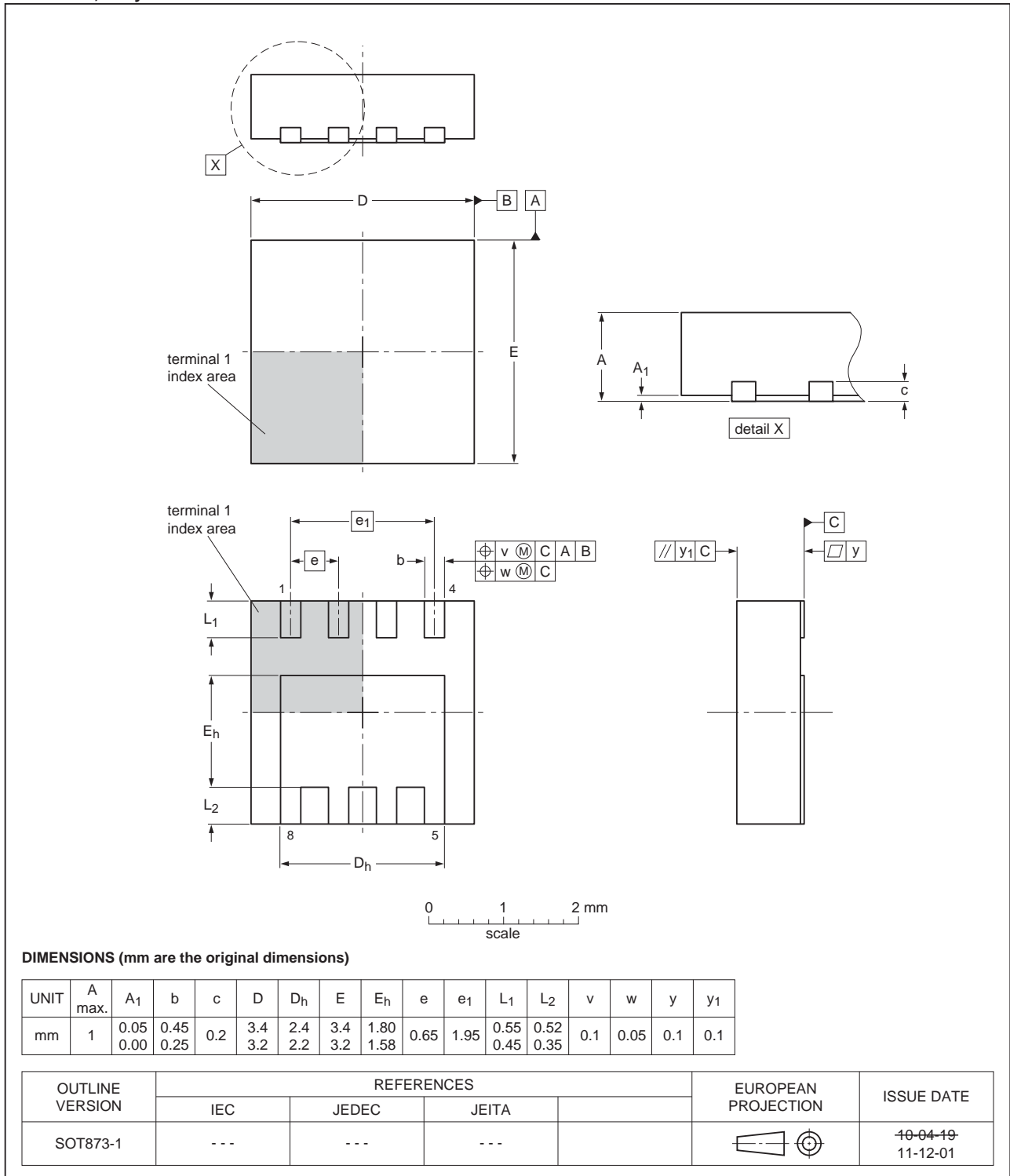


Fig 18. Package outline SOT873-1 (DFN3333-8)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN013-30LL v.5	20111208	Product data sheet	-	PSMN013-30LL v.4
Modifications:	• Various changes to content.			
PSMN013-30LL v.4	20100707	Product data sheet	-	PSMN013-30LL v.3

## 9. Legal information

### 9.1 Data sheet status

Document status <a href="#">[1]</a> <a href="#">[2]</a>	Product status <a href="#">[3]</a>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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## 10. Contact information

For more information, please visit: <http://www.nxp.com>

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## 11. Contents

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<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features and benefits . . . . .	1
1.3	Applications . . . . .	1
1.4	Quick reference data . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>2</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Limiting values</b> . . . . .	<b>3</b>
<b>5</b>	<b>Thermal characteristics</b> . . . . .	<b>5</b>
<b>6</b>	<b>Characteristics</b> . . . . .	<b>6</b>
<b>7</b>	<b>Package outline</b> . . . . .	<b>11</b>
<b>8</b>	<b>Revision history</b> . . . . .	<b>12</b>
<b>9</b>	<b>Legal information</b> . . . . .	<b>13</b>
9.1	Data sheet status . . . . .	13
9.2	Definitions . . . . .	13
9.3	Disclaimers . . . . .	13
9.4	Trademarks . . . . .	14
<b>10</b>	<b>Contact information</b> . . . . .	<b>14</b>

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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