

# PSMN023-80LS

N-channel DFN3333-8 80 V 23 mΩ standard level MOSFET

Rev. 3 — 12 December 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in DFN3333-8 package qualified to 150 °C. This product is designed and qualified for use in a wide range of industrial, communications and power supply equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources
- Small footprint for compact designs

### 1.3 Applications

- DC-to-DC converters
- Load switching
- Lithium-ion battery protection

### 1.4 Quick reference data

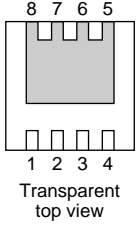
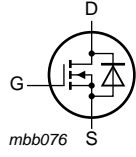
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>	-	-	34	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	65	W
$T_j$	junction temperature		-55	-	150	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_j = 100\text{ °C}$ ; see <a href="#">Figure 12</a>	-	-	38	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 13</a>	-	19	23	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 30\text{ A}$ ; $V_{DS} = 40\text{ V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	4.8	-	nC
$Q_{G(tot)}$	total gate charge		-	21	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 34\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ Ω}$ ; unclamped	-	-	37	mJ



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>Transparent top view</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
5,6,7,8	D	drain		
mb	D	mounting base; connected to drain		

**SOT873-1 (DFN3333-8)**

## 3. Ordering information

Table 3. Ordering information

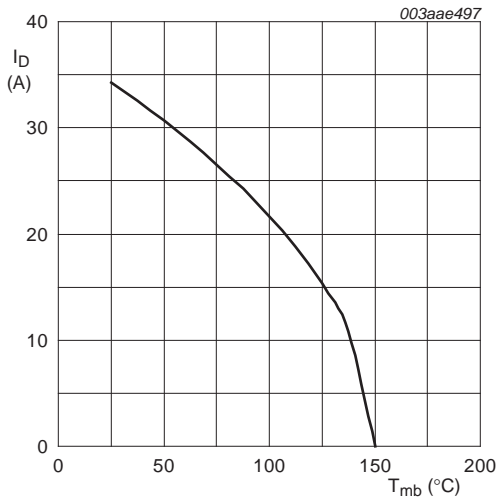
Type number	Package		
	Name	Description	Version
PSMN023-80LS	DFN3333-8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals	SOT873-1

## 4. Limiting values

Table 4. Limiting values

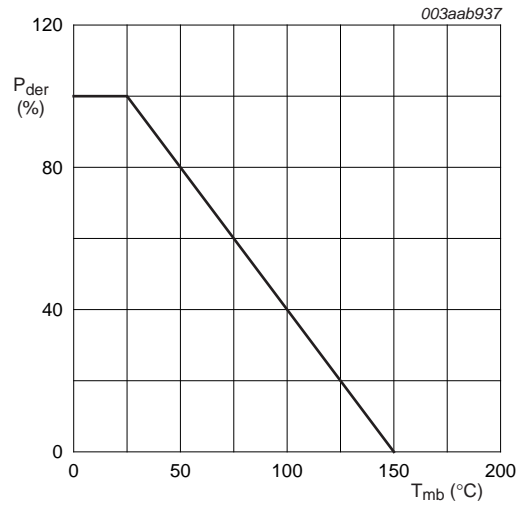
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	80	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	80	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	22	A
		$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	34	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	137	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	65	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	34	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	137	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 34\text{ A}; V_{sup} \leq 80\text{ V}; R_{GS} = 50\text{ }\Omega$ ; unclamped	-	37	mJ



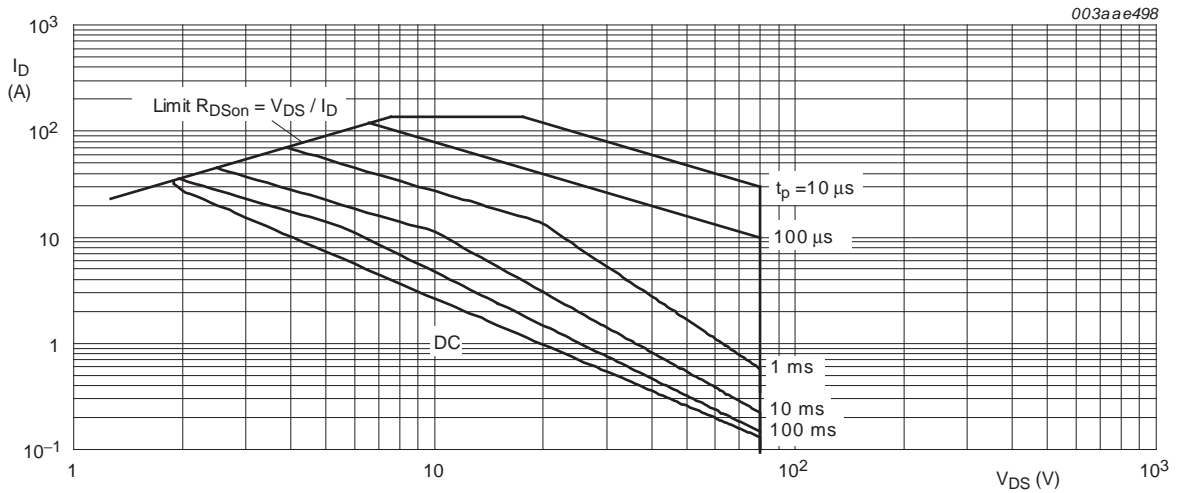
$V_{GS} \geq 10\text{ V}$

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$T_{mb} = 25^\circ\text{C}$ ;  $I_{DM}$  is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	1	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	53	60	K/W

[1]  $R_{th(j-a)}$  is guaranteed by design and assumes that the device is mounted on a 40mm x 40mm x 70μm copper pad at 20°C ambient temperature. In practice  $R_{th(j-a)}$  will be determined by the customer's PCB characteristics

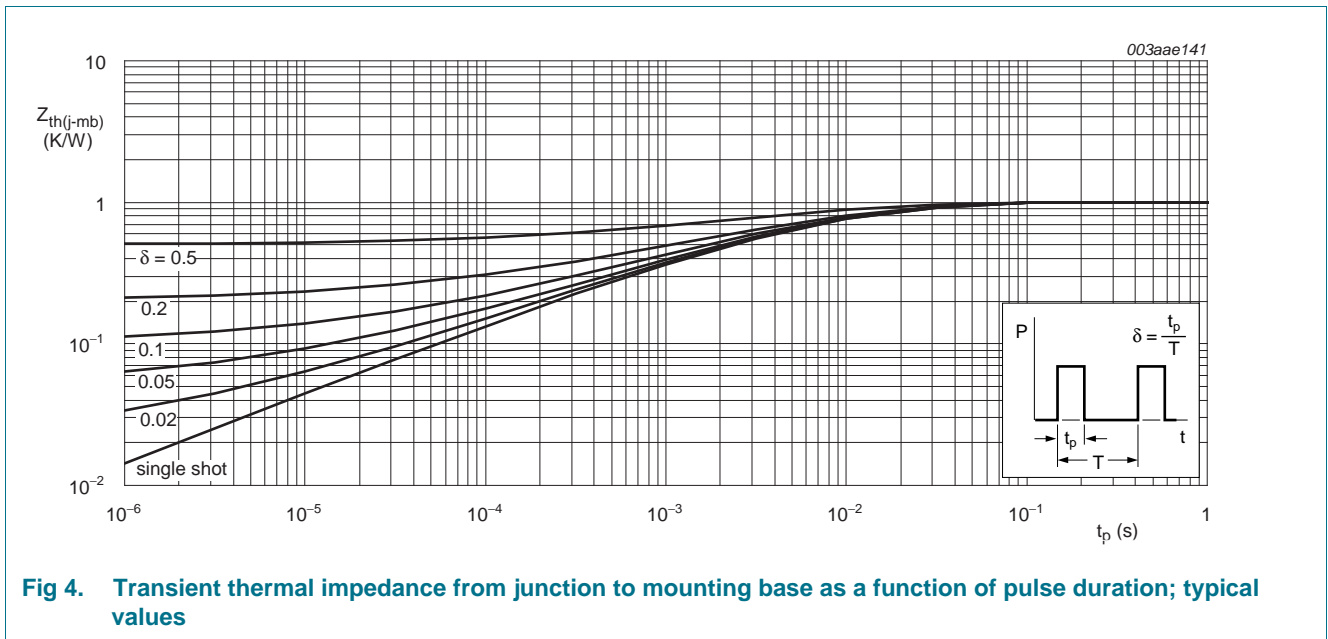


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

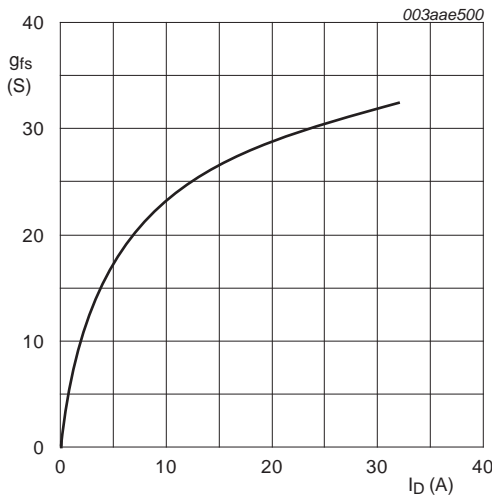
## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	73	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	-	4.7	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	2.3	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.1	2	$\mu\text{A}$
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	50	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	39.9	48.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	-	38	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	19	23	mΩ
$R_G$	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	1	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a>	-	18.4	-	nC
		$I_D = 30 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	21	-	nC
$Q_{GS}$	gate-source charge		-	6.6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	3.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	2.7	-	nC
$Q_{GD}$	gate-drain charge		-	4.8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 30 \text{ A}; V_{DS} = 40 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	5	-	V
$C_{iss}$	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 16</a>	-	1295	-	pF
$C_{oss}$	output capacitance		-	125	-	pF
$C_{riss}$	reverse transfer capacitance		-	69	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 1.33 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 4.7 \text{ } \Omega$	-	10.5	-	ns
$t_r$	rise time	$V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 4.7 \text{ } \Omega$	-	8	-	ns
$t_{d(off)}$	turn-off delay time	$V_{DS} = 40 \text{ V}; R_L = 1.33 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 4.7 \text{ } \Omega$	-	20.5	-	ns
$t_f$	fall time		-	5.4	-	ns

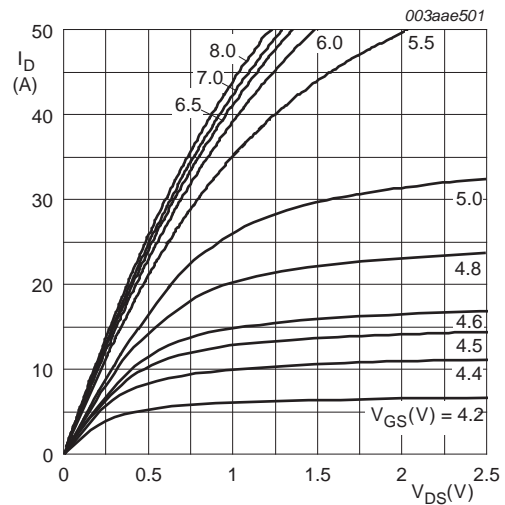
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 10\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 17</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10\text{ A}$ ; $dI_S/dt = 100\text{ A}/\mu\text{s}$ ;	-	36	-	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 40\text{ V}$	-	53	-	nC



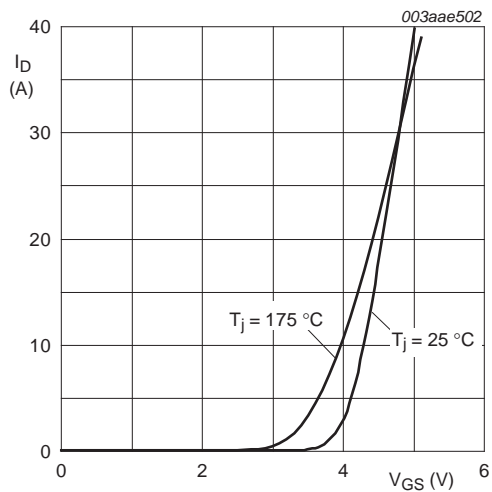
$T_j = 25\text{ °C}$ ;  $V_{DS} = 10\text{ V}$

Fig 5. Forward transconductance as a function of drain current; typical values



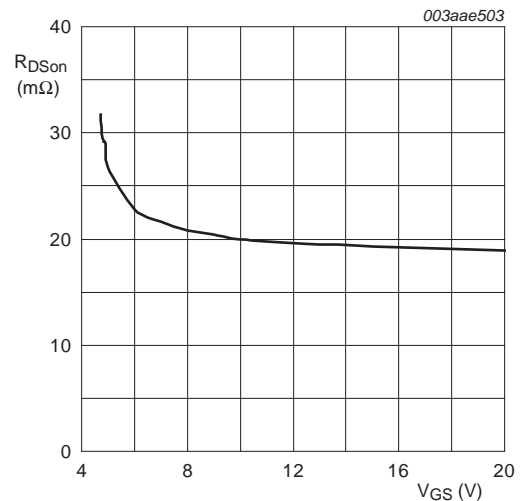
$T_j = 25\text{ °C}$ ;  $t_p = 300\text{ }\mu\text{s}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



$V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$T_j = 25\text{ °C}$ ;  $I_D = 10\text{ A}$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

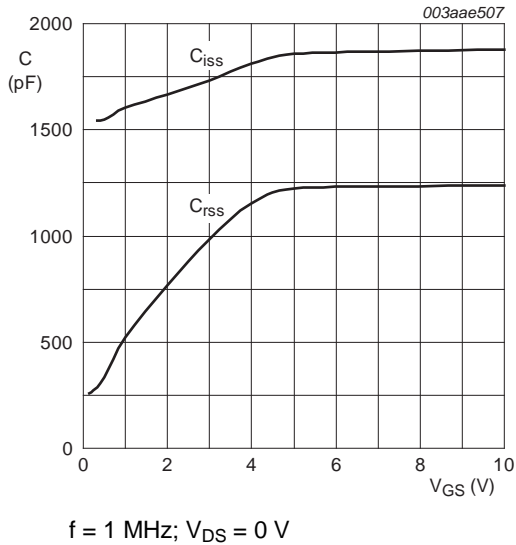
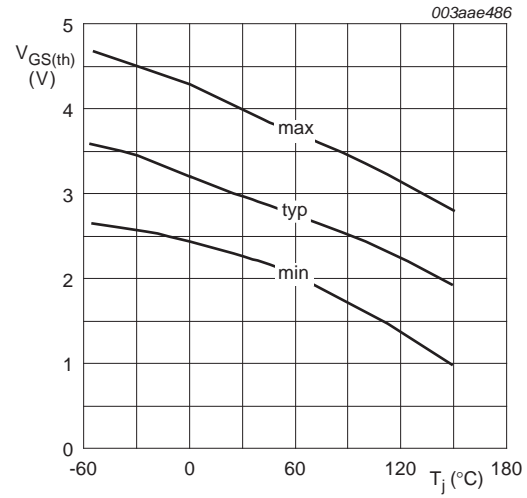
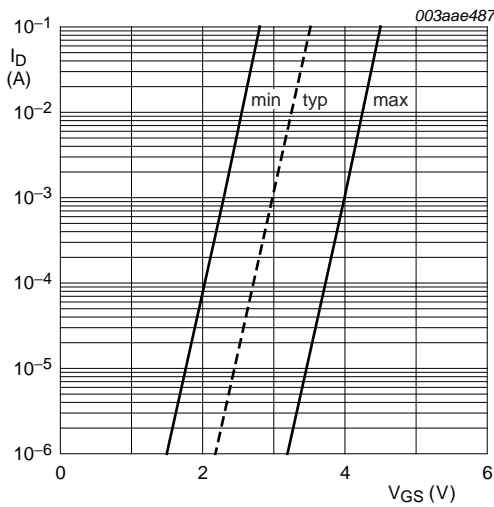


Fig 9. Input and reverse transfer capacitances as a function of gate-source voltage, typical values



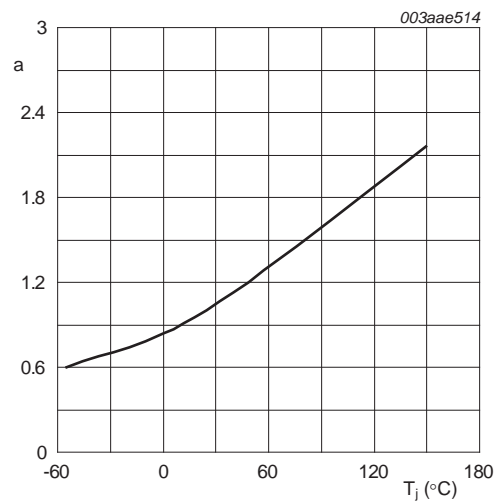
$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

Fig 10. Gate-source threshold voltage as a function of junction temperature



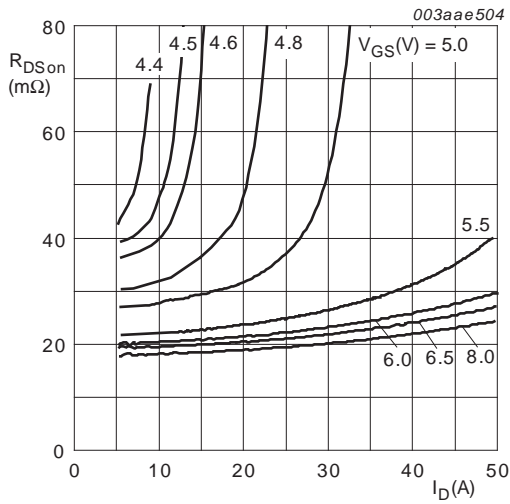
$$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon}(25 \text{ }^\circ\text{C})}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

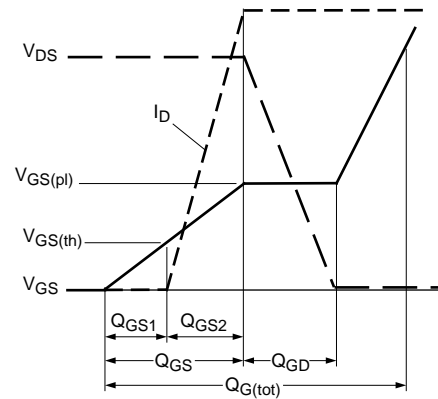
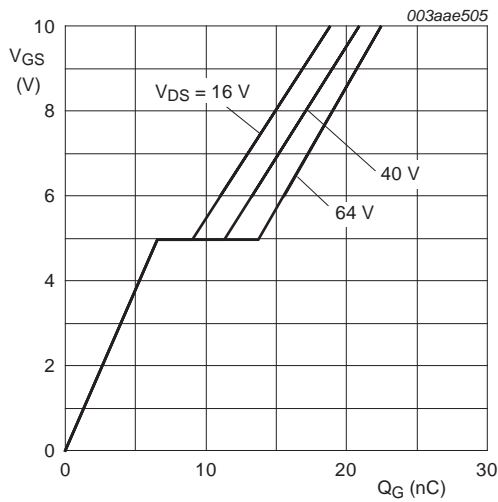
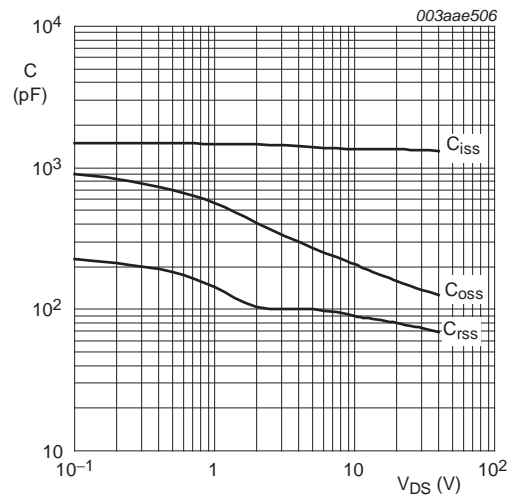


Fig 14. Gate charge waveform definitions



$T_j = 25^\circ\text{C}; I_D = 30 \text{ A}$

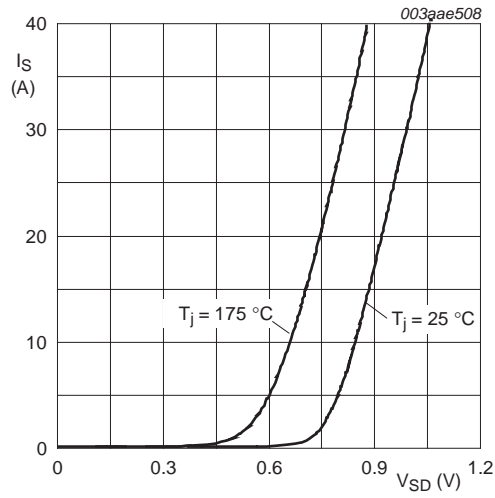
Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





$V_{GS} = 0\text{ V}$

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

## 7. Package outline

DFN3333-8: plastic thermal enhanced very thin small outline package; no leads;  
8 terminals; body 3.3 x 3.3 x 1.0 mm

SOT873-1

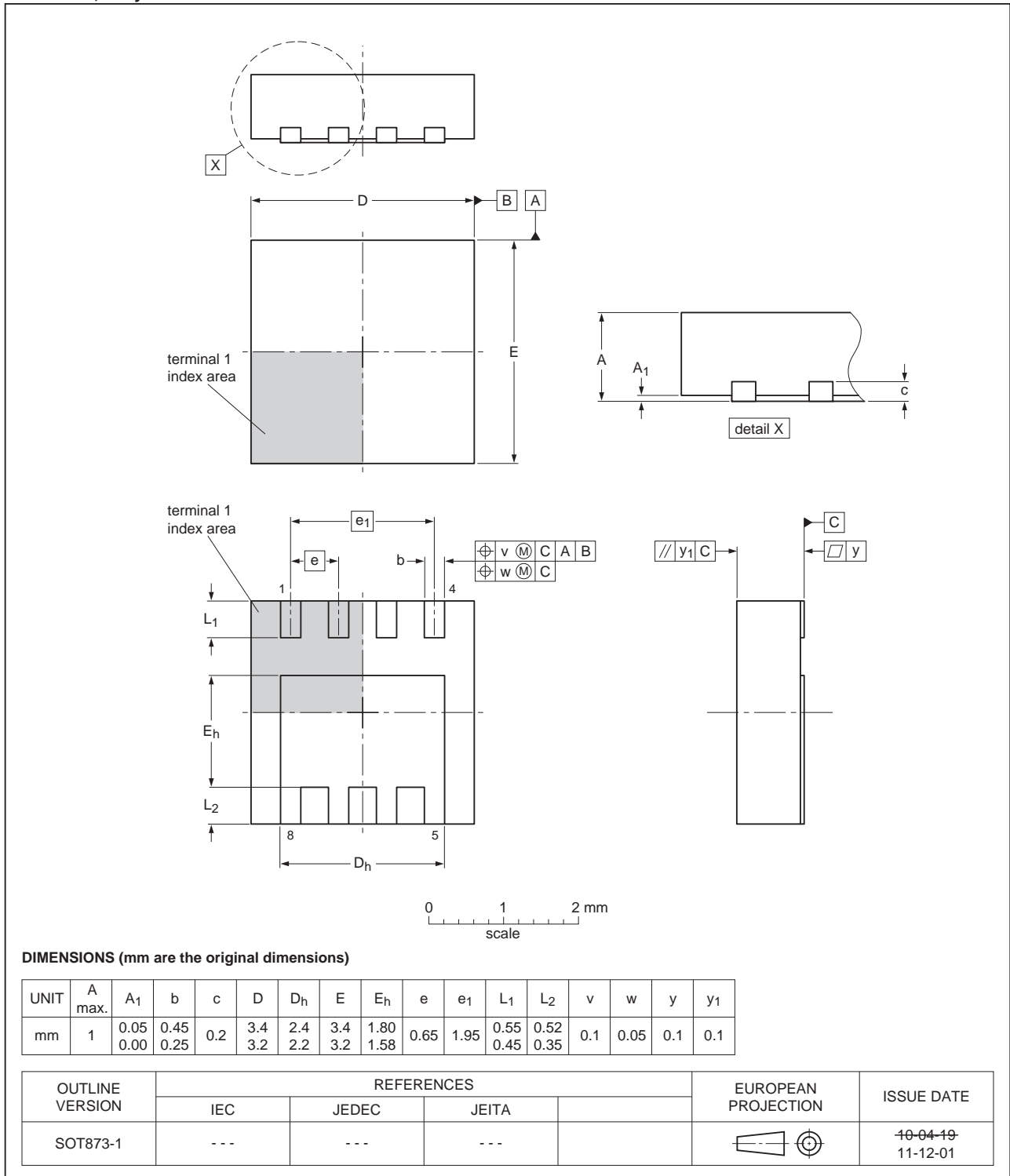


Fig 18. Package outline SOT873-1 (DFN3333-8)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN023-80LS v.3	20111212	Product data sheet	-	PSMN023-80LS v.2
Modifications:	• Various changes to content.			
PSMN023-80LS v.2	20100818	Product data sheet	-	PSMN023-80LS v.1

## 9. Legal information

### 9.1 Data sheet status

Document status <a href="#">[1]</a> <a href="#">[2]</a>	Product status <a href="#">[3]</a>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 11. Contents

<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features and benefits . . . . .	1
1.3	Applications . . . . .	1
1.4	Quick reference data . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>2</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Limiting values</b> . . . . .	<b>2</b>
<b>5</b>	<b>Thermal characteristics</b> . . . . .	<b>4</b>
<b>6</b>	<b>Characteristics</b> . . . . .	<b>5</b>
<b>7</b>	<b>Package outline</b> . . . . .	<b>10</b>
<b>8</b>	<b>Revision history</b> . . . . .	<b>11</b>
<b>9</b>	<b>Legal information</b> . . . . .	<b>12</b>
9.1	Data sheet status . . . . .	12
9.2	Definitions . . . . .	12
9.3	Disclaimers . . . . .	12
9.4	Trademarks . . . . .	13
<b>10</b>	<b>Contact information</b> . . . . .	<b>13</b>

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