DATA SHEET

UBA2033
HF full bridge driver IC

Product specification

2002 Oct 08

HF full bridge driver IC UBA2033

FEATURES

- Full bridge driver circuit
- Integrated bootstrap diodes
- Integrated high voltage level shift function
- High voltage input for the internal supply voltage
- 550 V maximum voltage
- Bridge disable function
- Input for start-up delay
- Adjustable oscillator frequency
- Predefined bridge position during start-up.

APPLICATIONS

- The UBA2033 can drive (via the MOSFETs) any kind of load in a full bridge configuration
- The circuit is especially designed as a commutator for High Intensity Discharge (HID) lamps.

GENERAL DESCRIPTION

The UBA2033 is a high voltage monolithic integrated circuit made in the EZ-HV SOI process. The circuit is designed for driving the MOSFETs in a full bridge configuration. In addition, it features a disable function, an internal adjustable oscillator and an external drive function with a low-voltage level shifter for driving the bridge.
To guarantee an accurate 50% duty factor, the oscillator signal can be passed through a divider before being fed to the output driver.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA2033TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

BLOCK DIAGRAM

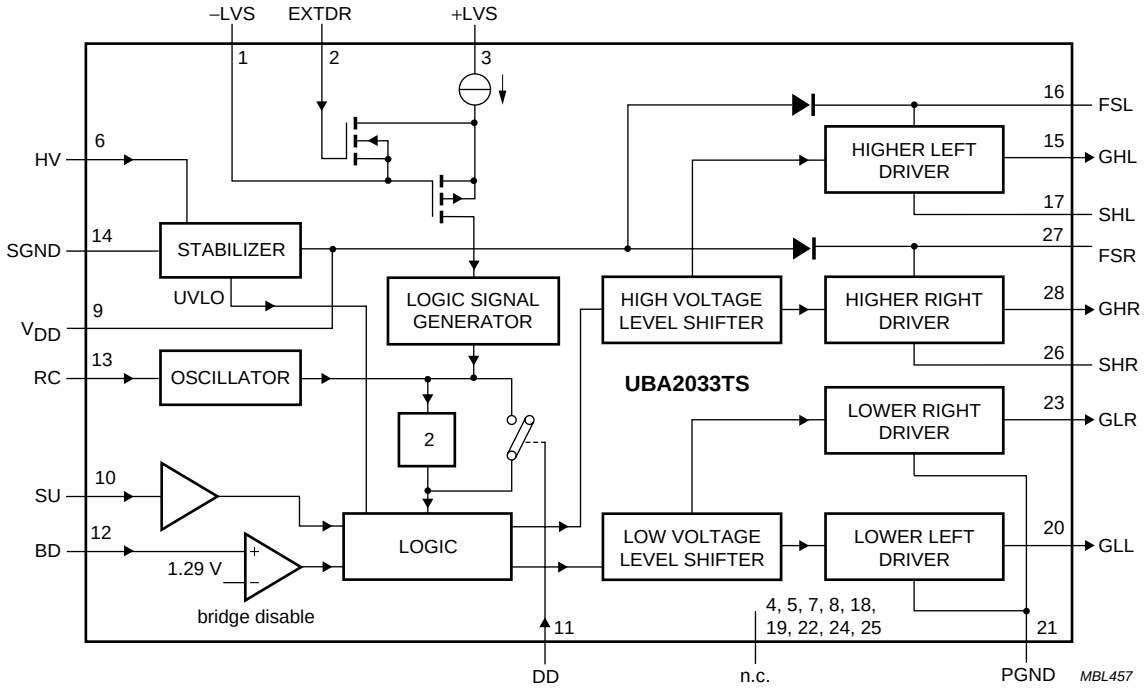


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
−LVS	1	negative supply voltage (for logic input)
EXTDR	2	oscillator signal input
+LVS	3	positive supply voltage (for logic input)
n.c.	4	not connected
n.c.	5	not connected
HV	6	high voltage supply input
n.c.	7	not connected
n.c.	8	not connected
V_{DD}	9	internal low voltage supply
SU	10	input signal for start-up delay
DD	11	divider disable input
BD	12	bridge disable control input
RC	13	RC input for internal oscillator
SGND	14	signal ground
GHL	15	gate of higher left output MOSFET
FSL	16	floating supply voltage left
SHL	17	source of higher left MOSFET
n.c.	18	not connected
n.c.	19	not connected
GLL	20	gate of lower left output MOSFET
PGND	21	power ground
n.c.	22	not connected
GLR	23	gate of lower right output MOSFET
n.c.	24	not connected
n.c.	25	not connected
SHR	26	source of higher right MOSFET
FSR	27	floating supply voltage right
GHR	28	gate of higher right output MOSFET

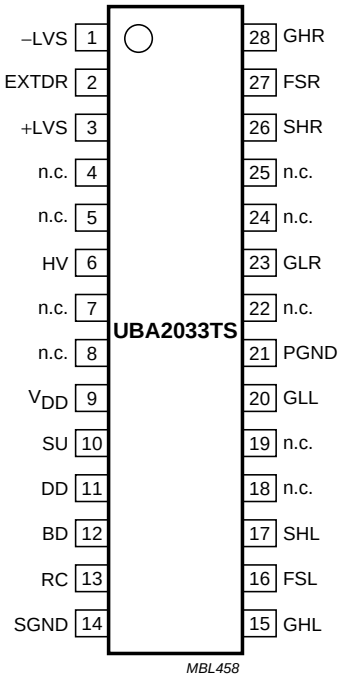


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Supply voltage

The UBA2033 is powered by a supply voltage applied to pin HV, for instance the supply voltage of the full bridge. The IC generates its own low supply voltage for the internal circuitry. Therefore an additional low voltage supply is not required. A capacitor has to be connected to pin V_{DD} to obtain a ripple-free internal supply voltage.

The circuit can also be powered by a low voltage supply directly applied to pin V_{DD}. In this case pin HV should be connected to pin V_{DD} or SGND.

Start-up

With an increasing supply voltage the IC enters the start-up state; the higher power transistors are kept off and the lower power transistors are switched on. During the start-up state the bootstrap capacitors are charged and the bridge output current is zero. The start-up state is defined until $V_{DD} = V_{DD(UVLO)}$, where UVLO stands for Under Voltage Lock-out. The state of the outputs during the start-up phase is overruled by the bridge disable function.

Release of the power drive

At the moment the supply voltage on pin V_{DD} or HV exceeds the level of release power drive, the output voltage of the bridge depends on the control signal on pin EXTDR (see Table 1). The bridge position after start-up, disable, or delayed start-up (via pin SU) depends on the status of the pins DD and EXTDR. If pin DD = LOW (divider enabled) the bridge will start in the pre-defined position: pin GLR and pin GHL = HIGH and pin GLL and pin GHR = LOW. If pin DD = HIGH (divider disabled) the bridge position will depend on the status of pin EXTDR.

If the supply voltage on pin V_{DD} or HV decreases and drops below the reset level of power drive the IC enters the start-up state again.

Oscillation

At the point where the supply voltage on pin HV crosses the level of release power drive, the bridge begins commutating between the following two defined states:

- Higher left and lower right MOSFETs on, higher right and lower left MOSFETs off
- Higher left and lower right MOSFETs off, higher right and lower left MOSFETs on.

The oscillation can take place in three different modes:

- Internal oscillator mode.

  In this mode the bridge commutating frequency is determined by the values of an external resistor (R_{osc}) and capacitor (C_{osc}). In this mode pin EXTDR must be connected to pin +LVS. To realize an accurate 50% duty factor, the internal divider should be used. The internal divider is enabled by connecting pin DD to SGND. Due to the presence of the divider the bridge frequency is half the oscillator frequency. The commutation of the bridge will take place at the falling edge of the signal on pin RC. To minimize the current consumption pins +LVS, –LVS and EXTDR can be connected together to either pin SGND or V_{DD}. In this way the current source in the logic voltage supply circuit is shut off.
- External oscillator mode without the internal divider.

  In the external oscillator mode the external source is connected to pin EXTDR and pin RC is short-circuited to pin SGND to disable the internal oscillator. If the internal divider is disabled (pin DD = V_{DD}) the duty factor of the bridge output signal is determined by the external oscillator signal and the bridge frequency equals the external oscillator frequency.
- External oscillator mode with the internal divider.

  The external oscillator mode can also be used with the internal divider function enabled (pin RC and pin DD = SGND). Due to the presence of the divider the bridge frequency is half the external oscillator frequency. The commutation of the bridge is triggered by the falling edge of the EXTDR signal with respect to V_{-LVS}.

The design equation for the bridge oscillator frequency is:

$$f_{bridge} = \frac{1}{(k_{osc} \times R_{osc} \times C_{osc})}$$

Non-overlap time

The non-overlap time is the time between turning off the conducting pair of MOSFETs and turning on the next pair. The non-overlap time is internally fixed to a very small value, which allows an HID system to operate with a very small phase difference between load current and full bridge voltage (pins SHL and SHR). Especially when igniting an HID lamp via a LC resonance circuit, a small ‘dead time’ is essential. The high maximum operating frequency, together with a small ‘dead time’, also gives the opportunity to ignite the HID lamp at the third harmonic of the full bridge voltage, thereby reducing costs in the magnetic power components.

'Dead time' can be increased by adding a resistor (for slowly turning on the full bridge power FETs) and a diode (for quickly turning off the full bridge power FETs) in parallel, both in series with the gate drivers (see Fig.3).

Divider function

If pin DD = SGND, then the divider function is enabled/present. If the divider function is present there is no direct relation between the position of the bridge output and the status of pin EXTDR.

Start-up delay

Normally, the circuit starts oscillating as soon as pin V_{DD} or HV reaches the level of release power drive. At this moment the gate drive voltage is equal to the voltage on pin V_{DD} for the low side transistors and $V_{DD} - 0.6$ V for the high side transistors. If this voltage is too low for sufficient drive of the MOSFETs the release of the power drive can be delayed via pin SU.

A simple RC filter (R between pins V_{DD} and SU; C between pins SU and SGND) can be used to make a delay, or a control signal from a processor can be used.

Bridge disable

The bridge disable function can be used to switch off all the MOSFETs as soon as the voltage on pin BD exceeds the bridge disable voltage (1.29 V). The bridge disable function overrules all the other states.

Table 1 Logic table; note 1

DEVICE STATUS	INPUTS				OUTPUTS			
	BD	SU	DD	EXTDR	GHL	GHR	GLL	GLR
Start-up state	HIGH	X	X	X	LOW	LOW	LOW	LOW
	LOW	X	X	X	LOW	LOW	HIGH	HIGH
Oscillation state	HIGH	X	X	X	LOW	LOW	LOW	LOW
	LOW	LOW	X	X	LOW	LOW	HIGH	HIGH
	LOW	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	LOW
				LOW	HIGH	LOW	LOW	HIGH
	LOW	HIGH	LOW	LOW	HIGH	LOW	LOW	HIGH
				LOW-to-HIGH				
				HIGH				
				HIGH-to-LOW	LOW	HIGH	HIGH	LOW

Note

1. X = don't care
   a) BD, SU and DD logic levels are with respect to SGND
   b) EXTDR logic levels are with respect to V_{-LVS}
   c) GHL logic levels are with respect to SHL
   d) GHR logic levels are with respect to SHR
   e) GLL and GLR logic levels are with respect to PGND
   f) If pin DD = LOW the bridge enters the state (oscillation state and pin BD = LOW and pin SU = HIGH) in the pre-defined position pin GHL and pin GLR = HIGH and pin GLL and pin GHR = LOW.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are measured with respect to SGND; positive currents flow into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (low voltage)	DC value	0	14	V
		transient at t < 0.1 μs	0	17	V
V_{HV}	supply voltage (high voltage)		0	550	V
V_{FSL}	floating supply voltage left	$V_{SHL} = V_{SHR}$ = 550 V	0	564	V
		$V_{SHL} = V_{SHR}$ = 0 V	0	14	V
V_{FSR}	floating supply voltage right	$V_{SHL} = V_{SHR}$ = 550 V	0	564	V
		$V_{SHL} = V_{SHR}$ = 0 V	0	14	V
V_{SHL}	source voltage for higher left MOSFETs	with respect to PGND and SGND	−3	+550	V
		with respect to SGND; t < 1 μs	−14	−	V
V_{SHR}	source voltage for higher right MOSFETs	with respect to PGND and SGND	−3	+550	V
		with respect to SGND; t < 1 μs	−14	−	V
V_{PGND}	power ground voltage	with respect to SGND	0	5	V
V_{-LVS}	negative supply voltage for logic input		−0.9	+17	V
I_{-LVS}	negative supply current for logic input	pin EXTDR = HIGH	−1	−	mA
V_{+LVS}	positive supply voltage for logic input	V_{HV} = 0 V; DC value	0	14	V
		transient at t < 0.1 μs	0	17	V
$V_{i(EXTDR)}$	input voltage from external oscillator on pin EXTDR	with respect to V_{-LVS}	0	V_{+LVS}	V
$V_{i(RC)}$	input voltage on pin RC	DC value	0	V_{DD}	V
		transient at t < 0.1 μs	0	17	V
$V_{i(SU)}$	input voltage on pin SU	DC value	0	V_{DD}	V
		transient at t < 0.1 μs	0	17	V
$V_{i(BD)}$	input voltage on pin BD	DC value	0	V_{DD}	V
		transient at t < 0.1 μs	0	17	V
$V_{i(DD)}$	input voltage on pin DD	DC value	0	V_{DD}	V
		transient at t < 0.1 μs	0	17	V
SR	slew rate at output pins	repetitive	0	4	V/ns
T_j	junction temperature		−40	+150	°C
T_{amb}	ambient temperature		−40	+150	°C
T_{stg}	storage temperature		−55	+150	°C
V_{esd}	electrostatic discharge voltage on pins HV, +LVS, −LVS, EXTDR, FSL, GHL, SHL, SHR, GHR and FSR	note 1	−	900	V

Note

1. In accordance with the Human Body Model (HBM): equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	100	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611D"*.

CHARACTERISTICS

T_j = 25 °C; all voltages are measured with respect to SGND; positive currents flow into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High voltage						
I_{HV}	high voltage supply current	t < 0.5 s and V_{HV} = 550 V	0	–	30	μA
I_{FSL}, I_{FSR}	high voltage floating supply current	t < 0.5 s and V_{FSL} = V_{FSR} = 564 V	0	–	30	μA
Start-up; powered via pin HV						
$I_{i(HV)}$	HV input current	V_{HV} = 11 V; note 1	–	0.5	1.0	mA
$V_{HV(rel)}$	level of release power drive voltage		11	12.5	14	V
$V_{HV(UVLO)}$	reset level of power drive voltage		8.5	10	11.5	V
$V_{HV(hys)}$	HV hysteresis voltage		2.0	2.5	3.0	V
V_{DD}	internal supply voltage	V_{HV} = 20 V	10.5	11.5	13.5	V
Start-up; powered via pin V_{DD}						
$I_{i(DD)}$	V_{DD} input current	V_{DD} = 8.25 V; note 2	–	0.5	1.0	mA
$V_{DD(rel)}$	level of release power drive voltage		8.25	9.0	9.75	V
$V_{DD(UVLO)}$	reset level of power drive voltage		5.75	6.5	7.25	V
$V_{DD(hys)}$	hysteresis voltage		2.0	2.5	3.0	V
Output stage						
$R_{on(H)}$	higher MOSFETs on resistance	V_{FSR} = V_{FSL} = 12 V (with respect to SHR and SHL); I_{source} = 50 mA	15	21	26	Ω
$R_{off(H)}$	higher MOSFETs off resistance	V_{FSR} = V_{FSL} = 12 V (with respect to SHR and SHL); I_{sink} = 50 mA	9	14	18	Ω
$R_{on(L)}$	lower MOSFETs on resistance	V_{DD} = 12 V; I_{source} = 50 mA	15	21	26	Ω
$R_{off(L)}$	lower MOSFETs off resistance	V_{DD} = 12 V; I_{sink} = 50 mA	9	14	18	Ω
$I_{o(source)}$	output source current	V_{DD} = V_{FSL} = V_{FSR} = 12 V; V_{GHR} = V_{GHL} = V_{GLR} = V_{GLL} = 0 V	130	180	–	mA
$I_{o(sink)}$	output sink current	V_{DD} = V_{FSL} = V_{FSR} = 12 V; V_{GHR} = V_{GHL} = V_{GLR} = V_{GLL} = 12 V	150	200	–	mA
V_{diode}	bootstrap diode voltage drop	I_{diode} = 20 mA	1.7	2.1	2.5	V
t_{no}	non-overlap time		–	–	250	ns
V_{FSL}	HS lockout voltage left		3.0	4.0	5.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{FSR}	HS lockout voltage right		3.0	4.0	5.0	V
I_{FSL}	FS supply current left	V_{FSL} = 12 V	2	4	6	μA
I_{FSR}	FS supply current right	V_{FSR} = 12 V	2	4	6	μA
DD input						
V_{IH}	HIGH-level input voltage	V_{DD} = 12 V	6	–	–	V
V_{IL}	LOW-level input voltage		–	–	3	V
$I_{i(DD)}$	input current into pin DD		–	–	1	μA
SU input						
V_{IH}	HIGH-level input voltage	V_{DD} = 12 V	4	–	–	V
V_{IL}	LOW-level input voltage		–	–	2	V
$I_{i(SU)}$	input current into pin SU		–	–	1	μA
External drive input						
V_{IH}	HIGH-level input voltage	with respect to V_{-LVS}	4.0	–	–	V
V_{IL}	LOW-level input voltage	with respect to V_{-LVS}	–	–	1.0	V
$I_{i(EXTDR)}$	input current into pin EXTDR		–	–	1	μA
f_{bridge}	bridge frequency	note 3	–	–	250	kHz
Low voltage logic supply						
I_{+LVS}	low voltage supply current	V_{+LVS} = V_{EXTDR} = 5.75 to 14 V with respect to V_{-LVS}	–	250	500	μA
V_{+LVS}	low voltage supply voltage	with respect to V_{-LVS}	5.75	–	14	V
Bridge disable input						
$V_{ref(dis)}$	disable reference voltage		1.23	1.29	1.35	V
$I_{i(BD)}$	disable input current		–	–	1	μA
Internal oscillator						
f_{bridge}	bridge oscillating frequency	note 3	–	–	100	kHz
$\Delta f_{osc(T)}$	oscillator frequency variation with temperature	f_{bridge} = 250 Hz and T_{amb} = −40 to +150 °C	−10	0	+10	%
$\Delta f_{osc(VDD)}$	oscillator frequency variation with V_{DD}	f_{bridge} = 250 Hz and V_{DD} = 7.25 to 14 V	−10	0	+10	%
k_H	high level trip point	$V_{RC(high)} = k_H \times V_{DD}$	0.38	0.4	0.42	
k_L	low level trip point	$V_{RC(low)} = k_L \times V_{DD}$	–	0.01	–	
k_{osc}	oscillator constant	f_{bridge} = 250 Hz	0.94	1.02	1.10	
R_{ext}	external resistor to V_{DD}		100	–	–	kΩ

Notes

1. The current is specified without commutation of the bridge. The current into pin HV is limited by a thermal protection circuit. The current is limited to 11 mA at T_j = 150 °C.
2. The current is specified without commutation of the bridge and pin HV is connected to V_{DD}.
3. The minimum frequency is mainly determined by the value of the bootstrap capacitors.

APPLICATION INFORMATION

Basic application

A basic full bridge configuration with an HID lamp is shown in Fig.3. The bridge disable, the start-up delay and the external drive functions are not used in this application. The pins −LVS, +LVS, EXTDR and BD are short-circuited to SGND. The internal oscillator is used and to realize a 50% duty cycle the internal divider function has to be used by connecting pin DD to SGND. The IC is powered by the high voltage supply. Because the internal oscillator is used, the bridge commutating frequency is determined by the values of R_{osc} and C_{osc}. The bridge starts oscillating when the HV supply voltage exceeds the level of release power drive (typically 12.5 V on pin HV). If the supply voltage on pin HV drops below the reset level of power drive (typically 10 V on pin HV), the UBA2033 enters the start-up state.

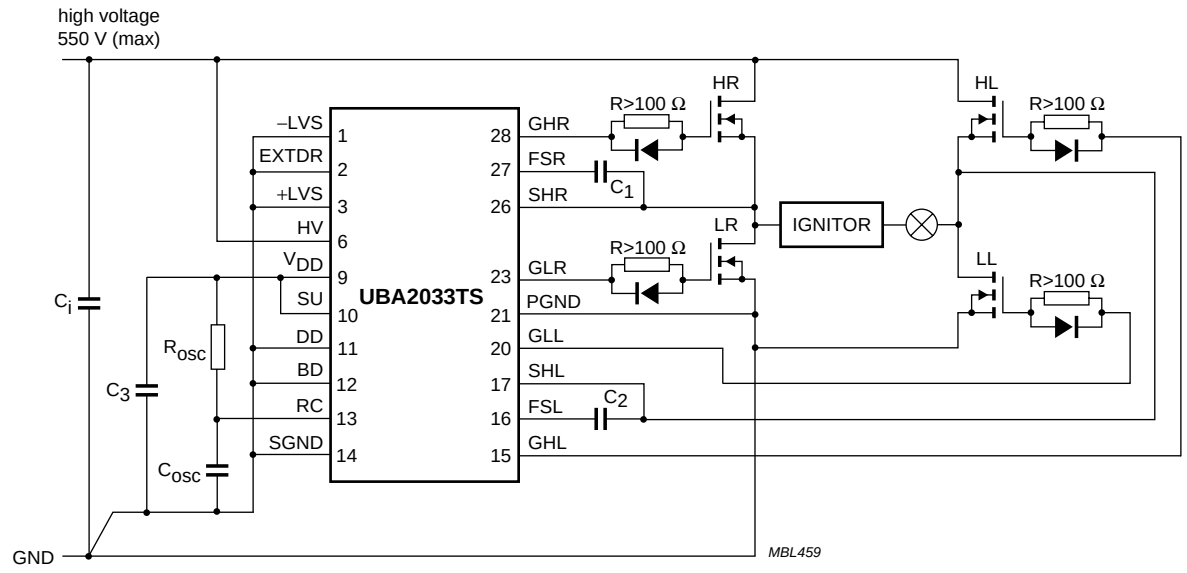


Fig.3 Basic configuration.

Application with external control

Figure 4 shows an application containing a system ground-referenced control circuit. Pin +LVS can be connected to the same supply as the external oscillator control unit and pin −LVS is connected to SGND. Pin RC is short-circuited to SGND. The bridge commutation frequency is determined by the external oscillator. The bridge disable input (pin BD) can be used to immediately turn off all four MOSFETs in the full bridge.

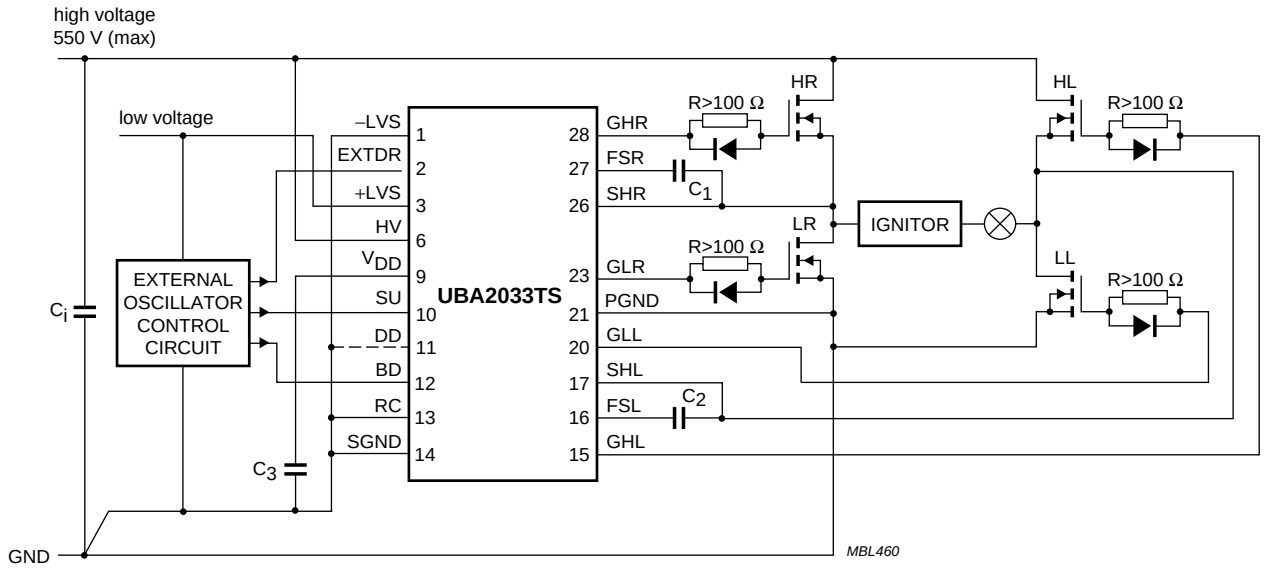


Fig.4 External control configuration.

Additional application information

GATE RESISTORS

At ignition of an HID lamp, a large EMC spark occurs. This can result in a large voltage transient or oscillation at the gates of the full bridge MOSFETs (LL, LR, HR and HL). When these gates are directly coupled to the gate drivers (pins GHR, GLR, GHL and GLL), voltage overstress of the driver outputs may occur. Therefore it is advised to add a resistor with a minimum value of 100 Ω in series with each gate driver to isolate the gate driver outputs from the actual power MOSFETs gate.

'Dead time' can also be adjusted via the combination gate resistor and gate-source capacitance.

GATE CHARGE AND SUPPLY CURRENT AT HIGH FREQUENCY USE

The total gate current needed to charge the gates of the power MOSFETs equals:

$$I_{gate} = 4 \times f_{bridge} \times Q_{gate}$$

Where:

I_{gate} = gate current

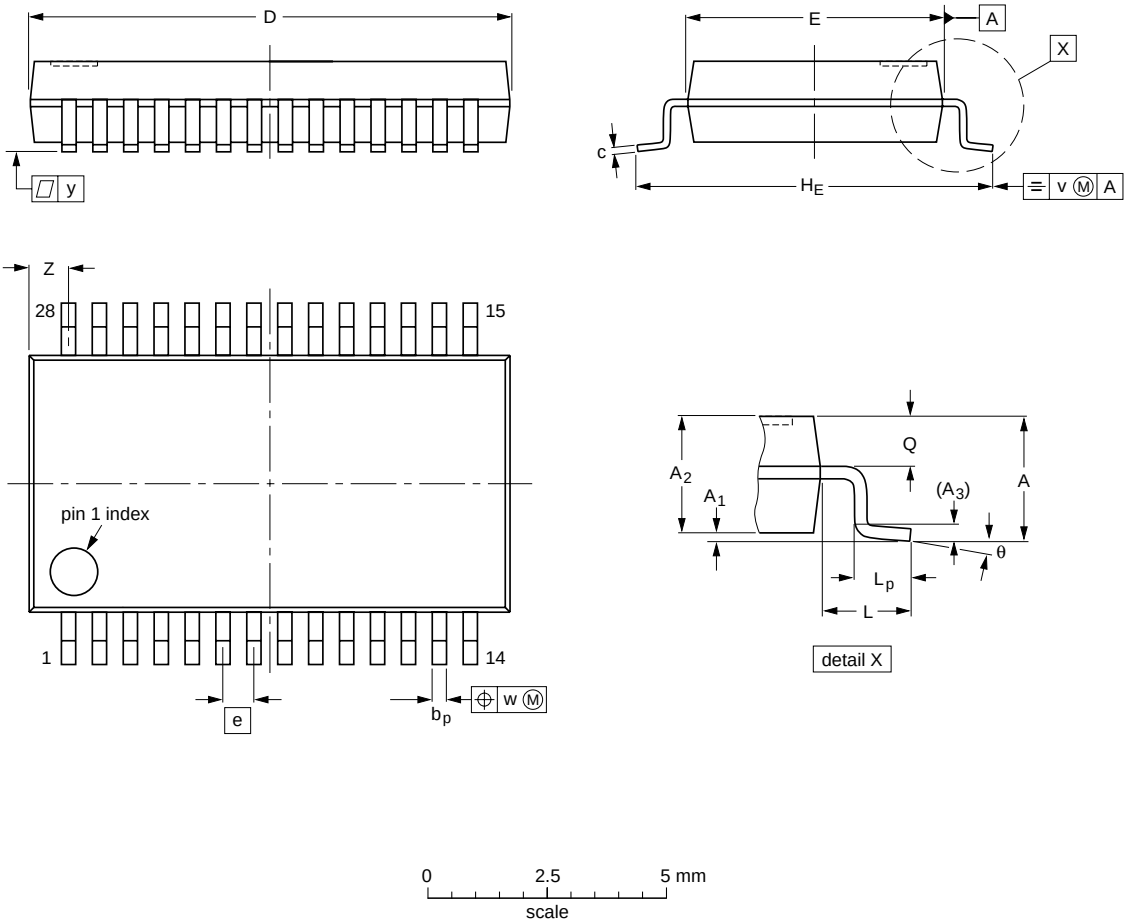
f_{bridge} = bridge frequency

Q_{gate} = gate charge.

This current is supplied via the internal low voltage supply (V_{DD}). Since this current is limited to 11 mA (see "Characteristics" table note 1), at higher frequencies and with MOSFETs having a relative high gate charge, this maximum V_{DD} supply current may not be sufficient anymore. As a result the internal low voltage supply (V_{DD}) and the gate drive voltage will drop resulting in an increase of the higher resistance (R_{on}) of the full bridge MOSFETs. In this case an auxiliary low voltage supply is necessary.

PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT341-1		MO-150				~~99-12-27~~ 03-02-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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