



2SK4085LS

N-Channel Power MOSFET 500V, 16A, 430mΩ, TO-220F-3FS

ON Semiconductor®

<http://onsemi.com>

Features

- ON-resistance $R_{DS(on)}=0.33\Omega$ (typ.)
- Input capacitance $C_{iss}=1200\text{pF}$ (typ.)
- 10V drive

Specifications

Absolute Maximum Ratings at $T_a=25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DS}		500	V
Gate-to-Source Voltage	V_{GS}		± 30	V
Drain Current (DC)	I_{Dc} *1	Limited only by maximum temperature $T_{ch}=150^\circ\text{C}$	16	A
	I_{Dpack} *2	$T_c=25^\circ\text{C}$ (Our ideal heat dissipation condition)*3	11	A
Drain Current (Pulse)	I_{DP}	$PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$	60	A
			2.0	W
Allowable Power Dissipation	P_D	$T_c=25^\circ\text{C}$ (Our ideal heat dissipation condition)*3	40	W
			150	$^\circ\text{C}$
Channel Temperature	T_{ch}		-55 to $+150$	$^\circ\text{C}$
Storage Temperature	T_{stg}			$^\circ\text{C}$
Avalanche Energy (Single Pulse) *4	E_{AS}		141	mJ
Avalanche Current *5	I_{AV}		16	A

*1 Shows chip capability.

*2 Package limited.

*3 Our condition is radiation from backside.

The method is applying silicone grease to the backside of the device and attaching the device to water-cooled radiator made of aluminium.

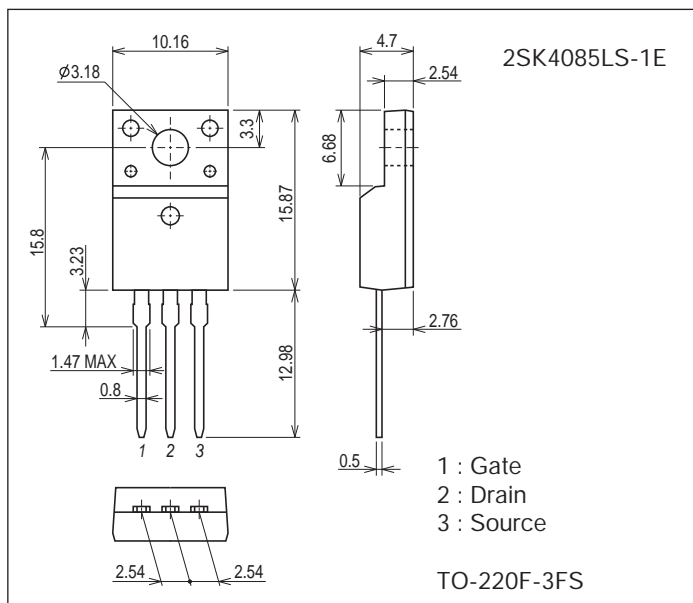
*4 $V_{DD}=50\text{V}$, $L=1\text{mH}$, $I_{AV}=16\text{A}$ (Fig.1)*5 $L \leq 1\text{mH}$, Single pulse

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

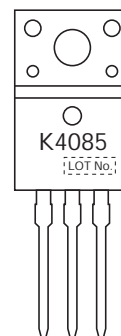
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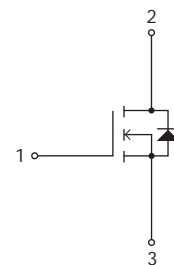
Product & Package Information

- Package : TO-220F-3FS
- JEITA, JEDEC : SC-67
- Minimum Packing Quantity : 50 pcs./magazine

Marking



Electrical Connection



2SK4085LS

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit	
			min.	typ.	max.		
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=10mA, V_{GS}=0V$	500			V	
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS}=400V, V_{GS}=0V$			100	μA	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$			± 100	nA	
Cutoff Voltage	$V_{GS(off)}$	$V_{DS}=10V, I_D=1mA$	3		5	V	
Forward Transfer Admittance	$ y_{fs} $	$V_{DS}=10V, I_D=8A$	4.5	9		S	
Static Drain-to-Source On-State Resistance	$R_{DS(on)}$	$I_D=8A, V_{GS}=10V$		0.33	0.43	Ω	
Input Capacitance	C_{iss}	$V_{DS}=30V, f=1MHz$		1200		pF	
Output Capacitance	C_{oss}				250		pF
Reverse Transfer Capacitance	C_{rss}				55		pF
Turn-ON Delay Time	$t_{d(on)}$	See Fig.2		26.5		ns	
Rise Time	t_r				78		ns
Turn-OFF Delay Time	$t_{d(off)}$				146		ns
Fall Time	t_f				57		ns
Total Gate Charge	Q_g	$V_{DS}=200V, V_{GS}=10V, I_D=16A$		46.6		nC	
Gate-to-Source Charge	Q_{gs}				8.2		nC
Gate-to-Drain "Miller" Charge	Q_{gd}				27.4		nC
Diode Forward Voltage	V_{SD}	$I_S=16A, V_{GS}=0V$		0.95	1.3	V	

Fig.1 Avalanche Resistance Test Circuit

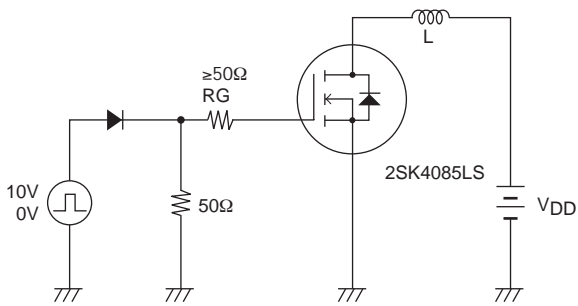
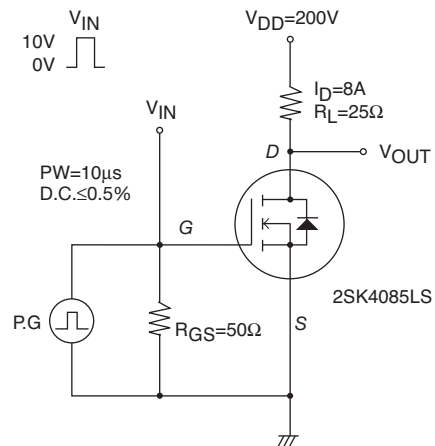


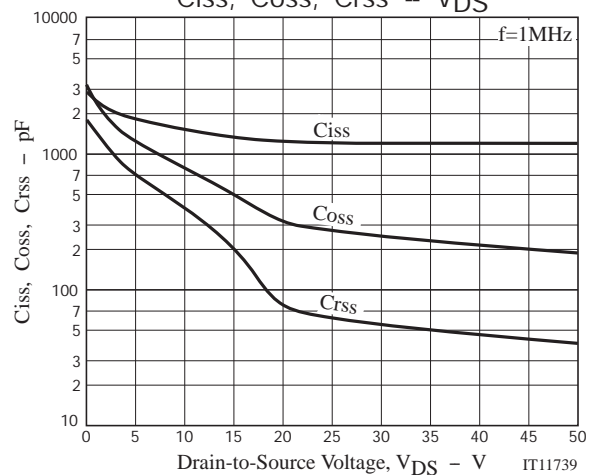
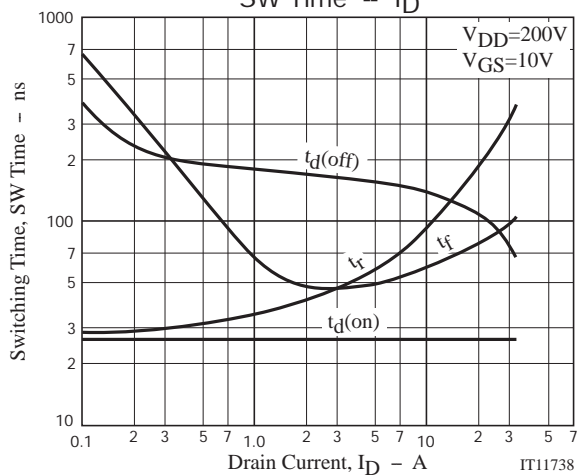
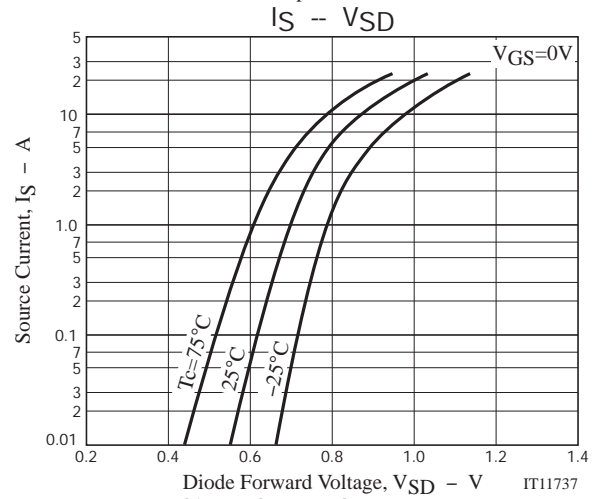
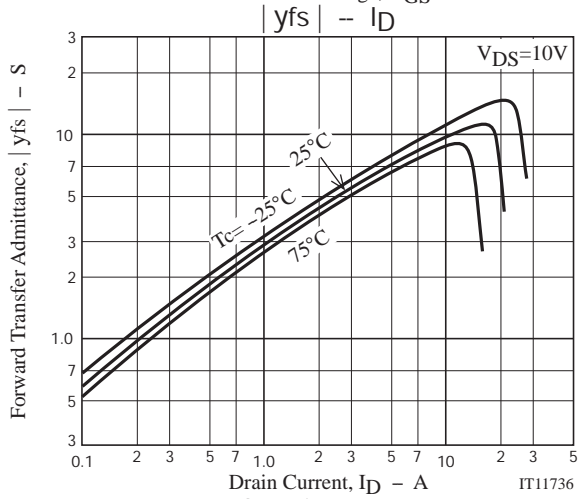
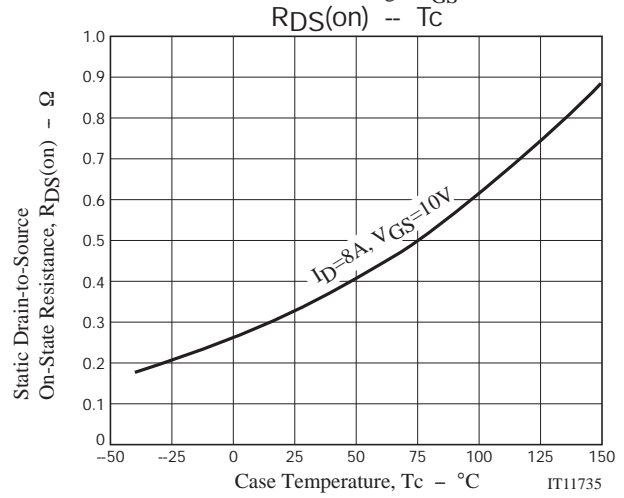
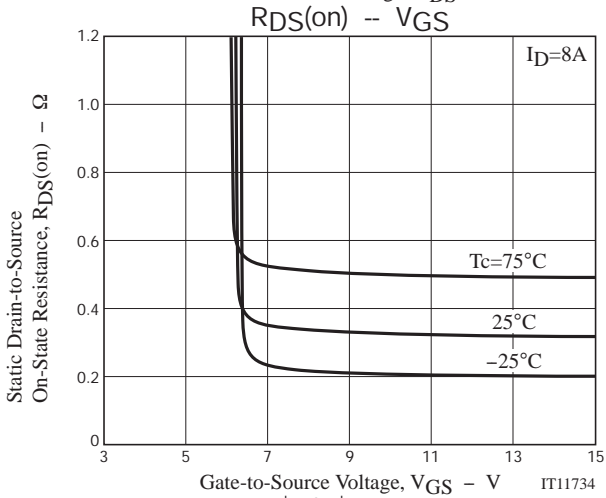
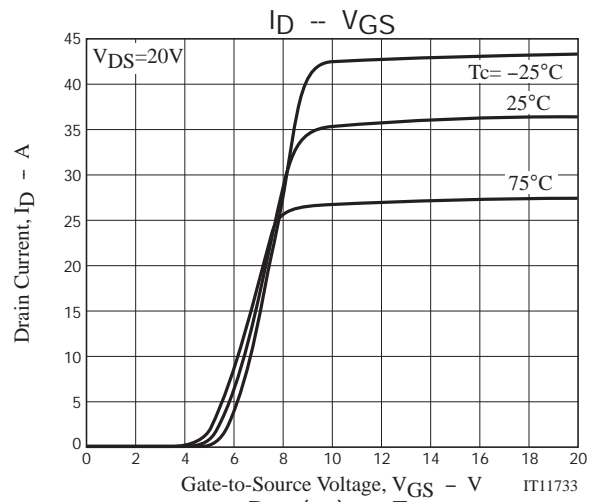
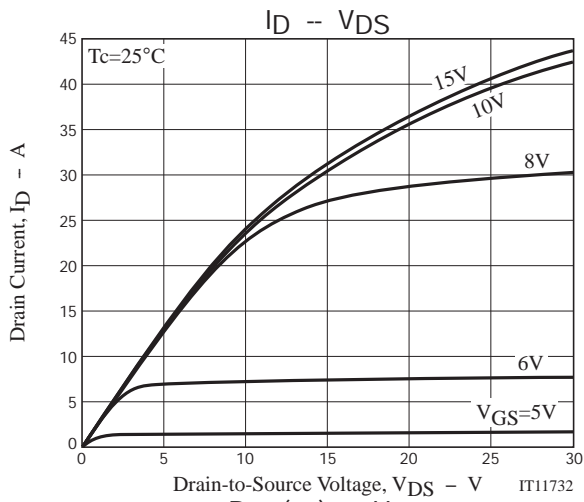
Fig.2 Switching Time Test Circuit



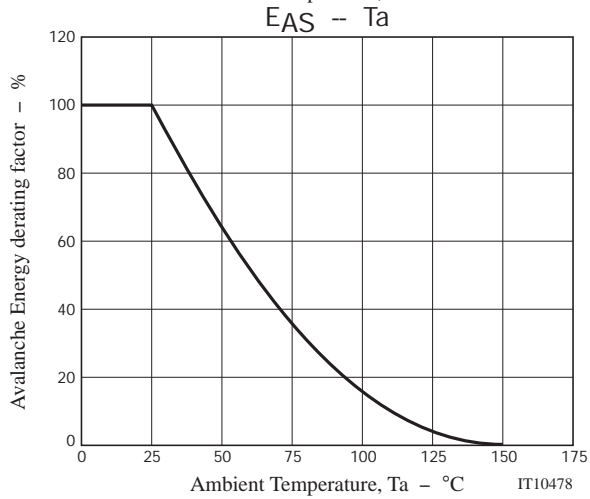
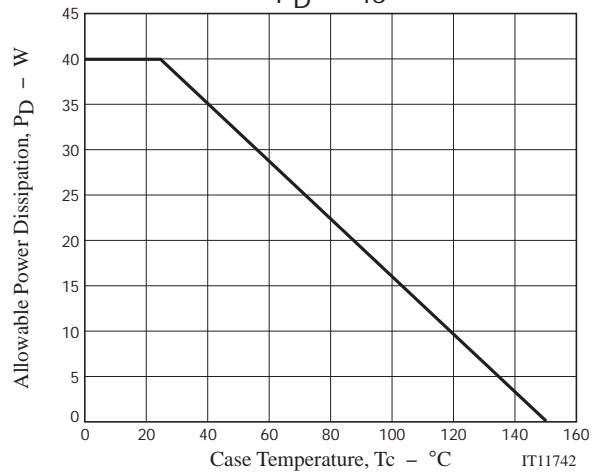
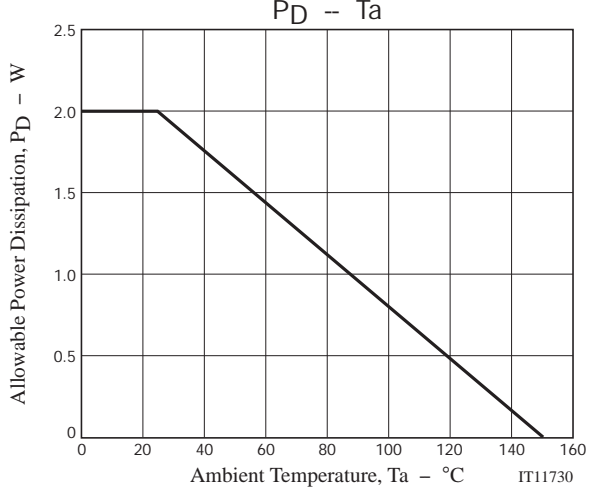
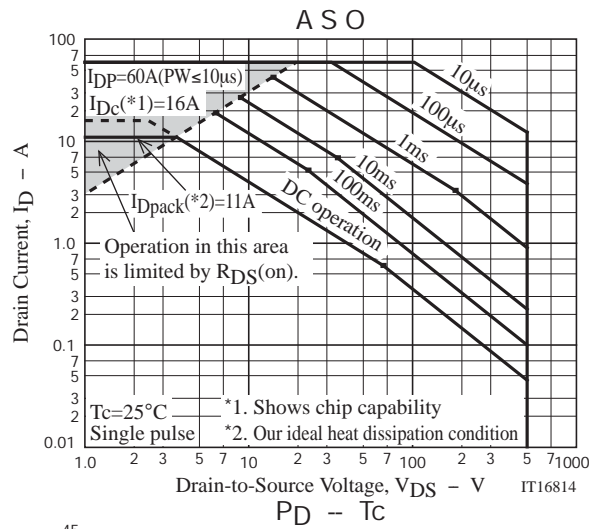
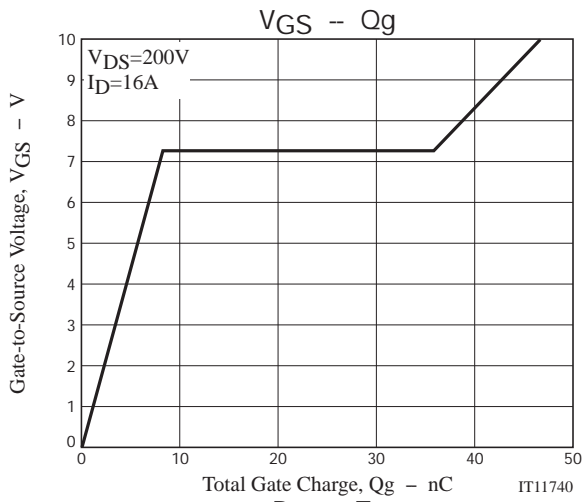
Ordering Information

Device	Package	Shipping	memo
2SK4085LS-1E	TO-220F-3FS	50pcs./magazine	Pb Free

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Magazine Specification

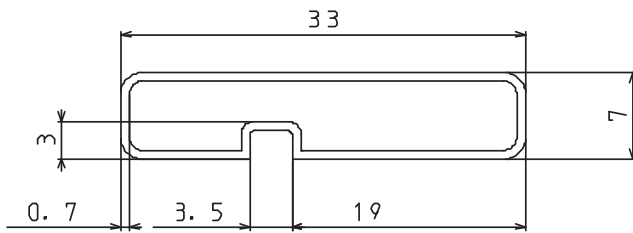
2SK4085LS-1E

1. Packing Format

Package Name	Magazine Name	Maximum Number of devices contained (pcs)			Packing format	
		Magazine	Inner box	Outer box	Inner BOX	Outer BOX
TO-220F-3FS	TO-220F	50	1,000	4,000	SPD-0V0001 20 magazines contained Dimensions:mm {external} 568×150×55	SPT-081029 4 inner boxes contained Dimensions:mm {external} 590×225×178

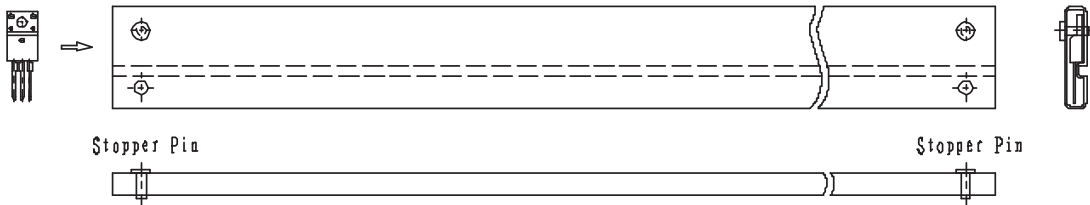
2. Magazine dimensions

(unit:mm)

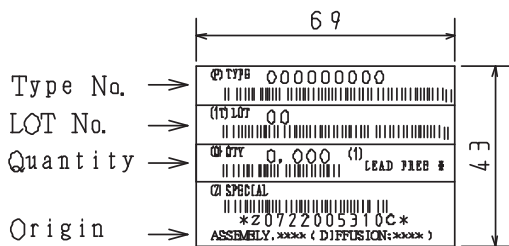


Tolerance=±0.3mm
 Thickness=0.7±0.2mm
 Length =532.5±2mm
 Material =PVC (Antistatic treatment)

3. Storage method to magazine

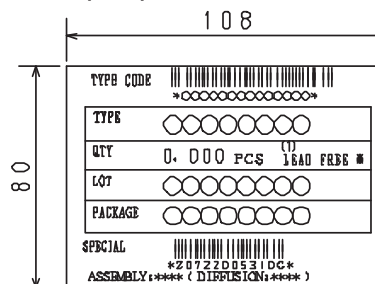


4. Inner box label (unit:mm)



5. Outer box label (unit:mm)

It is a label at the time of factory shipments.
 The form of a label may change in physical
 distribution process.



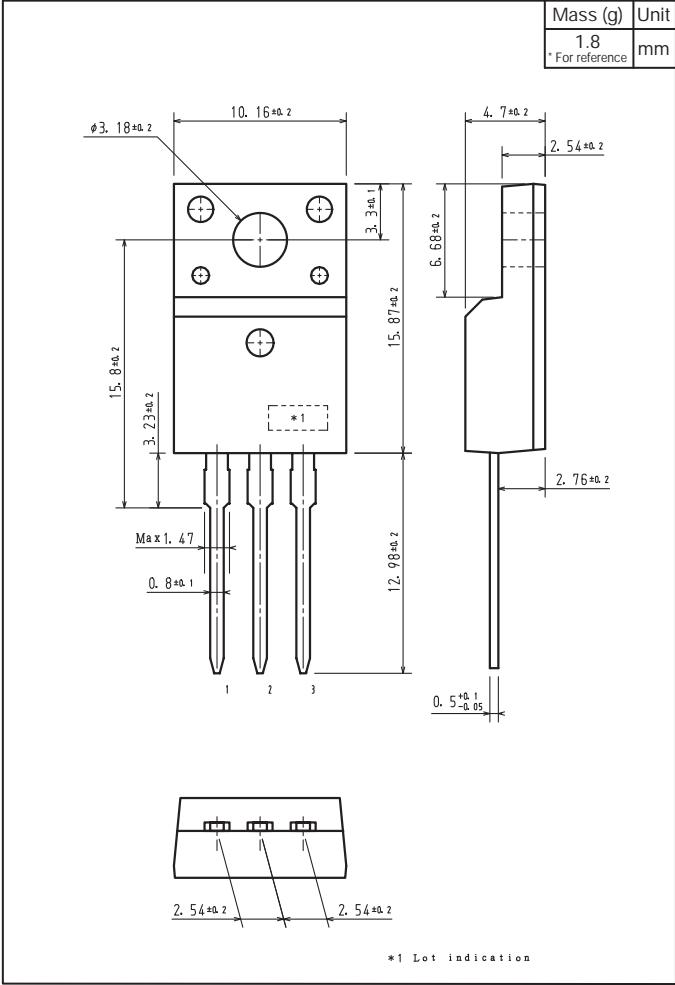
NOTE (1)

The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A

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Outline Drawing
2SK4085LS-1E



Note on usage : Since the 2SK4085LS is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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