



# **Peak EMI Reducing Solution**

#### **Features**

- Generates an EMI optimized clock signal at the output.
- Integrated loop filter components.
- Operates with a 3.3V Supply.
- · Operating current less than 6mA.
- · CMOS design.
- Input frequency range: 13MHz to 30MHz
- Generates a 1X and 2X low EMI spread spectrum clock of the input frequency.
- Output Frequency Selection through FSEL pin
- Frequency deviation: -1.5% (Typ) @25MHz
   -1.5% (Typ) @50MHz
- Available in 6L-TSOP (6L-TSOT-23) package.

#### **Product Description**

The ASM3P2474A is a versatile spread spectrum frequency modulator designed specifically for a wide range of clock frequencies. The ASM3P2474A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The ASM3P2474A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads and shielding that are traditionally required to pass EMI regulations.

The ASM3P2474A uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all digital method.

The ASM3P2474A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation.'

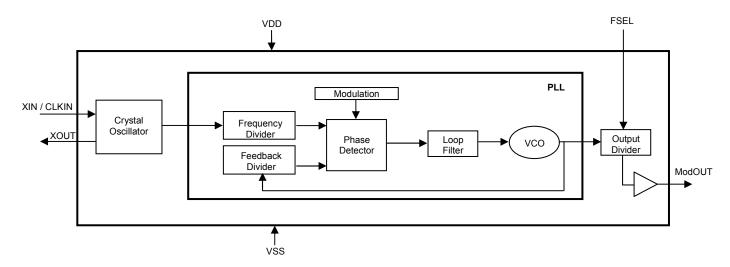
#### **Applications**

The ASM3P2474A is targeted towards all portable devices like MP3 players and digital still cameras.

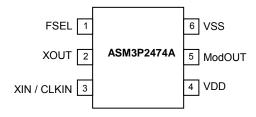
## **Key Specifications**

Description		Specification		
Supply voltages		VDD = 3.3V ± 0.3V		
Cycle-to-Cycle Jitt	ter	±200pS (Typ)		
Output Duty Cycle		45/55% (worst case)		
Modulation Rate E	Equation	F <sub>IN</sub> /640		
Frequency	FSEL=0	-1.5% (Typ) @ 50MHz		
Deviation	FSEL=1	-1.5% (Typ) @ 25MHz		

#### **Block Diagram**



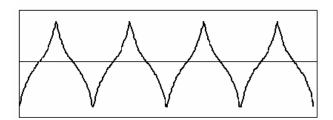
# Pin Configuration (6L-TSOP Package)



## **Pin Description**

Pin#	Pin Name	Туре	Description
1	FSEL	I	Selection Pin for 1X and 2X Output Frequency Options. Please refer to the table Frequency Selection Options for further details.
2	XOUT	0	Crystal connection. If using an external reference, this pin must be left unconnected.
3	XIN / CLKIN	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
4	VDD	Р	Power supply for the entire chip.
5	ModOUT	0	Spread spectrum clock output.
6	VSS	Р	Ground connection.

## **Modulation Profile**



## **Specifications**

Description	Specification		
Frequency Range	13MHz < CLKIN < 30MHz		
Modulation Equation	F <sub>IN</sub> /640		
Fraguency Deviation	FSEL=0	-1.5% (Typ) @ 50MHz	
Frequency Deviation	FSEL=1	-1.5% (Typ) @ 25MHz	

**Frequency Selection Options** 

FSEL Pin	Input Frequency (MHz)	Output Frequency (MHz)
0	13-30	26-60
1	13-30	13-30

**Absolute Maximum Ratings** 

on any pin with respect to Ground temperature oldering Temperature (10 sec)	-0.5 to +4.6 -65 to +125 260	V °C
·		-
oldering Temperature (10 sec)	260	3
• ,	200	
n Temperature	150	${\mathfrak C}$
	2	KV
)	n Temperature  Discharge Voltage  JEDEC STD22- A114-B) s only and are not implied for functional use. Exposure to absolute maximum ratings	Discharge Voltage 2

**Operating Conditions** 

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3	3.6	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)	0	70	${\mathcal C}$
$C_L$	Load Capacitance		15	pF
C <sub>IN</sub>	Input Capacitance		7	pF

## **DC Electrical Characteristics**

Symbol	Parameter	Min	Тур	Max	Unit
V <sub>IL</sub>	Input low voltage	VSS-0.3		0.8	V
V <sub>IH</sub>	Input high voltage	2.0		VDD+0.3	V
I <sub>IL</sub>	Input low current			-35	μΑ
I <sub>IH</sub>	Input high current			35	μΑ
I <sub>XOL</sub>	XOUT output low current (@ 0.4V, VDD = 3.3V)		3		mA
I <sub>XOH</sub>	XOUT output high current (@ 2.5V, VDD = 3.3V)		3		mA
V <sub>OL</sub>	Output low voltage (VDD = 3.3V, I <sub>OL</sub> = 8mA)			0.4	V
V <sub>OH</sub>	Output high voltage (VDD = 3.3V, I <sub>OH</sub> = 8mA)	2.5			V
I <sub>DD</sub>	Static supply current <sup>1</sup>		1.6		mA
Icc	Dynamic supply current (3.3V, 25MHz and no load and FSEL=1)		4.0		mA
VDD	Operating voltage	3.0	3.3	3.6	V
ton	Power-up time (first locked cycle after power-up)			5	mS
Z <sub>OUT</sub>	Output impedance		45		Ω
Note: 1. XIN	CLKIN pin is pulled low.		•		•

## **AC Electrical Characteristics**

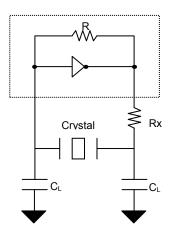
Symbol	Р	Parameter		Тур	Max	Unit	
CLKIN	Input frequency	Input frequency			30	MHz	
MAJOUT	Output fraguancy	FSEL = 0	26		60	MHz	
ModOUT	Output frequency	Output frequency FSEL = 1	13		30		
r	Francisco Deviation	Output Frequency = 13MHz		-1.8		%	
f <sub>d</sub>	Frequency Deviation	Frequency Deviation Output Frequency = 30MHz		-0.9			
_	· · ·	Output Frequency = 26MHz		-1.8		%	
f <sub>d</sub>	Frequency Deviation	Output Frequency = 60MHz		-0.9			
t <sub>LH</sub> <sup>1</sup>	Output rise time (meas	Output rise time (measured from 0.8 to 2.0V)			1.1	nS	
t <sub>HL</sub> 1	Output fall time (meas	Output fall time (measured at 2.0V to 0.8V)		0.7	0.9	nS	
t <sub>JC</sub>	Jitter (cycle-to-cycle)			±200		pS	
$t_D$	Output duty cycle	Output duty cycle		50	55	%	
Note: 1. t <sub>LH</sub> and t <sub>HL</sub> are mea	Note: 1. t <sub>LH</sub> and t <sub>HL</sub> are measured into a capacitive load of 15pF.						

## **Typical Crystal Specifications**

Fundamental AT cut parallel resonant crystal				
Nominal frequency	25MHz			
Frequency tolerance	± 30 ppm or better at 25℃			
Operating temperature range	-25℃ to +85℃			
Storage temperature	-40℃ to +85℃			
Load capacitance(C <sub>P</sub> )	18pF			
Shunt capacitance	7pF maximum			
ESR	25 Ω			

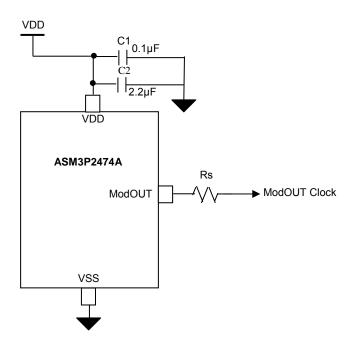
Note: Note: C<sub>L</sub> is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

## **Typical Crystal Interface Circuit**



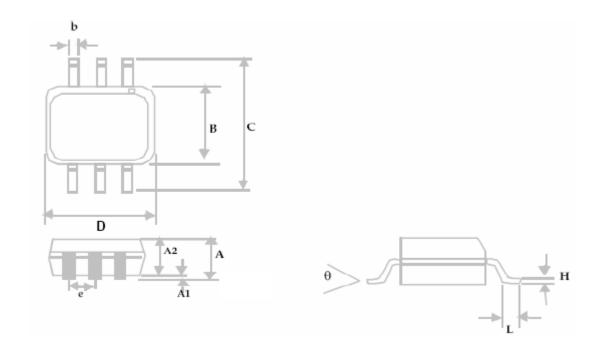
$$\begin{split} C_L &= 2^*(C_P - C_S), \\ \text{Where } C_P &= Load \text{ capacitance of crystal} \\ C_S &= \text{Stray capacitance due to } C_{\text{IN,}} \text{ PCB, Trace etc.} \end{split}$$

# **Typical Application Schematic**



# **Package Information**

# **6L-TSOP Package**



	Dimensions				
Symbol	Inc	hes	Millim	neters	
	Min	Max	Min	Max	
Α		0.04		1.00	
A1	0.00	0.004	0.00	0.10	
A2	0.033	0.036	0.84	0.90	
b	0.012	0.02	0.30	0.50	
Н	0.005 BSC		0.127 BSC		
D	0.114 BSC		2.90 BSC		
В	0.06 BSC		1.60 BSC		
е	0.0374 BSC		0.950 BSC		
С	0.11 BSC		2.80 BSC		
L	0.0118	0.02	0.30	0.50	
θ	0°	4°	0°	4°	

**Ordering Information** 

Part Number	Marking	Package Type	Temperature
ASM3P2474AF-06OR	W4L	6L-TSOP (6L-TSOT-23), TAPE & REEL, Pb Free	0℃ to +70℃

A "microdot" placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. U.S Patent Pending; Timing-Safe and Active Bead are trademarks of PulseCore Semiconductor, a wholly owned subsidiary of ON Semiconductor. This literature is subject to all applicable copyright laws

#### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA **Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada

Fax: 303-675-2176 or 800-344-3867 Toll Free

USA/Canada

Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Europe, Middle East and Africa Technical

Support:

Phone: 421 33 790 2910 Japan Customer Focus Center

Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your

local Sales Representative