BDX53B, BDX53C (NPN), BDX54B, BDX54C (PNP)

Plastic Medium-Power Complementary Silicon Transistors

These devices are designed for general−purpose amplifier and low−speed switching applications.

Features

- High DC Current Gain −
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector Emitter Sustaining Voltage − @ 100 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (Min) − BDX53B, 54B
  = 100 Vdc (Min) − BDX53C, 54C
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- These Devices are Pb−Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage BDX53B, BDX54B BDX53C, BDX54C	V_{CEO}	 80 100	Vdc
Collector−Base Voltage BDX53B, BDX54B BDX53C, BDX54C	V_{CB}	 80 100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous − Peak	I_C	8.0 12	Adc
Base Current	I_B	0.2	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.48	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

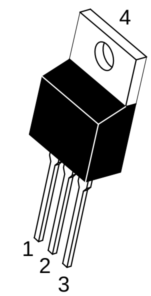
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.92	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

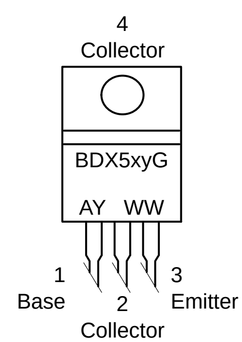
www.onsemi.com

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
80−100 VOLTS, 65 WATTS



TO−220
CASE 221A
STYLE 1

MARKING DIAGRAM & PIN ASSIGNMENT



BDX5xy	=	Device Code x = 3 or 4 y = B or C
A	=	Assembly Location
Y	=	Year
WW	=	Work Week
G	=	Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

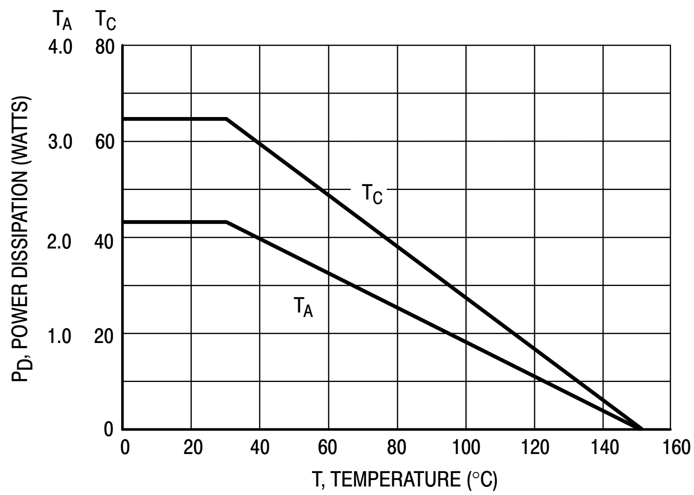


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 100 mAdc, I_B = 0) BDX53B, BDX54B BDX53C, BDX54C	$V_{CEO(sus)}$	 80 100	 – –	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) BDX53B, BDX54B (V_{CE} = 50 Vdc, I_B = 0) BDX53C, BDX54C	I_{CEO}	 – –	 0.5 0.5	mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0) BDX53B, BDX54B (V_{CB} = 100 Vdc, I_E = 0) BDX53C, BDX54C	I_{CBO}	 – –	 0.2 0.2	mAdc
ON CHARACTERISTICS (Note 1)				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	750	–	–
Collector−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc)	$V_{CE(sat)}$	– –	2.0 4.0	Vdc
Base−Emitter Saturation Voltage (I_C = 3.0 Adc, I_C = 12 mA)	$V_{BE(sat)}$	–	2.5	Vdc
DYNAMIC CHARACTERISTICS				
Small−Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)	h_{fe}	4.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) BDX53B, 53C BDX54B, 54C	C_{ob}	 – –	 300 200	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

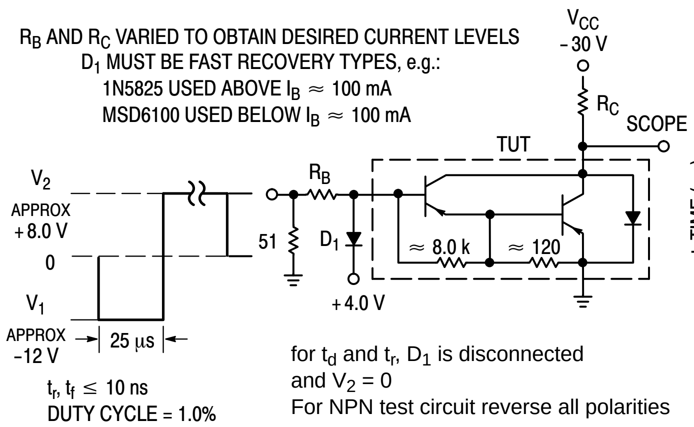


Figure 2. Switching Time Test Circuit

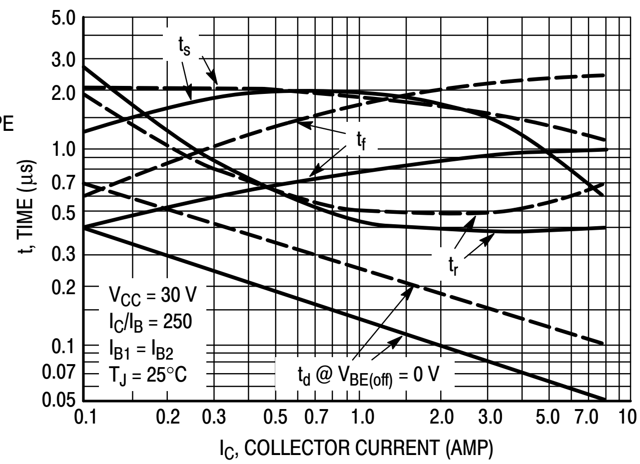


Figure 3. Switching Times

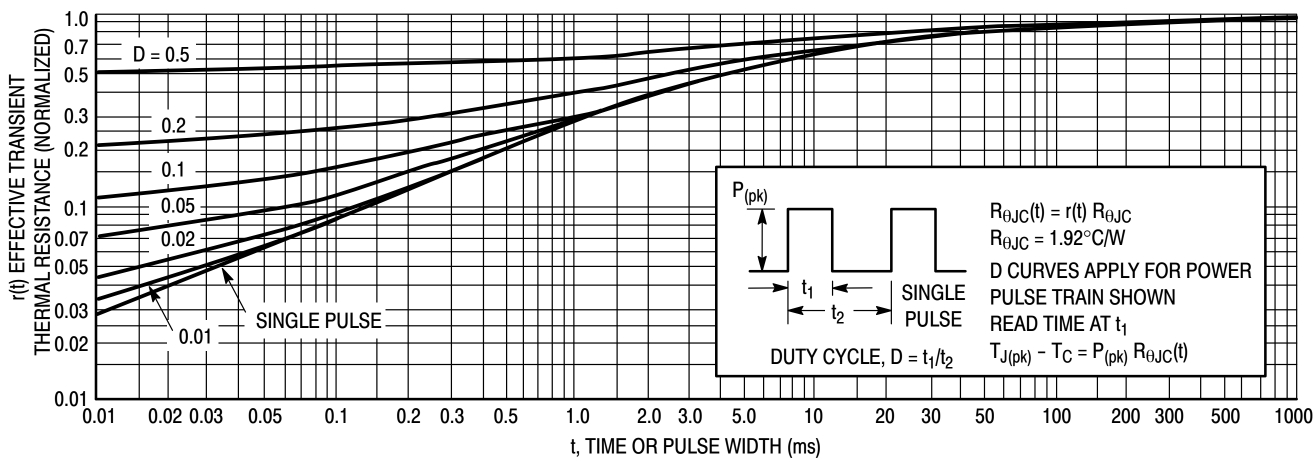


Figure 4. Thermal Response

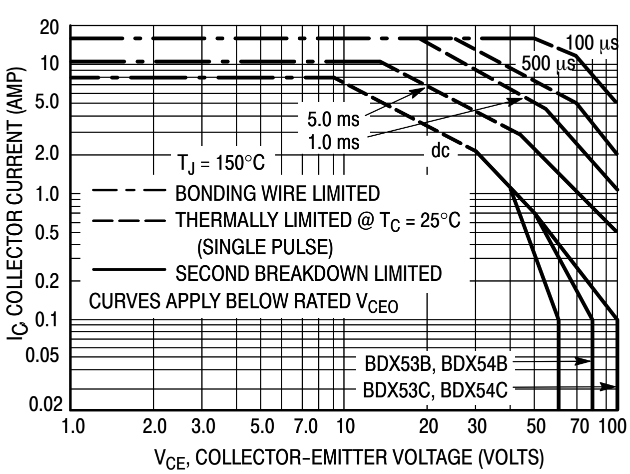


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

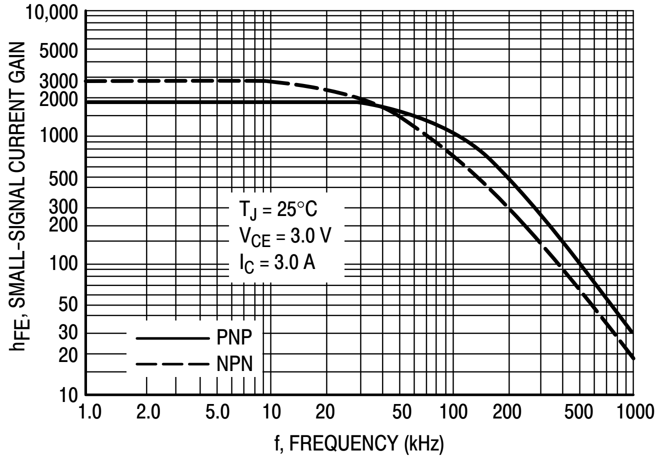


Figure 6. Small-Signal Current Gain

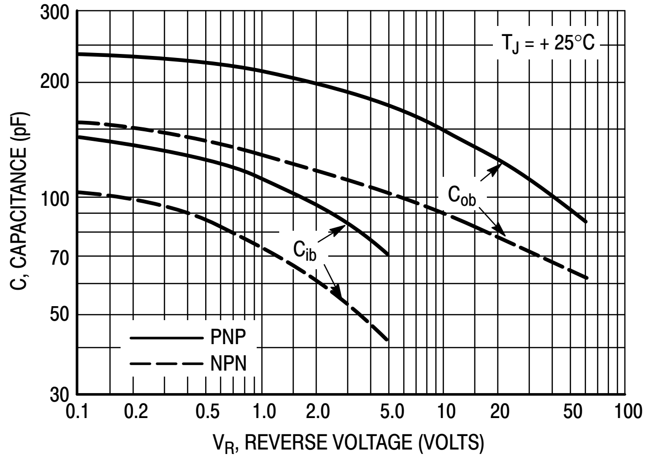


Figure 7. Capacitance

NPN
BDX53B, 53C

PNP
BDX54B, 54C

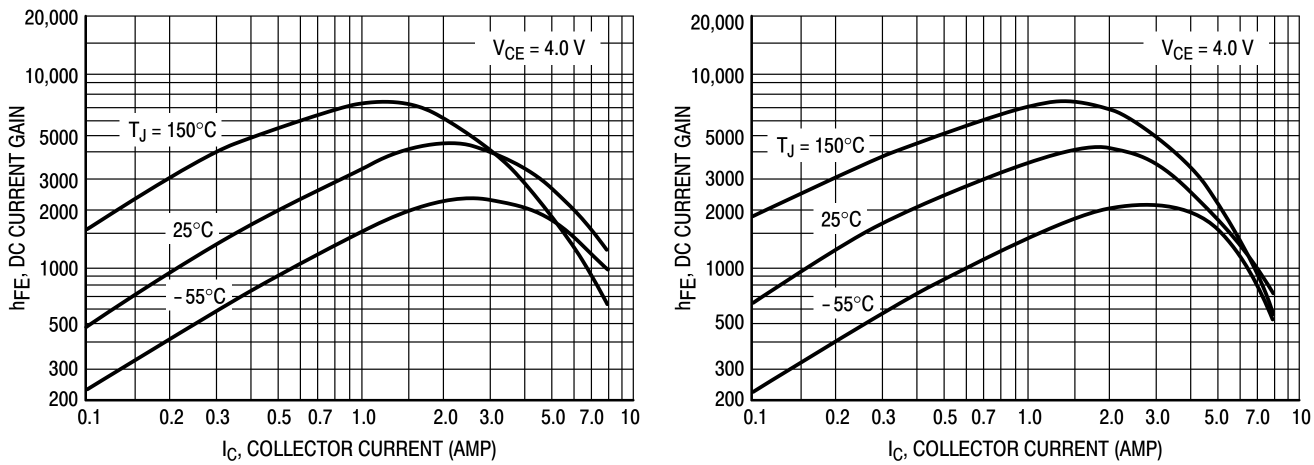


Figure 8. DC Current Gain

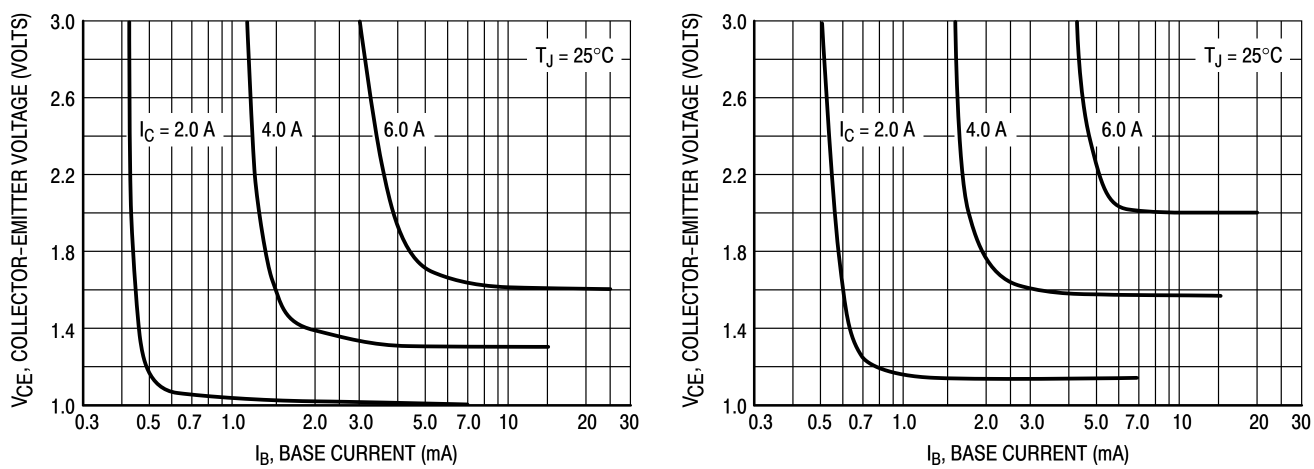
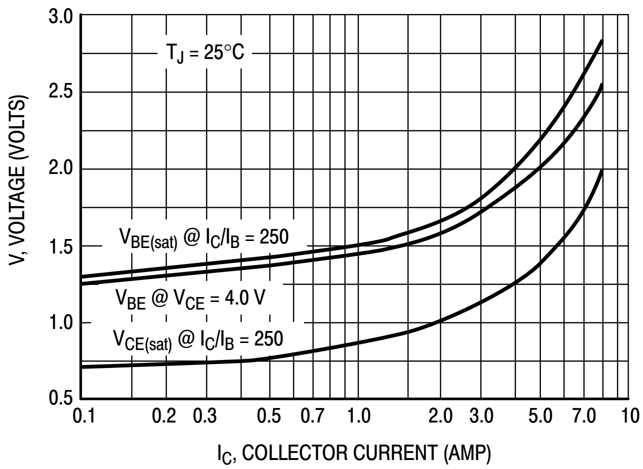


Figure 9. Collector Saturation Region



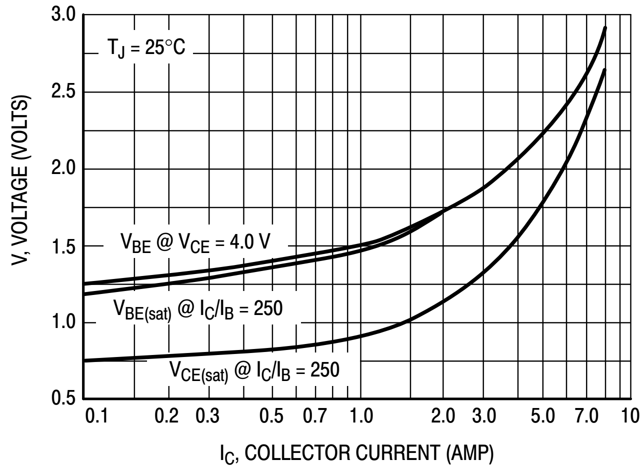
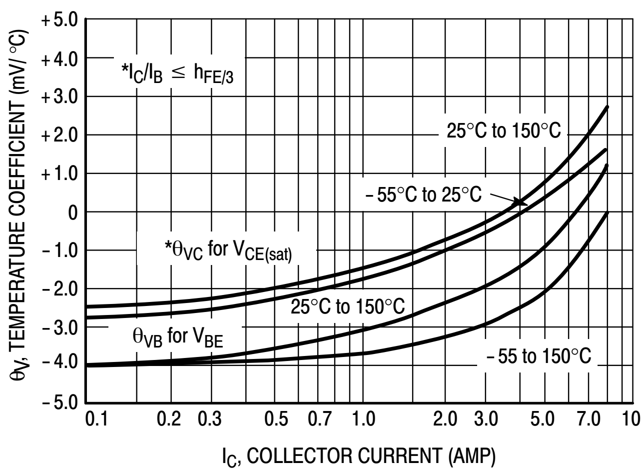


Figure 10. "On" Voltages

NPN
BDX53B, BDX53C



PNP
BDX54B, BDX54C

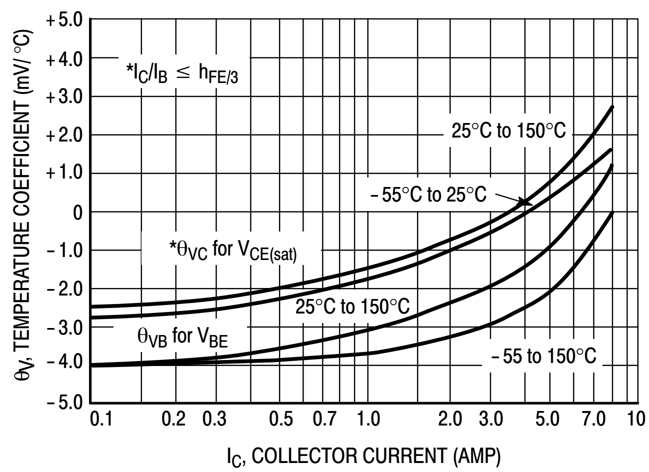
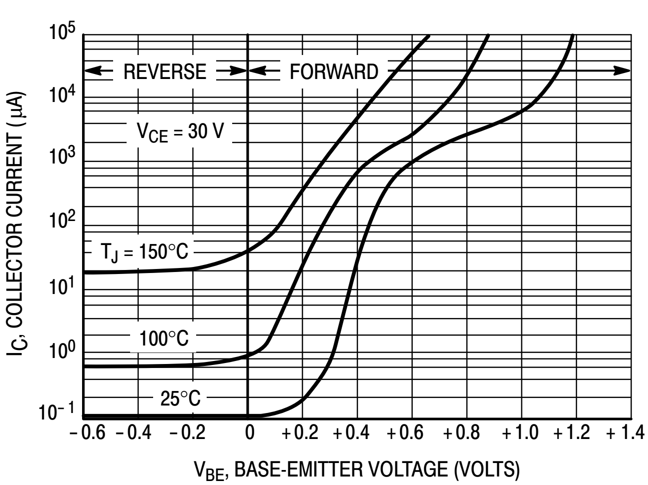


Figure 11. Temperature Coefficients



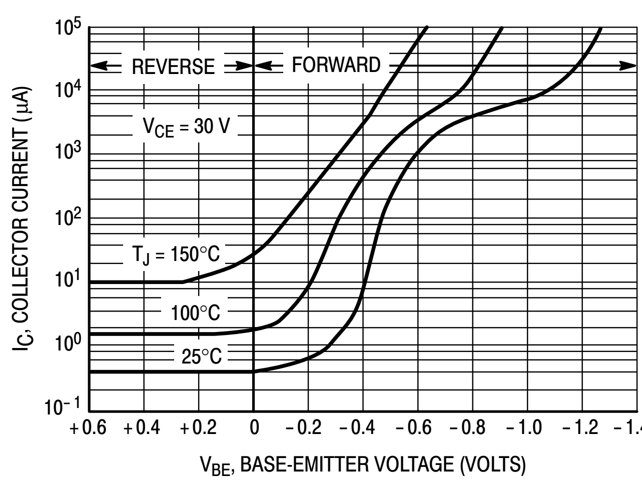


Figure 12. Collector Cut−Off Region

Figure 13. Darlington Schematic

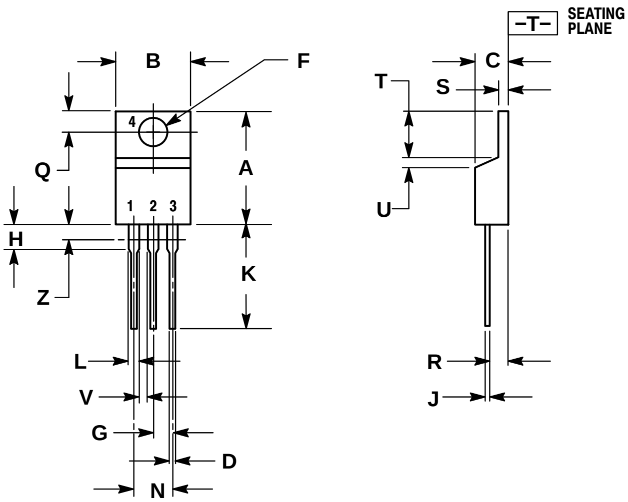
ORDERING INFORMATION

Device	Package	Shipping†
BDX53BG	TO−220 (Pb−Free)	50 Units / Rail
BDX53CG	TO−220 (Pb−Free)	50 Units / Rail
BDX54BG	TO−220 (Pb−Free)	50 Units / Rail
BDX54CG	TO−220 (Pb−Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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