NB6L239MNEVB

NB6L239MNEVB Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Description

The NB6L239 Evaluation Board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the performance and operation of the NB6L239. This user's manual provides detailed information on board contents, layout and its use. It should be used in conjunction with the NB6L239 data sheet: (www.onsemi.com).

The NB6L239 is a differential Receiver to differential LVPECL Clock Divider. The board features Output Enable control of the Outputs.

Board Features

- Accommodates the electrical characterization of the NB6L239
- Selectable Jumper for the VT pin, minimizing cabling
- CLK/$\overline{\text{CLK}}$ input and QA/$\overline{\text{QA}}$ and QB/$\overline{\text{QB}}$ output pins are accessed via SMA connectors
- $\overline{\text{MR}}$, $\overline{\text{EN}}$ and Clock Divide Select pins are accessed via SMA Connectors or by the Logic Switches
- Convenient and compact board layout
- 2.5 V, 3.3 V Power Supply Operating Range

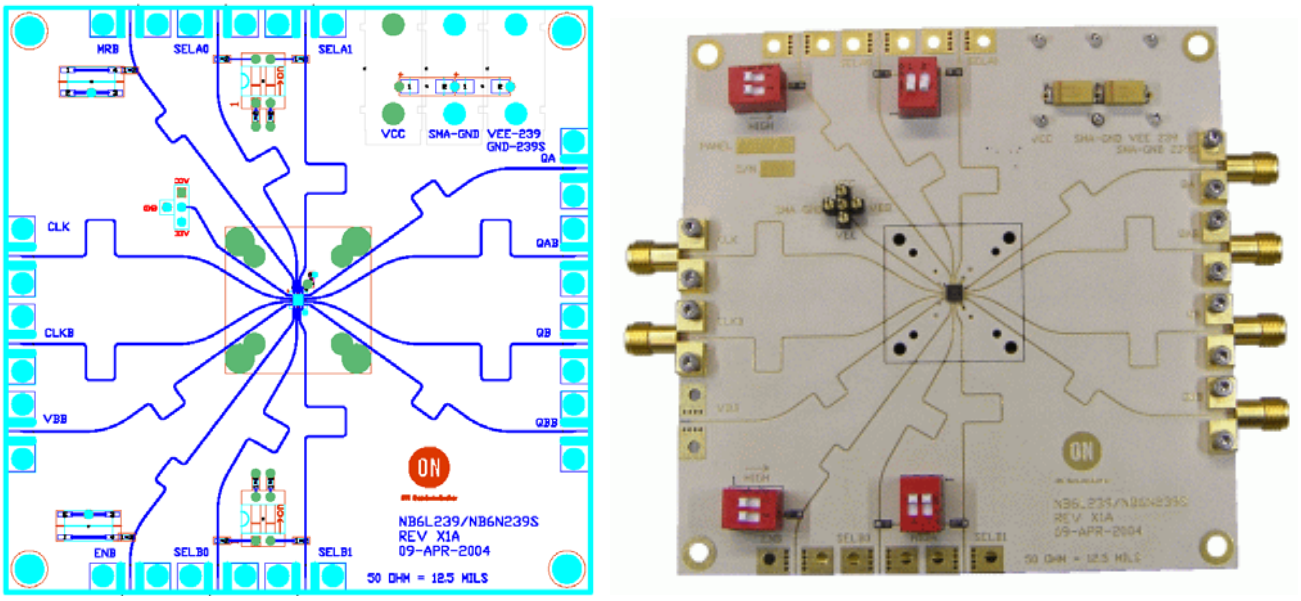


Figure 1. Evaluation Board

PROCEDURE

Lab Setup and Measurement Procedure

Equipment Used

- Agilent Signal Generator #8133A
- Tektronix TDS8000 Oscilloscope
- Agilent #6624A DC Power Supply
- Digital Voltmeter
- Matched High−Speed Cables with SMA Connectors

Power Supply Connections

The NB6L239 has a positive supply pin, V_{CC}, and a negative supply pin, V_{EE}. SMAGND = V_{TT} = V_{CC} – 2.0 V is the termination supply for the LVPECL outputs, only.

Power supply terminals V_{CC}, V_{EE} and SMAGND are provided. The SMAGND terminal is for the isolated SMA connector GROUND plane, and is not to be confused with a device V_{EE} pin. Since SMAGND = V_{TT} = V_{CC} – 2.0 V, is the termination supply for the LVPECL outputs, by offsetting V_{CC} by +2.0 V yields V_{TT} = 0 V or Ground. A "split" or dual power supply technique can be used to take advantage of terminating the PECL outputs into 50 Ω to Ground of an oscilloscope or a frequency counter. (see AND8020/D for more information on terminating ECL).

Table 1. POWER SUPPLY CONFIGURATIONS

Device Pin	Power Supply Connector Color	"Spilt" Power Supply
V_{CC}	RED	V_{CC} = +2.0 V
–	BLACK – SMAGND	V_{TT} = V_{CC} – 2 V = 0 V
V_{EE} – 239	YELLOW	V_{EE} = −1.3 V (or −0.5 V)

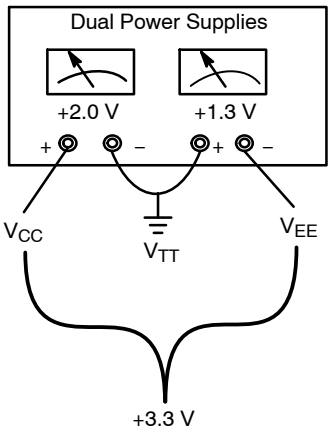


Figure 2. "Split" or Dual Power Supply Connections

NB6L239

To monitor the QA/$\overline{QA}$ and QB/$\overline{QB}$ outputs on an oscilloscope, the power supply needs to be DC offset:

1. Connect a "split" power supply to the evaluation board. (Figure 1)
   Connect V_{CC} to +2.0 V
   Connect SMAGND to 0 V
   Connect V_{EE} to −1.3 V for 3.3 V operation; or –0.5 V for 2.5 V operation
2. Ensure the oscilloscope is triggered properly and has 50 Ω termination to ground. The board does not provide 50 Ω source termination resistors. Trigger the oscilloscope from trigger output of signal generator.
3. Connect the LVPECL QA/$\overline{QA}$ and QB/$\overline{QB}$ outputs to the oscilloscope with matched cables. The outputs are terminated with 50 Ω to V_{TT} (V_{CC} – 2.0 V) = 0 V = Ground internal to the oscilloscope.

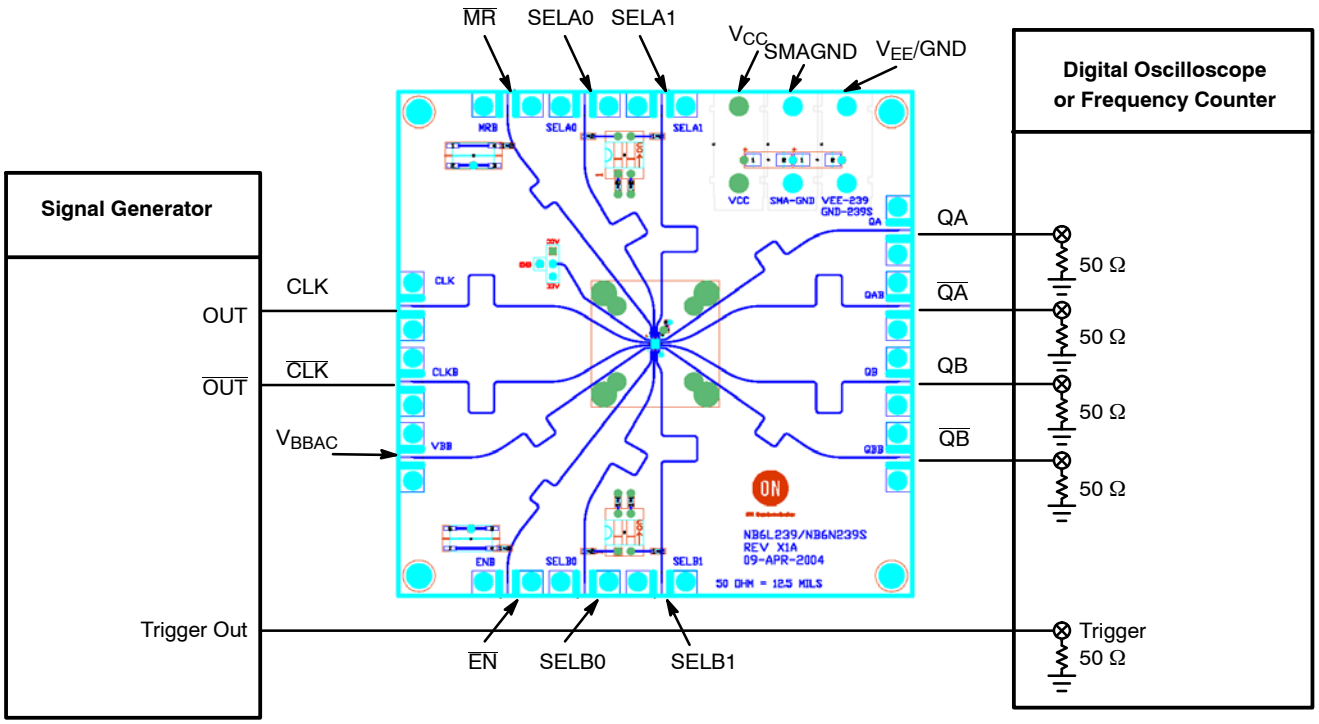


Figure 3. Evaluation Board

Board Layout

The evaluation board is constructed with Rogers material with 50 Ω trace impedances designed to minimize noise, achieve high bandwidth and minimize crosstalk.

Layer Stack

L1 Signal (top) (Rogers)
L2 SMA Ground
L3 V_{CC} and V_{EE} (positive and negative power supply)
L4 Signal (bottom)

Control and Select Pins

The Control / Select pins, $\overline{MR}$, SELXn and $\overline{EN}$, can be accessed via the appropriate SMA connector. These pins can also be manually controlled by using the H/L switch. When using the switch, the SMA connector should be left open. When using the SMA connector, the switch must be in the "OPEN" position.

The SELXn and $\overline{EN}$ device pins have internal pulldown resistors. The NB6L239 evaluation board was designed to take advantage of this attribute. When the SELXn and $\overline{EN}$ switch is in the logic LOW position, the input pin "floats" to a logic LOW owing to the pulldown resistor; a logic LOW voltage is not forced on the pin. In the HIGH position, the switch forces the SELXn and $\overline{EN}$ pin to the positive power supply rail, a logic HIGH.

The $\overline{MR}$ device pin has an internal pullup resistor. When the $\overline{MR}$ switch is in the logic HIGH position, the input pin "floats" to a logic HIGH owing to the pullup resistor; a logic HIGH voltage is not forced on the pin. In the LOW position, the switch forces the $\overline{MR}$ pin to the negative power supply rail, a logic LOW.

V_{BB} = V_{BBAC}

V_{BB} labeled on the board is actually V_{BBAC} per the data sheet.

V_T

The V_T pin can be set to V_{CC}, V_{EE} (239) GND (239S), V_{BB} or SMAGND by using a jumper.

V_{EE} / GND

V_{EE} is the negative supply for the NB6L239. GND is the negative supply for NB6N239S.

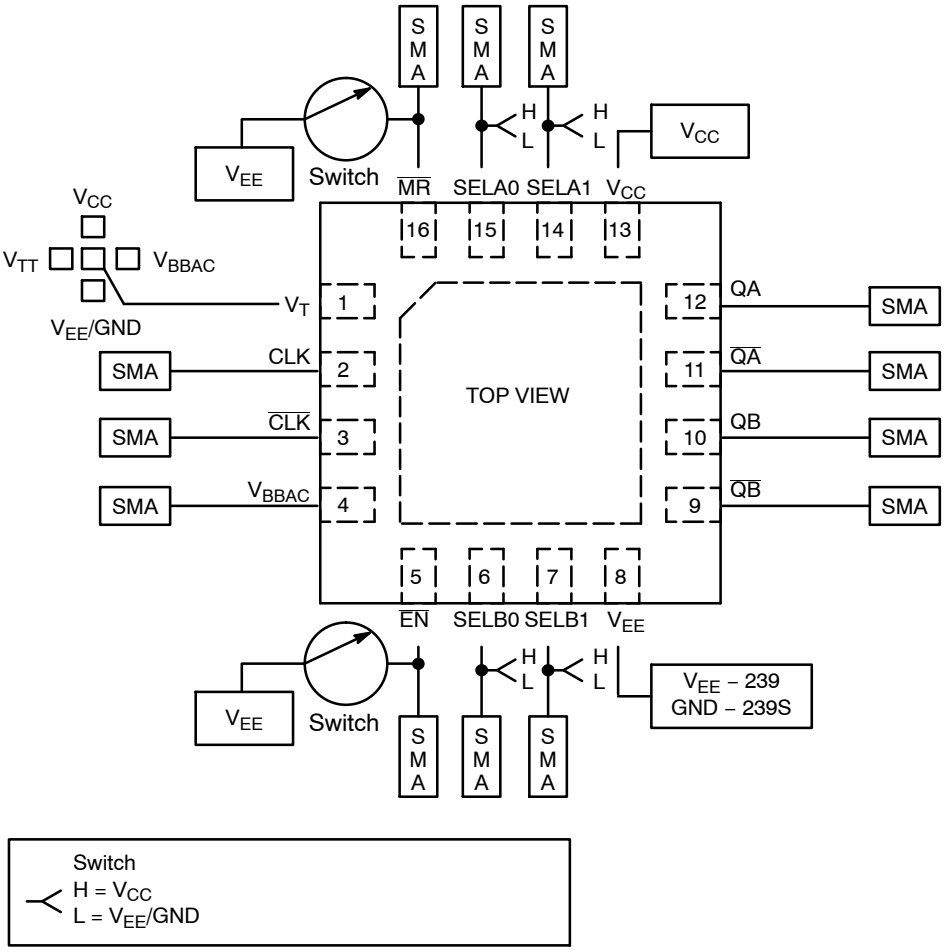
Table 2. PIN DESCRIPTION (refer to data sheet, NB6L239/D)

Pin # 16−QFN	Pin Name	I/O	Open Pin Default	Type	Function
1	VT				Internal 100 Ω Center
2	CLK	Input		LVPECL, CML, LVDS, HSTL	Noninverted Differential CLOCK Input.
3	$\overline{CLK}$	Input		LVPECL, CML, LVDS, HSTL	Inverted Differential CLOCK Input.
4	V_{BBAC}	Output		Reference Voltage	Output Voltage Reference for Capacitor Coupled Inputs, Only.
5	$\overline{EN}$	Input	L	LVCMOS/LVTTL Input	Synchronous Output Enable
6	SELB0	Input	L	LVCMOS/LVTTL Input	Clock Divide Select Pin
7	SELB1	Input	L	LVCMOS/LVTTL Input	Clock Divide Select Pin
8	V_{EE}	Negative Power Supply			Negative Supply Voltage
9	$\overline{QB}$	Output		LVPECL	Inverted Differential Output. Typically terminated with 50 Ω resistor to V_{TT}.
10	QB	Output		LVPECL	Noninverted Differential Output. Typically terminated with 50 Ω resistor to V_{TT}.
11	$\overline{QA}$	Output		LVPECL	Inverted Differential Output. Typically terminated with 50 Ω resistor to V_{TT}.
12	QA	Output		LVPECL	Noninverted Differential Output. Typically terminated with 50 Ω resistor to V_{TT}.
13	V_{CC}	Positive Power Supply			Positive Power Supply
14	SELA1	Input	L	LVCMOS/LVTTL	Clock Divide Select Pin
15	SELA0	Input	L	LVCMOS/LVTTL Input	Clock Divide Select Pin
16	$\overline{MR}$	Input	H	LVCMOS/LVTTL Input	Master Reset Asynchronous, Default Open High, Asserted LOW
	EP	Negative Power Supply (opt)			The Exposed Pad on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to V_{EE} on the PC board.

EVALUATION BOARD APPLICATION INFORMATION

Table 3. EVALUATION BOARD BILL OF MATERIALS

Component	Description	Qty
Connector	Rosenberger SMA #32K243−40ME3	6
Capacitor	22 μF, 10%, KEMET T491D226K016AS, Case C or D	2
Capacitor	0.1 μF, 10%, KEMET C060C104K5RAC	4
Switch	Grayhill #78B02	4
Jumper Header	100 mil, Berg	5
Jumper/Shunt		1
Resistor	1 kΩ, 0603	6
Banana Jack	Deltron #EF681 150−039 Red	1
Banana Jack	Deltron #EF681 150−040 Black	1
Banana Jack	Deltron #EF681 150−043 Yellow	1
Stand−offs with Screws	Optional	4
NB6L239 or NB6N239S	QFN−16 Part Mounted on Board	1
QFN−16 Socket	Optional, M&M #50−000−00350	1



Rosenberger connectors with matched trace launches
Switch for $\overline{MR}$
Normally open switch for $\overline{EN}$
CLK & $\overline{CLK}$ traces – equal length
All Q Output traces – equal length
"Side–mount" banana jacks for power supplies (can be located on backside of board)
V_T pin has a "jumper capability to V_{CC}, V_{EE} / GND, V_{TT} (SMAGND), or V_{BBAC}

Figure 4. Evaluation Demo Board

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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