

NLAS7222CMUGEVB

NLAS7222C High-Speed USB 2.0 (480 Mbps) DPDT Switch Evaluation Board User's Manual



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EVAL BOARD USER'S MANUAL

Introduction

This evaluation board has been designed for a quick evaluation of the NLAS7222C. The NLAS7222C is a 2-to-1 analog switch designed for USB 2.0 signals, as shown in the block diagram in Figure 1 on the right. Among its main characteristics, this evaluation board has been constructed to easily interface with a customer's systems and equipment through USB connectors. The evaluation board can be seen in Figure 2 below.

This manual provides a bill of materials, board schematic, and a layout overview of the evaluation board. The appropriate setup to evaluate the device is also provided.

This document must be used with the NLAS7222C datasheet available on www.onsemi.com. The datasheet contains full technical details about the specifications and operation of the device. When the intention is to evaluate the device considering the specifications given in the datasheet, it is important to take into account the additional circuitry which may include changes in the characteristic impedance matching.

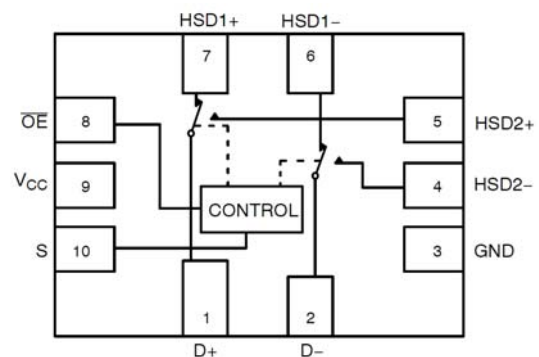


Figure 1. Block Diagram of NCN7222C



Figure 2. Evaluation Board

NLAS7222CMUGEVB

TEST PROCEDURE

Equipment

- DC Power Supply
- Two Banana Cables
- Computer with USB port
- USB Flash Drive
- USB Cable (Type A to Type B)

Procedure

1. Set the power supply to 3.3 V. Connect the power supply from **VCC** to **GND** using the banana cables. The supply current should be less than 1 μ A.
2. Connect the USB drive to the **Common I/O** USB port.

3. Select the desired output port (**HSD1** or **HSD2**) by moving the jumpers to the appropriate logic level for **S** and **OE**, as shown in the function table in Table 1.
4. Connect the USB cable from the desired output port (**HSD1** or **HSD2**) to the computer's USB port. You will now be able to access the USB drive through the computer.

Table 1. FUNCTION TABLE

\overline{OE}	S	HSD1+, HSD1-	HSD2+, HSD2-
1	X	OFF	OFF
0	0	ON	OFF
0	1	OFF	ON

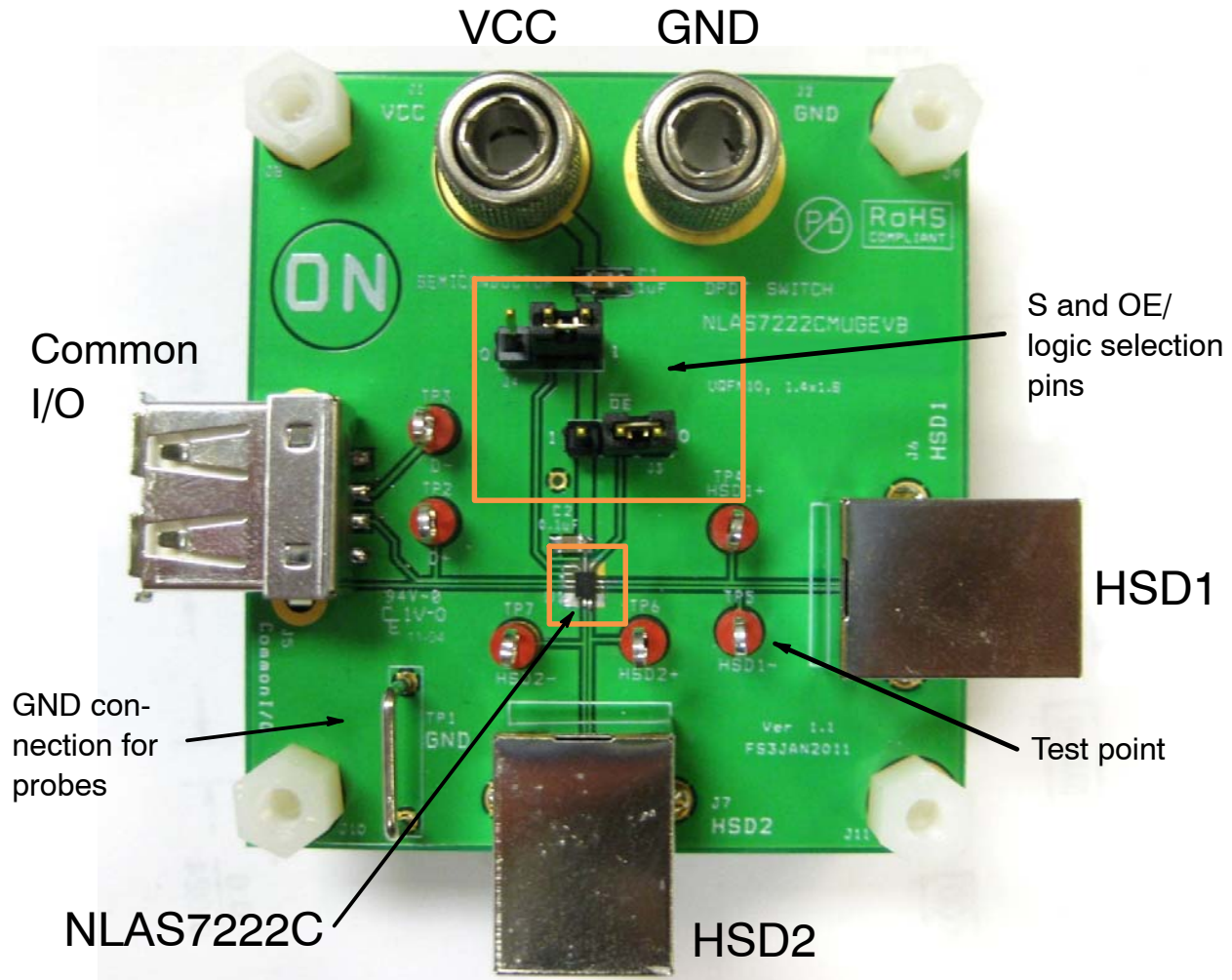


Figure 3. Evaluation Board Close-Up

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SCHEMATIC

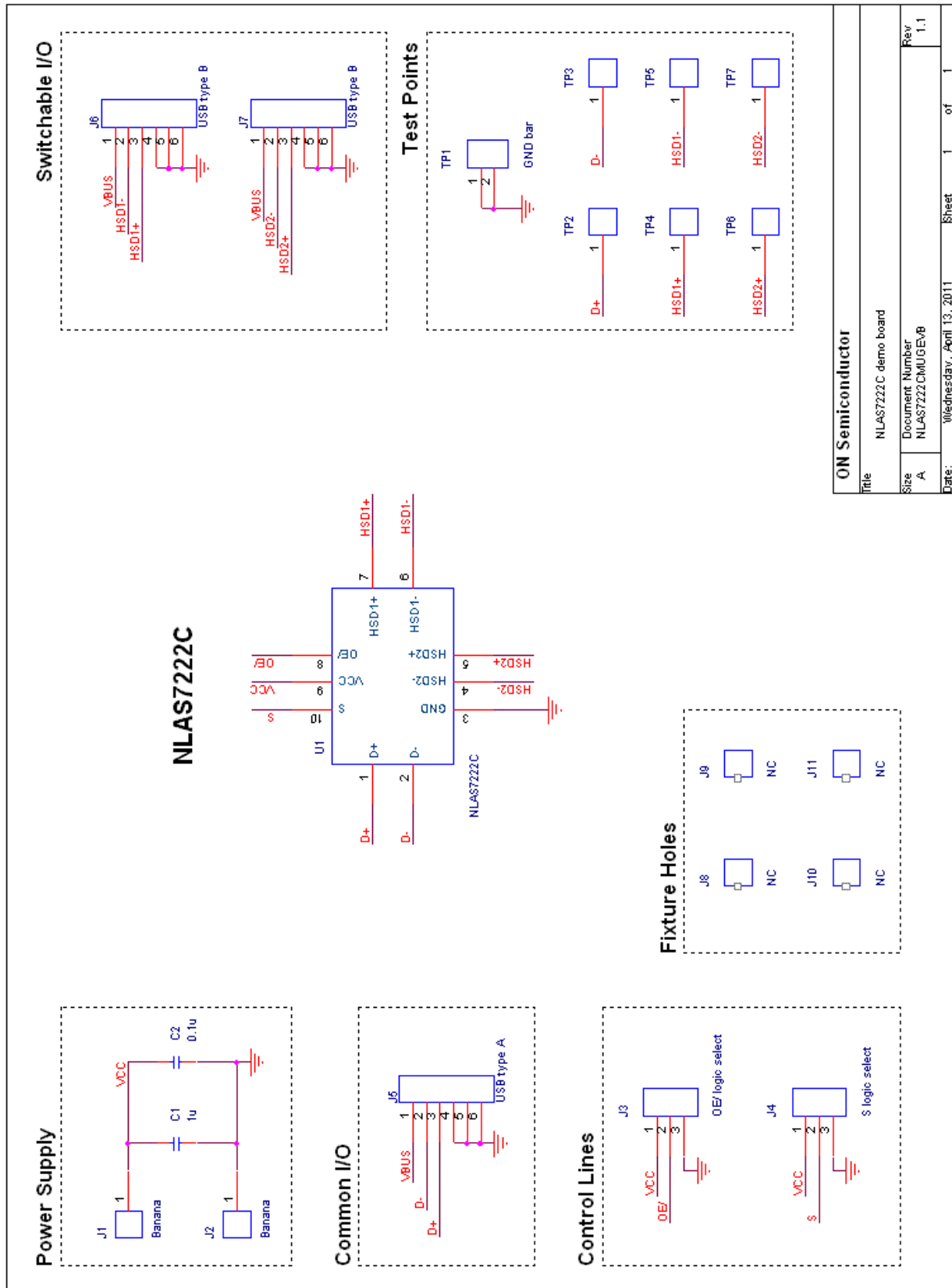


Figure 4. Evaluation Board Schematic

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Table 2. BILL OF MATERIALS

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
C1	1	Ceramic Capacitor SMD	1 μ F	10%	0805	AVX	GRM155R60J105
C2	1	Ceramic Capacitor SMD	0.1 μ F	10%	0402	Yageo	CC0402ZRY5V7BB104
J1, J2	2	Banana Connector	n/a	n/a	7 mm Hole	Johnson Components	111-2223-001
J3, J4	2	3-Pin Header	n/a	n/a	Header3	Tyco Electronics	5-826629-0
J3, J4	2	2-Pin Jumper	n/a	n/a	n/a	Tyco Electronics	4-881545-2
J5	1	USB TypeA Connector	n/a	n/a	USB TypeA	Mill-Max	896-43-004-00-000000
J6, J7	2	USB TypeB Connector	n/a	n/a	USB TypeB	Adam Tech	USB-B-S-RA
J8, J9, J10, J11	4	Standoff Nut	n/a	n/a	n/a	Keystone Electronics	1903C
J8, J9, J10, J11	4	Standoff Screw	n/a	n/a	n/a	Keystone Electronics	4814K-ND
TP1	1	PCB Shorting Link	n/a	n/a	n/a	Harwin	D3082-46
TP2, TP3, TP4, TP5, TP6, TP7	6	Test Point PC Multi Purpose	n/a	n/a	1.6mm hole	Keystone Electronics	5010
U1	1	NLAS7222C	n/a	n/a	UQFN10	ON Semiconductor	NLAS7222CMUTBG

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PCB LAYOUT

The PCB and components are made of lead-free and RoHS compliant materials. The layout is shown in Figure 5 below. The top layer traces are shown in magenta, and the

bottom layer traces are shown in cyan. Ground pours are present on the top and bottom layers for connectivity. PCB dimensions are 53 mm x 58 mm x 1 mm.

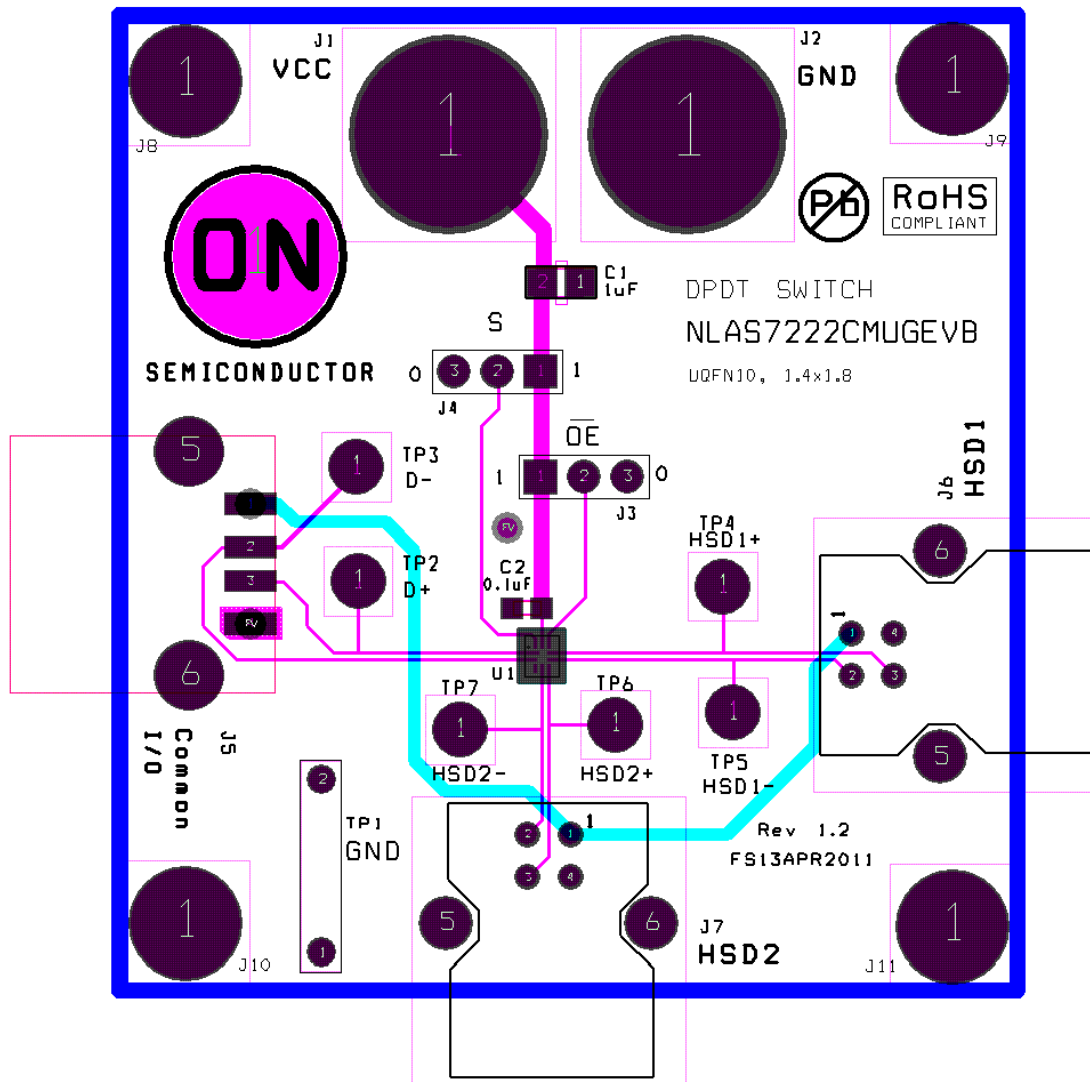



Figure 5. Evaluation Board Layout

PCB LAYOUT GUIDELINES

Implementing a high speed USB switch device requires paying attention on data lines and traces to preserve signal integrity. The demonstration board serves as layout example and can support the design engineers to preserve high speed performances.

Electrical layout guidelines are:

- ♦ The bypass capacitor must be placed as close as possible to the VCC input pin for noise immunity.
- ♦ The characteristics impedance of each switch segment must be 45 Ω .
- ♦ The ground plane of the PCB will be used to determine the characteristics impedance of each line.
- ♦ All corresponding D+/D- line segment pairs must be the same length.
- ♦ The use of vias to route these signals should be avoided when possible.
- ♦ The use of turns or bends to route these signal should be avoided when possible.

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