

# KAF-40000

## 7304 (H) x 5478 (V) Full Frame CCD Image Sensor

### Description

The KAF-40000 Image Sensor is a high performance, 40-megapixel CCD. Based on the TRUESENSE 6.0 micron Full Frame CCD Platform, the sensor features ultra-high resolution, broad dynamic range, and a four-output architecture. A lateral overflow drain suppresses image blooming, while an integrated Pulse Flush Gate clears residual charge on the sensor with a single electrical pulse. A Fast Dump Gate can be used to selectively remove a line of charge to facilitate partial image readout. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

The sensor shares a common pin-out and electrical configuration with the KAF-50100 Image Sensor, allowing a single camera design to support both members of this sensor family.

**Table 1. GENERAL SPECIFICATIONS**

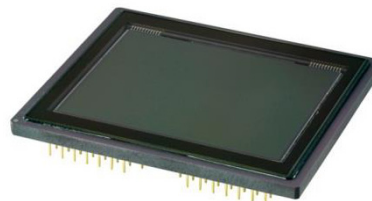
| Parameter  | Typical Value  |
|--|--|
| Architecture   | Full Frame CCD (Square Pixels)   |
| Total Number of Pixels                               | 7410 (H) × 5566 (V) = 41.2 Mp  |
| Number of Effective Pixels                           | 7336 (H) × 5510 (V) = 40.4 Mp  |
| Number of Active Pixels                              | 7304 (H) × 5478 (V) = 40.0 Mp  |
| Pixel Size   | 6.0 $\mu\text{m}$ (H) × 6.0 $\mu\text{m}$ (V)                                  |
| Active Image Size                                    | 45.76 mm (H) × 35.34 mm (V)<br>54.78 mm (Diagonal),<br>645 1.3x Optical Format |
| Aspect Ratio   | 4:3  |
| Horizontal Outputs                                   | 4  |
| Saturation Signal                                    | 42 ke <sup>-</sup>   |
| Output Sensitivity                                   | 31 $\mu\text{V/e}^-$   |
| Quantum Efficiency (Peak R, G, B)                    | 42%, 44%, 38%  |
| Read Noise (f = 18 MHz)                              | 13 e <sup>-</sup>  |
| Dark Signal (T = 60°C)                               | 42 pA/cm <sup>2</sup>  |
| Dark Current Doubling Temperature                    | 5.5°C  |
| Dynamic Range (f = 18 MHz)                           | 70.2 dB  |
| Estimated Linear Dynamic Range (f = 18 MHz)          | 69.3 dB  |
| Charge Transfer Efficiency<br>Horizontal<br>Vertical | 0.999995<br>0.999999   |
| Blooming Protection<br>(4 ms Exposure Time)          | 1400X Saturation Exposure  |
| Maximum Data Rate                                    | 18 MHz   |
| Package  | Ceramic PGA  |
| Cover Glass  | MAR Coated, 2 Sides  |

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.



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**Figure 1. KAF-40000 CCD Image Sensor**

### Features

- TRUESENSE Transparent Gate Electrode for High Sensitivity
- Ultra-High Resolution
- Board Dynamic Range
- Low Noise Architecture
- Large Active Imaging Area

### Application

- Digitization
- Mapping/Aerial
- Photography

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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## ORDERING INFORMATION

Table 2. ORDERING INFORMATION

| Part Number          | Description   | Marking Code                  |
|----------------------|---|-------------------------------|
| KAF-40000-FXA-JD-AA  | Gen2 Color (Bayer RGB), Microlens, Enhanced, ESD, Ceramic PGA, Clear Cover Glass with AR Coating (Both Sides), Standard Grade     | KAF-40000-FX<br>Serial Number |
| KAF-40000-FXA-JD-AE  | Gen2 Color (Bayer RGB), Microlens, Enhanced, ESD, Ceramic PGA, Clear Cover Glass with AR Coating (Both Sides), Engineering Sample |                               |
| KAF-40000-CXA-JD-AA* | Gen1 Color (Bayer RGB), Microlens, Enhanced, ESD, Ceramic PGA, Clear Cover Glass with AR Coating (Both Sides), Standard Grade     | KAF-40000-CX<br>Serial Number |
| KAF-40000-CXA-JD-AE* | Gen1 Color (Bayer RGB), Microlens, Enhanced, ESD, Ceramic PGA, Clear Cover Glass with AR Coating (Both Sides), Engineering Sample |                               |

\*Not recommended for new designs.

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.onsemi.com](http://www.onsemi.com).

## DEVICE DESCRIPTION

### Architecture

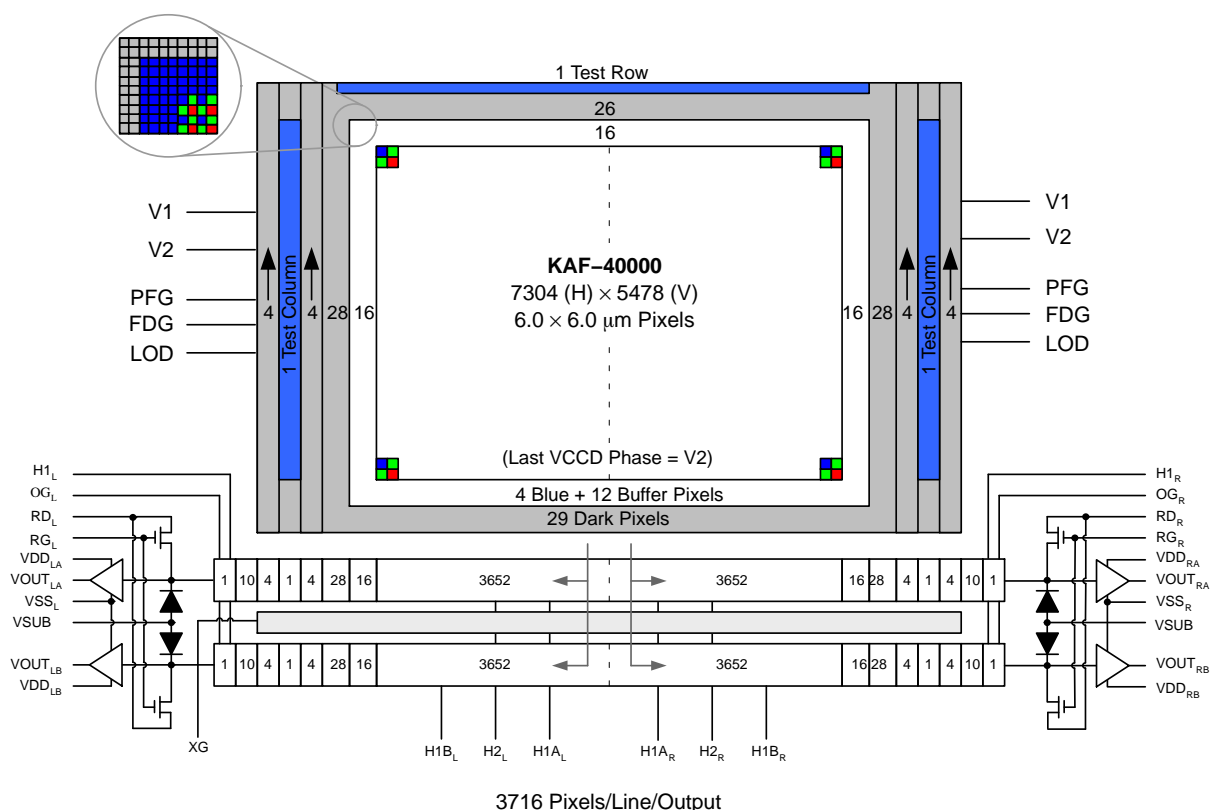


Figure 2. Block Diagram

#### Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Existing within this dark region are light shielded pixels that include 28 leading dark pixels on every line. There are also 29 full dark lines at the start and 26 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

#### Dummy Pixels

Within each horizontal shift register there are 20 leading pixels. These are designated as dummy pixels and should not be used to determine a dark reference level. These pixels are noted on the block diagram as the leading pixels in a horizontal line sequence: 1 + 10 + 4 + 1 (CTE monitor pixel) + 4.

#### Active Buffer Pixels

Forming the outer boundary of the effective active pixel region, there are 16 unshielded active buffer pixels between the photoactive area and the dark reference. These pixels are light sensitive but they are not tested for defects and

non-uniformities. For the leading 16 active column pixels, the first 4 pixels are covered with blue pigment while the remaining active buffer pixels are arranged in a Bayer pattern (R, GR, GB, B).

#### CTE Monitor Pixels

Two CTE test columns, at the leading end of each output, and one CTE test row are included for manufacturing test purposes.

#### Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs (charge) within the device. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain (LOD) to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

### Charge Transport

The integrated charge from each pixel in the Vertical CCD (VCCD) is transported to the output using a two-step process. Each remaining line (row) of charge is first transported from the VCCD to a dual parallel split horizontal register (HCCD) using the V1 and V2 register clocks. The transfer to the HCCD occurs on the falling edge of V2 while H1A is held high. This line of charge may be readout immediately (dual split) or may be passed through a transfer gate (XG) into a second (B) HCCD register while the next line loads into the first (A) HCCD register (dual parallel split). Readout of each line in the HCCD is always split at the middle and, thus, either two or four outputs are used. Left (or right) outputs carry image content from pixels in the left (or right) columns of the VCCD. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the output amplifier. On each falling edge of H1L, a new charge packet is sensed by the output amplifier. Left and right HCCDs are electrically isolated from each other except for the common transfer gate (XG).

### Pulsed Flush Gate/Fast Dump Gate

The Pulsed Flush Gate (PFG) feature is used to drain the charge of all pixels prior to exposure. The exception is pixels

in the Fast Dump Gate (FDG) row that are drained using the separate FDG pin. Draining is accomplished by first clocking V2 high while V1 is held low. This forces all charge into the V2 phase of the pixel. While V2 is high, PFG (or FDG) may be clocked high to begin draining the signal from the pixel to the LOD. Charge transfer out of the pixel is fully completed only after V2 has been clocked low plus some characteristic time.

### Horizontal Register

#### Output Structure

The output consists of a floating diffusion connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip current source must be added to the VOUT pin of the device. See Figure 4.

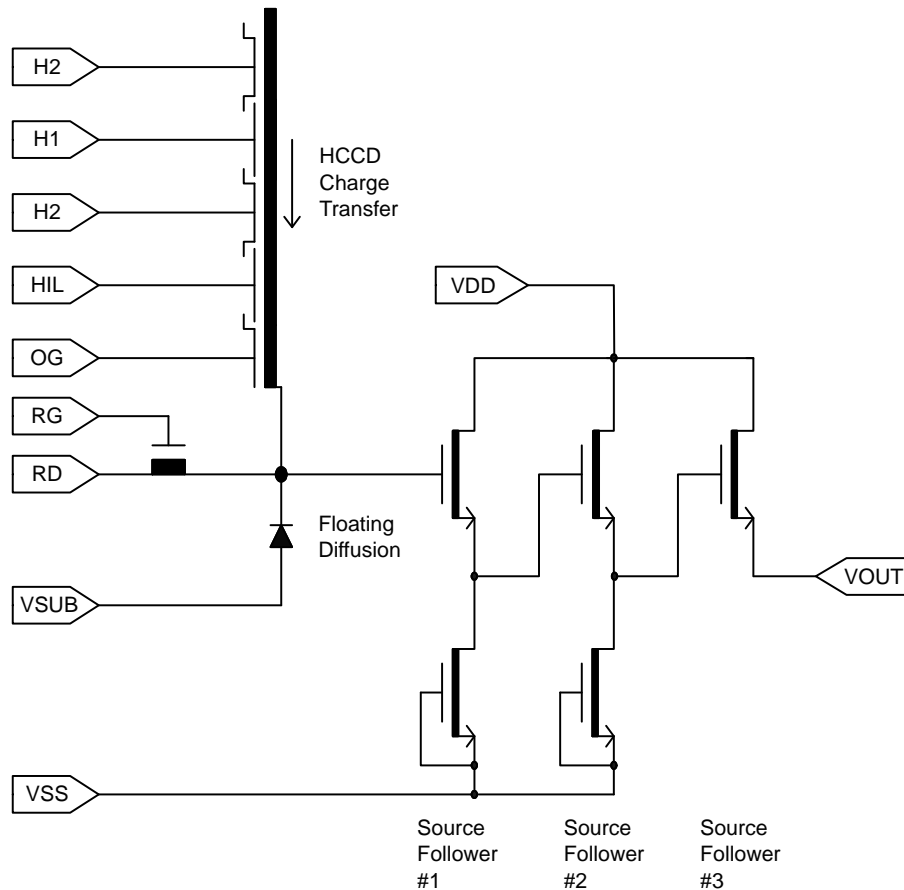
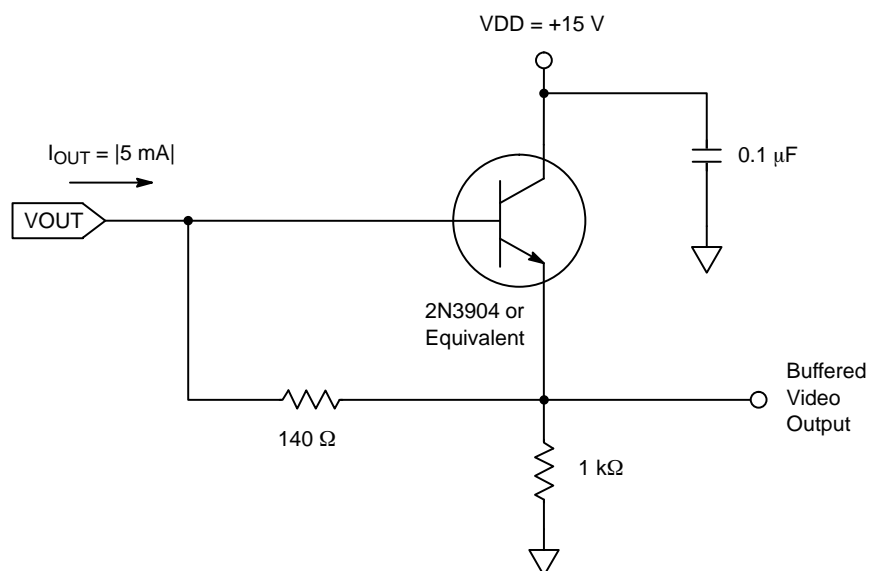


Figure 3. Output Architecture (Each Output)

*Output Load*

NOTE: Component values may be revised based on operating conditions and other design considerations.

**Figure 4. Recommended Output Structure Load Diagram**

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## Physical Description

### Pin Description and Device Orientation

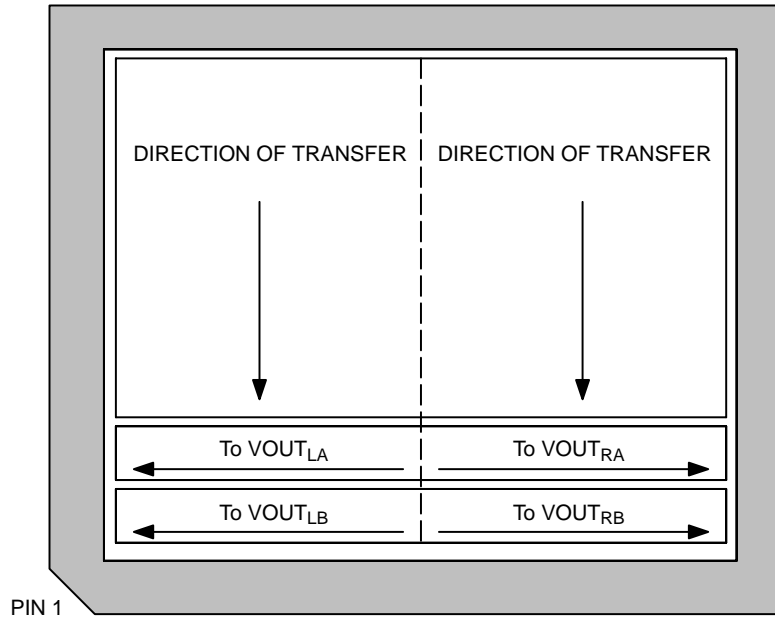
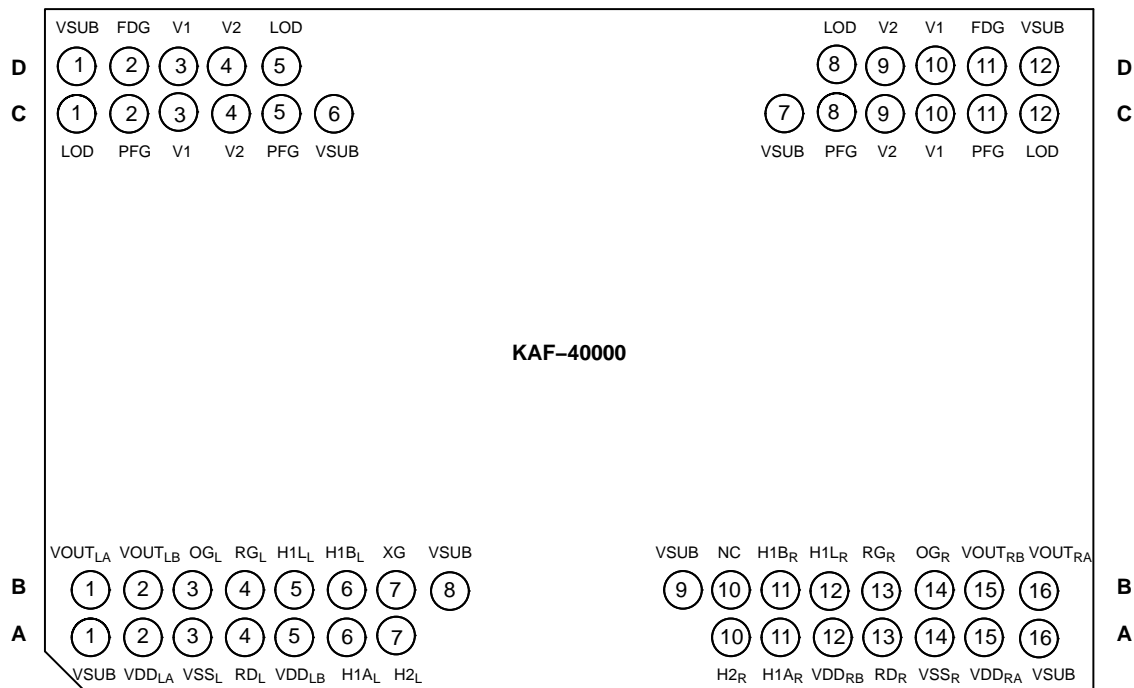


Figure 5. Image Transfer Diagram Viewed from the Top (Cover Glass Side)



#### Notes:

1. Pins with the same name are nominally tied together on the circuit board and have the same operating conditions. In addition, pins labeled with left ('L') and ('R') designations may also be tied together except for VOUT pins.
2. To achieve optimal output signal matching, electrical layout of the PCB should be made as symmetrical as possible relative to the left and right sides of the sensor.

Figure 6. Pinout Diagram

Table 3. PIN DESCRIPTION

| Pin | Name   | Description                      |
|-----|--------|----------------------------------|
| A1  | VSUB   | Substrate                        |
| A2  | VDDLA  | Output Amplifier Supply, Left A  |
| A3  | VSSL   | Output Amplifier Return, Left    |
| A4  | RDL    | Reset Drain, Left                |
| A5  | VDDL B | Output Amplifier Supply, Left B  |
| A6  | H1AL   | Horizontal Phase 1, A Left       |
| A7  | H2L    | Horizontal Phase 2, Left         |
| A10 | H2R    | Horizontal Phase 2, Right        |
| A11 | H1AR   | Horizontal Phase 1, A Right      |
| A12 | VDDRB  | Output Amplifier Supply, Right B |
| A13 | RDR    | Reset Drain, Right               |
| A14 | VSSR   | Output Amplifier Return, Right   |
| A15 | VDDRA  | Output Amplified Supply, Right A |
| A16 | VSUB   | Substrate                        |

|     |        |                                      |
|-----|--------|--------------------------------------|
| B1  | VOULTA | Video Output, Left A                 |
| B2  | VOULTB | Video Output, Left B                 |
| B3  | OGL    | Output Gate, Left                    |
| B4  | RGL    | Reset Gate, Left                     |
| B5  | H1LL   | Horizontal Phase 1, Last Gate, Left  |
| B6  | H1BL   | Horizontal Phase 1, B Left           |
| B7  | XG     | Horizontal Transfer Gate             |
| B8  | VSUB   | Substrate                            |
| B9  | VSUB   | Substrate                            |
| B10 | NC     | No Connection                        |
| B11 | H1BR   | Horizontal Phase 1, B Right          |
| B12 | H1LR   | Horizontal Phase 1, Last Gate, Right |
| B13 | RGR    | Reset Gate, Right                    |
| B14 | OGR    | Output Gate, Right                   |
| B15 | VOUTRB | Video Output, Right B                |
| B16 | VOUTRA | Video Output, Right A                |

| Pin | Name | Description            |
|-----|------|------------------------|
| C1  | LOD  | Lateral Overflow Drain |
| C2  | PFG  | Pulse Flush Gate       |
| C3  | V1   | Vertical Phase 1       |
| C4  | V2   | Vertical Phase 2       |
| C5  | PFG  | Pulse Flush Gate       |
| C6  | VSUB | Substrate              |
| C7  | VSUB | Substrate              |
| C8  | PFG  | Pulse Flush Gate       |
| C9  | V2   | Vertical Phase 2       |
| C10 | V1   | Vertical Phase 1       |
| C11 | PFG  | Pulse Flush Gate       |
| C12 | LOD  | Lateral Overflow Drain |

|     |      |                        |
|-----|------|------------------------|
| D1  | VSUB | Substrate              |
| D2  | FDG  | Fast Dump Gate         |
| D3  | V1   | Vertical Phase 1       |
| D4  | V2   | Vertical Phase 2       |
| D5  | LOD  | Lateral Overflow Drain |
| D8  | LOD  | Lateral Overflow Drain |
| D9  | V2   | Vertical Phase 2       |
| D10 | V1   | Vertical Phase 1       |
| D11 | FDG  | Fast Dump Gate         |
| D12 | VSUB | Substrate              |

NOTE: The leads are on a 0.100" spacing.

## IMAGING PERFORMANCE

Table 4. TYPICAL OPERATIONAL CONDITIONS

| Description  | Test Condition – Unless Otherwise Noted  | Units              | Notes   |
|--|--|--------------------|---|
| Readout Time ( $t_{\text{READOUT}}$ )                | 2093   | ms                 | Includes 140 Overclock Pixels<br>Includes 178 Overclock Lines                             |
| Integration Time ( $t_{\text{INT}}$ )                | Variable<br>33<br>200<br>250<br>1000   | ms                 | Low Light Tests<br>Saturation Tests<br>Brightfield Tests<br>Darkfield and Linearity Tests |
| Frame Time ( $t_{\text{READOUT}} + t_{\text{INT}}$ ) | Variable<br>2126 (2093 + 33)<br>2293 (2093 + 200)<br>2343 (2093 + 250)<br>3093 (2093 + 1000) | ms                 | Low Light Tests<br>Saturation Tests<br>Brightfield Tests<br>Darkfield and Linearity Tests |
| Line Time ( $t_{\text{LINE}}$ )                      | 364.3  | $\mu\text{s}$      | Includes 140 Overclock Pixels   |
| Horizontal Clock Frequency                           | 12 (as Tested)   | MHz                | Guaranteed for 18 MHz Operation   |
| Temperature – Room                                   | 20   | $^{\circ}\text{C}$ | Room Temperature  |
| Temperature – Device                                 | 29   | $^{\circ}\text{C}$ | Typical Device Operating Temperature at Test<br>Room Temperature                          |
| Operation  | Nominal Operating Levels   |                    | Dual Parallel Split Mode  |

Table 5. SPECIFICATIONS

| Description  | Symbol   | Min.     | Nom.             | Max. | Units                                | Verification Plan <sup>15</sup> |
|--|--|----------|------------------|------|--------------------------------------|---------------------------------|
| Saturation Signal (Note 1)                           | $N_{\text{SAT}}$<br>$N e^{-\text{SAT}}$<br>$Q/V$ | 1075     | 1300<br>42<br>31 |      | mV<br>$e^{-}$<br>$\mu\text{V}/e^{-}$ | Die                             |
| Photoresponse Non-Linearity (Note 2)                 | PRNL   |          | 5                | 10   | %                                    | Die                             |
| Photoresponse Non-Uniformity (Note 3)                | PRNU   |          | 8.5              | 25   | % p-p                                | Die                             |
| Readout Dark Signal (Note 4)                         | $V_{\text{DARK,READ}}$                           |          | 18               | 20   | mV/s                                 | Die                             |
| Integration Dark Signal (Note 5)                     | $V_{\text{DARK,INT}}$                            |          | 3                | 10   | mV/s                                 | Die                             |
| Dark Signal Non-Uniformity (Notes 6, 16)             | DSNU   |          | 1                | 4    | mV p-p                               | Die                             |
| Dark Signal Doubling Temperature (Note 4)            | $\Delta T$                                       |          | 5.5              |      | $^{\circ}\text{C}$                   | Design                          |
| Read Noise (Note 7)                                  | NR   |          | 13               |      | $e^{-}$ rms                          | Design                          |
| Dynamic Range (Note 8)                               | DR   |          | 70.2             |      | dB                                   | Design                          |
| Estimated Linear Dynamic Range                       | $DR_{\text{LIN}}$ (Est.)                         |          | 69.3             |      | dB                                   | Design                          |
| Red-Green Hue Shift<br>Blue-Green Hue Shift (Note 9) | $RG_{\text{HueUnif}}$<br>$BG_{\text{HueUnif}}$   |          | 5                | 12   | %                                    | Die                             |
| Horizontal Charge Transfer Efficiency (Note 10)      | HCTE   | 0.999995 |                  |      |                                      | Die                             |
| Vertical Charge Transfer Efficiency                  | VCTE   | 0.999999 | 0.999998         |      |                                      | Die                             |
| Blooming Protection (Note 11)                        | $X_{\text{AB}}$                                  | 800      | 1400             |      | $\times E_{\text{SAT}}$              | Design                          |
| DC Offset, Output Amplifier (Note 12)                | $V_{\text{ODC}}$                                 | 6.0      | 7.5              | 9.5  | V                                    | Die                             |
| Output Amplifier Bandwidth (Note 13)                 | $f_{-3\text{dB}}$                                |          | 220              |      | MHz                                  | Design                          |
| Output Impedance, Amplifier                          | $R_{\text{OUT}}$                                 | 100      | 145              | 300  | $\Omega$                             | Die                             |
| Reset Feedthrough                                    | $V_{\text{RFT}}$                                 |          | 0.5              |      | V                                    | Design                          |



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**Table 5. SPECIFICATIONS** (continued)

| Description | Symbol | Min. | Nom. | Max. | Units | Verification Plan <sup>15</sup> |
|-------------|--------|------|------|------|-------|---------------------------------|
|-------------|--------|------|------|------|-------|---------------------------------|

## KAF-40000-FXA CONFIGURATION GEN2 COLOR

|                                    |                   |   |     |   |      |        |
|------------------------------------|-------------------|---|-----|---|------|--------|
| Peak Quantum Efficiency            | QE <sub>MAX</sub> |   |     |   |      |        |
| Red                                |                   | – | 39  | – | % QE | Design |
| Green                              |                   | – | 45  | – |      |        |
| Blue                               |                   | – | 37  | – |      |        |
| Peak Quantum Efficiency Wavelength | λ <sub>QE</sub>   |   |     |   |      |        |
| Red                                |                   | – | 600 | – | nm   | Design |
| Green                              |                   | – | 530 | – |      |        |
| Blue                               |                   | – | 470 | – |      |        |

## KAF-40000-CXA CONFIGURATION GEN1 COLOR (Note 17)

|                                    |                   |   |     |   |      |        |
|------------------------------------|-------------------|---|-----|---|------|--------|
| Peak Quantum Efficiency            | QE <sub>MAX</sub> |   |     |   |      |        |
| Red                                |                   | – | 37  | – | % QE | Design |
| Green                              |                   | – | 41  | – |      |        |
| Blue                               |                   | – | 37  | – |      |        |
| Peak Quantum Efficiency Wavelength | λ <sub>QE</sub>   |   |     |   |      |        |
| Red                                |                   | – | 600 | – | nm   | Design |
| Green                              |                   | – | 520 | – |      |        |
| Blue                               |                   | – | 470 | – |      |        |

- Increasing output load currents to improve bandwidth will decrease these values.
- Worst-case deviation (from 15 mV & 90% N<sub>SAT</sub> min) relative to a linear fit applied between 0 and 65% of V<sub>SAT</sub>.
- Difference between the maximum and minimum average signal levels of 168 × 168 blocks within the sensor on a per color basis as a % of average signal level.
- T = 60°C. t<sub>INT</sub> = 0. Average non-illuminated signal with respect to over-clocked horizontal register signal.
- T = 60°C. Average non-illuminated signal with respect to over-clocked vertical register signal.
- T = 60°C. Absolute difference between the maximum and minimum average signal levels of 168 × 168 blocks within the sensor.
- rms deviation of horizontal over-clocked pixels measured in the dark.
- 20Log (Ne<sup>–</sup><sub>SAT</sub> / NR)
- Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest (168 × 168 blocks) within the sensor. The specification refers to the largest value of the response difference.
- Measured per transfer above and below (~70% V<sub>SAT</sub> min) saturation exposure levels. Typically, no degradation in HCCD CTE is observed up to 18 MHz.
- X<sub>AB</sub> is the number of times above the V<sub>SAT</sub> illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X<sub>AB</sub> is measured at 4 ms.
- Video level offset with respect to ground.
- Last stage only. Assumes 5 pF off-chip load.
- Amplitude of feed-through in VOUT during RG clocking.
- A “die” parameter is measured on every sensor during production testing. A “design” parameter is quantified during design verification and not guaranteed by specification.
- t<sub>INT</sub> = 1000 ms.
- This color filter set configuration (Gen1) is not recommended for new designs.

# KAF-40000

## TYPICAL PERFORMANCE CURVES

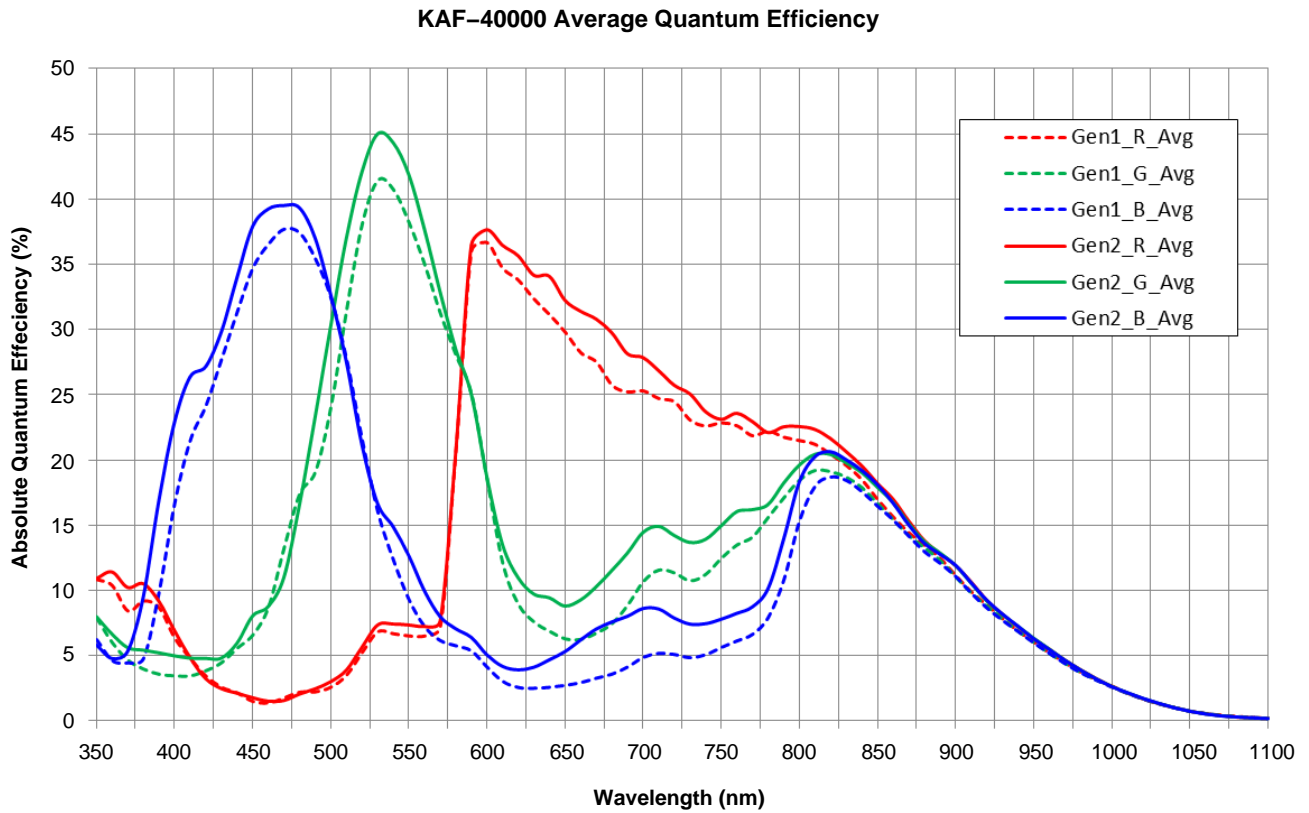


Figure 7. Spectral Response

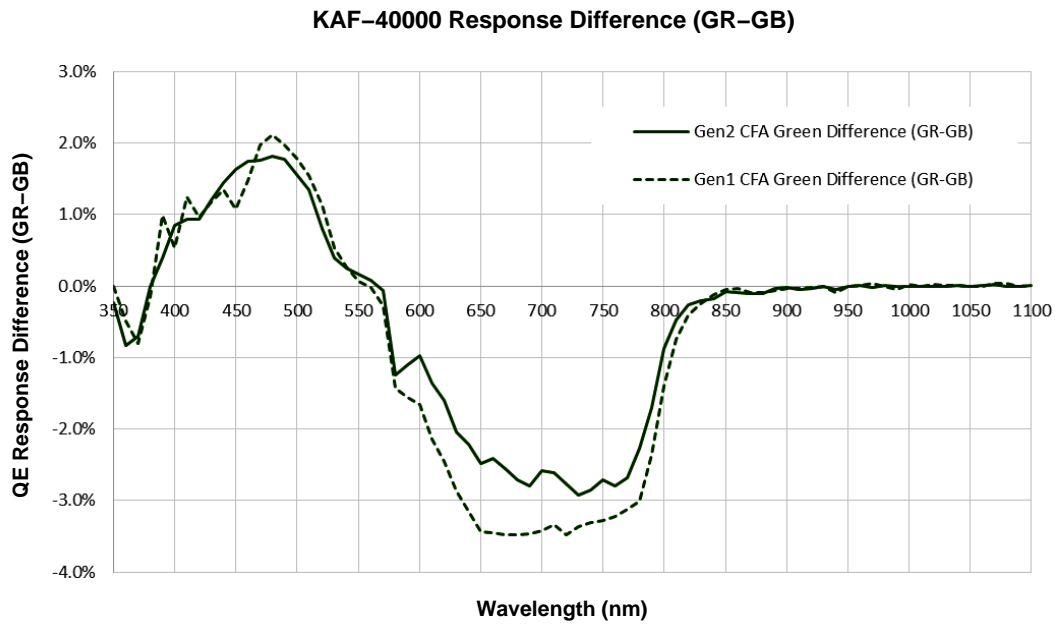


Figure 8. Typical GR-GB QE Difference

## KAF-40000

### KAF-40000 Anti-Blooming Performance

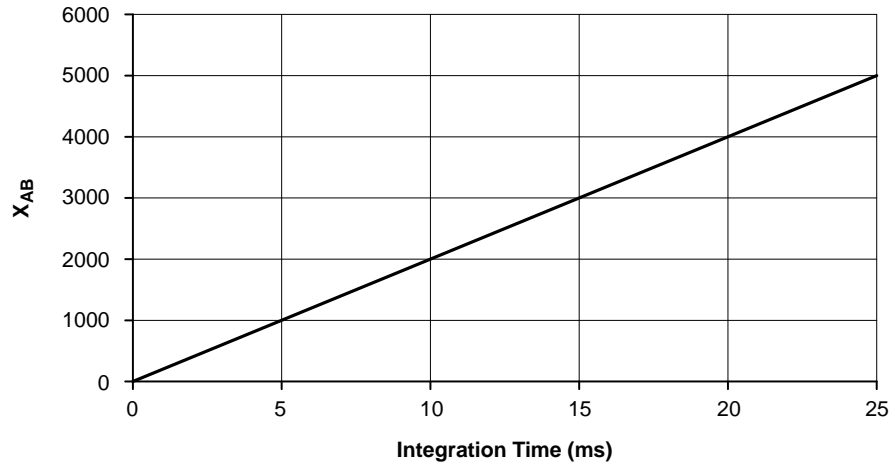


Figure 9. Minimum Expected Anti-Blooming Performance

## DEFECT DEFINITIONS

### Operating Conditions

Bright defect tests performed at  $T = 25^{\circ}\text{C}$ ,  $t_{\text{INT}} = 250 \text{ ms}$  and  $t_{\text{READOUT}} = 2093 \text{ ms}$ .

Dark defect tests performed at  $T = 25^{\circ}\text{C}$ ,  $t_{\text{INT}} = 1,000 \text{ ms}$  and  $t_{\text{READOUT}} = 2093 \text{ ms}$ .

**Table 6. SPECIFICATIONS**

| Classification | Points  | Clusters | Single Columns | Includes Dead Columns |
|----------------|---------|----------|----------------|-----------------------|
| Standard Grade | < 4,000 | < 50     | < 20           | Yes                   |

#### *Point Defects*

A pixel that deviates by more than 36 mV above neighboring pixels under non-illuminated conditions.

A pixel that deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions

#### *Cluster Defect*

A grouping of not more than 10 adjacent point defects.

Cluster defects are separated by no less than 4 good pixels in any direction.

#### *Column Defect*

A grouping of more than 10 point defects along a single column.

A column that deviates by more than 1.2 mV above neighboring columns under non-illuminated conditions.

A column that deviates by more than 1.5% above or below neighboring columns under illuminated conditions.

Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

#### *Dead Column*

A column that deviates by more than 50% below neighboring columns under illuminated conditions.

#### *Saturated Column*

A column that deviates by more than 120 mV above neighboring columns under non-illuminated conditions. No saturated columns are allowed.

## OPERATION

**Table 7. ABSOLUTE MAXIMUM RATINGS**

| Description                            | Symbol             | Minimum | Maximum | Units |
|--|--------------------|---------|---------|-------|
| Diode Pin Voltages (Notes 1, 2)        | $V_{\text{DIODE}}$ | -0.5    | 20      | V     |
| Gate Pin Voltages (Notes 1, 3)         | $V_{\text{GATE1}}$ | -14.3   | 14.5    | V     |
| RG Pin Voltage (Note 1)                | $V_{\text{RG}}$    | -0.5    | 14.5    | V     |
| Overlapping Gate Voltages (Note 4)     | $V_{1-2}$          | -14.3   | 14.5    | V     |
| Non-Overlapping Gate Voltages (Note 5) | $V_{q-q}$          | -14.3   | 14.5    | V     |
| Output Bias Current (Note 6)           | $I_{\text{OUT}}$   |         | -30     | mA    |
| LOD Diode Voltage (Note 1)             | $V_{\text{LODT}}$  | -0.5    | 13.5    | V     |
| Operating Temperature (Note 7)         | $T_{\text{OP}}$    | 0       | 60      | °C    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin VSUB.
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1A, H1B, H1L, H2, OG, PFG, FDG, XG.
4. Voltage difference between overlapping gates. Includes: V1 to V2, H1/H1L to H2, H1L to OG, V1 to H2, PFG to V1/V2, FDG to V1/V2, XG to H1A/H1B/H2.
5. Voltage difference between non-overlapping gates. Includes: V1 to H1A/H1B/H1L, V2 to XG, H2 to PFG/FDG, PFG to FDG.
6. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF (Mean Time to Failure).
7. Noise performance will degrade at higher temperatures.

### Power-up Sequence

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (VSUB).
2. Supply the appropriate biases and clocks to the remaining pins.

**Table 8. DC BIAS OPERATING CONDITIONS**

| Description                      | Symbol           | Minimum | Nominal | Maximum | Units | Maximum DC Current (mA)          |
|----------------------------------|------------------|---------|---------|---------|-------|----------------------------------|
| Reset Drain (Note 1)             | $V_{\text{RD}}$  | 11.3    | 11.5    | 11.7    | V     | $I_{\text{RD}} = 0.01$           |
| Output Amplifier Return (Note 1) | $V_{\text{SS}}$  | 0.5     | 0.7     | 1.0     | V     | $I_{\text{SS}} = 3.0$            |
| Output Amplifier Supply (Note 1) | $V_{\text{DD}}$  | 14.5    | 15.0    | 15.5    | V     | $I_{\text{OUT}} + I_{\text{SS}}$ |
| Substrate                        | $V_{\text{SUB}}$ |         | 0       |         | V     | 0.01                             |
| Output Gate (Note 1)             | $V_{\text{OG}}$  | -2.2    | -2.0    | -1.8    | V     | 0.01                             |
| Lateral Drain (Note 1)           | $V_{\text{LOD}}$ | 9.8     | 10.0    | 10.2    | V     | 0.01                             |
| Video Output Current (Note 2)    | $I_{\text{OUT}}$ |         | 5       | 10      | mA    |                                  |

1. Subscripts (L, R, LA, LB, RA, RB, T, B) have not been included in the symbol list.
2. An output load sink must be applied to VOUT to activate output amplifier – see Figure 4.

## AC Operating Conditions

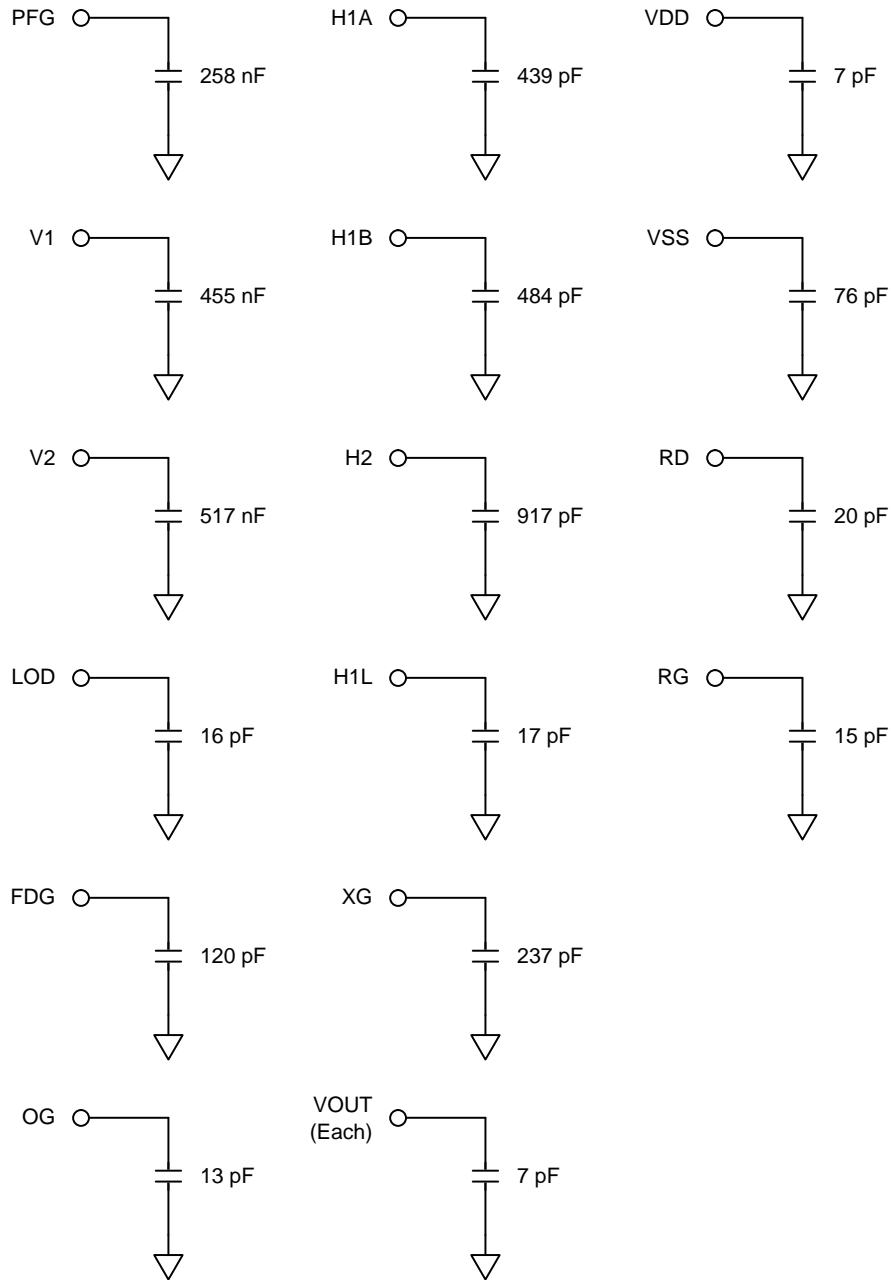
Table 9. CLOCK LEVELS

| Description | Symbol              | Level | Minimum | Nominal | Maximum | Units |
|-------------|---------------------|-------|---------|---------|---------|-------|
| V1          | V1L                 | Low   | -9.2    | -9.0    | -8.8    | V     |
|             | V1H                 | High  | 2.3     | 2.5     | 2.7     | V     |
| V2          | V2L                 | Low   | -9.2    | -9.0    | -8.8    | V     |
|             | V2H                 | High  | 3.3     | 3.5     | 3.7     | V     |
| H1A         | H1L                 | Low   | -4.2    | -4.0    | -3.8    | V     |
|             | H1H                 | High  | 1.8     | 2.0     | 2.2     | V     |
| H1B         | H1L                 | Low   | -4.2    | -4.0    | -3.8    | V     |
|             | H1H                 | High  | 1.8     | 2.0     | 2.2     | V     |
| H1L         | H1L <sub>LOW</sub>  | Low   | -6.2    | -6.0    | -5.8    | V     |
|             | H1L <sub>HIGH</sub> | High  | 1.8     | 2.0     | 2.2     | V     |
| H2          | H2L                 | Low   | -4.2    | -4.0    | -3.8    | V     |
|             | H2H                 | High  | 1.8     | 2.0     | 2.2     | V     |
| RG          | VRGL                | Low   | 0.8     | 1.0     | 1.2     | V     |
|             | VRGH                | High  | 7.8     | 8.0     | 8.2     | V     |
| PFG         | PFGL                | Low   | -9.2    | -9.0    | -8.8    | V     |
|             | PFGH                | High  | 4.8     | 5.0     | 5.2     | V     |
| FDG         | FDGL                | Low   | -9.2    | -9.0    | -8.8    | V     |
|             | FDGH                | High  | 4.8     | 5.0     | 5.2     | V     |
| XG          | XGL                 | Low   | -4.7    | -4.5    | -4.3    | V     |
|             | XGH                 | High  | 2.8     | 3.0     | 3.2     | V     |

1. Subscripts (L, R) have not been included in this symbol column.
2. All pins draw less than 10  $\mu$ A DC current. Capacitance values relative to SUB (substrate).
3. Capacitance values of left/right combined.

## KAF-40000

### Capacitance Model



**Figure 10. Lumped Capacitance Value Model – KAF-40000**

NOTE: A simplified pin capacitance model is provided by ON Semiconductor as a guideline for circuit design and tends to overstate the effective capacitance experienced by the clock driver. This model should be used as a reference. Although it is a moderately accurate target, it does not represent the values required for any automated circuit analysis.

## TIMING

Table 10. REQUIREMENTS AND CHARACTERISTICS

| Description                              | Symbol                                    | Minimum        | Nominal | Maximum | Units   |
|--|---|----------------|---------|---------|---------|
| H1, H2 Clock Frequency (Note 1, 2)       | $f_H$                                     |                |         | 18      | MHz     |
| V1, V2 Clock Frequency (Note 1, 2)       | $f_V$                                     |                |         | 25      | kHz     |
| V1–V2 Cross-over                         | $V_{VCR}$                                 | 0              | 1.0     | 2.7     | V       |
| H1–H2 Cross-over                         | $V_{HCR}$                                 | –2.0           | –1.0    | 0       | V       |
| H1, H2 Setup Time                        | $t_{HS}$                                  | 5              |         |         | $\mu s$ |
| V2–H1A Delay                             | $t_{D1}$                                  | 5              |         |         | $\mu s$ |
| H1A–XG Delay                             | $t_{D2}$                                  | 30             |         |         | $\mu s$ |
| XG–V2 Delay                              | $t_{D3}$                                  | 5              |         |         | $\mu s$ |
| H1, H2 Rise, Fall Times (Note 5, 6)      | $t_{H1r}, t_{H1f}$                        | 5              |         | 10      | %       |
| H1L Rise – H2 Fall Crossover (Note 9)    | $V_{H1LCR}$                               | –2.0           | –1.0    | 1.0     | V       |
| V1, V2 Rise, Fall Times (Note 5)         | $t_{V1r}, t_{V1f}$                        | 5              |         | 10      | %       |
| RG Clock Pulse Width (Note 7)            | $t_{RGw}$                                 | 5              |         |         | ns      |
| RG Rise, Fall Times (Note 5)             | $t_{RGr}, t_{RGf}$                        | 5              |         | 10      | %       |
| V1, V2 Clock Pulse Width (Notes 2, 3, 4) | $t_{Vw}$                                  | 16             | 20      |         | $\mu s$ |
| Pixel Period (1 Count) (Note 2)          | $t_e$                                     | 55.56          |         |         | ns      |
| H1L–VOUT Delay                           | $t_{HV}$                                  |                | 10      |         | ns      |
| RG–VOUT Delay                            | $t_{RV}$                                  |                | 5       |         | ns      |
| Readout Time (Note 8)                    | $t_{READOUT} - DS$<br>$t_{READOUT} - DPS$ | 1.35<br>0.76   |         |         | s       |
| Frame Rate (Note 8)                      | $t_F - DS$<br>$t_F - DPS$                 | 0.7<br>1.3     |         |         | fps     |
| Line Rate (Note 8)                       | $t_{LINEDS} - DS$<br>$t_{LINEDP} - DPS$   | 242.2<br>274.4 |         |         | $\mu s$ |
| PFG Holdoff Time                         | $t_{PFG}$                                 | 180            |         |         | $\mu s$ |
| FDG Holdoff Time                         | $t_{FDG}$                                 | 20             |         |         | $\mu s$ |

1. 50% duty cycle values.
2. CTE will degrade above the maximum frequency.
3. Longer times will degrade noise performance.
4. Measured where  $V_{CLOCK}$  is at 0 V.
5. Relative to the pulse width (based on 50% of high/low levels).
6. The maximum specification or 10 ns whichever is greater based on the frequency of the horizontal clocks.
7. RG should be clocked continuously.
8. DS = Dual Split DPS = Dual Parallel Split.
9. The charge capacity near the output could be degraded if the voltage at the clock crossover point is outside this range.



Edge Alignment

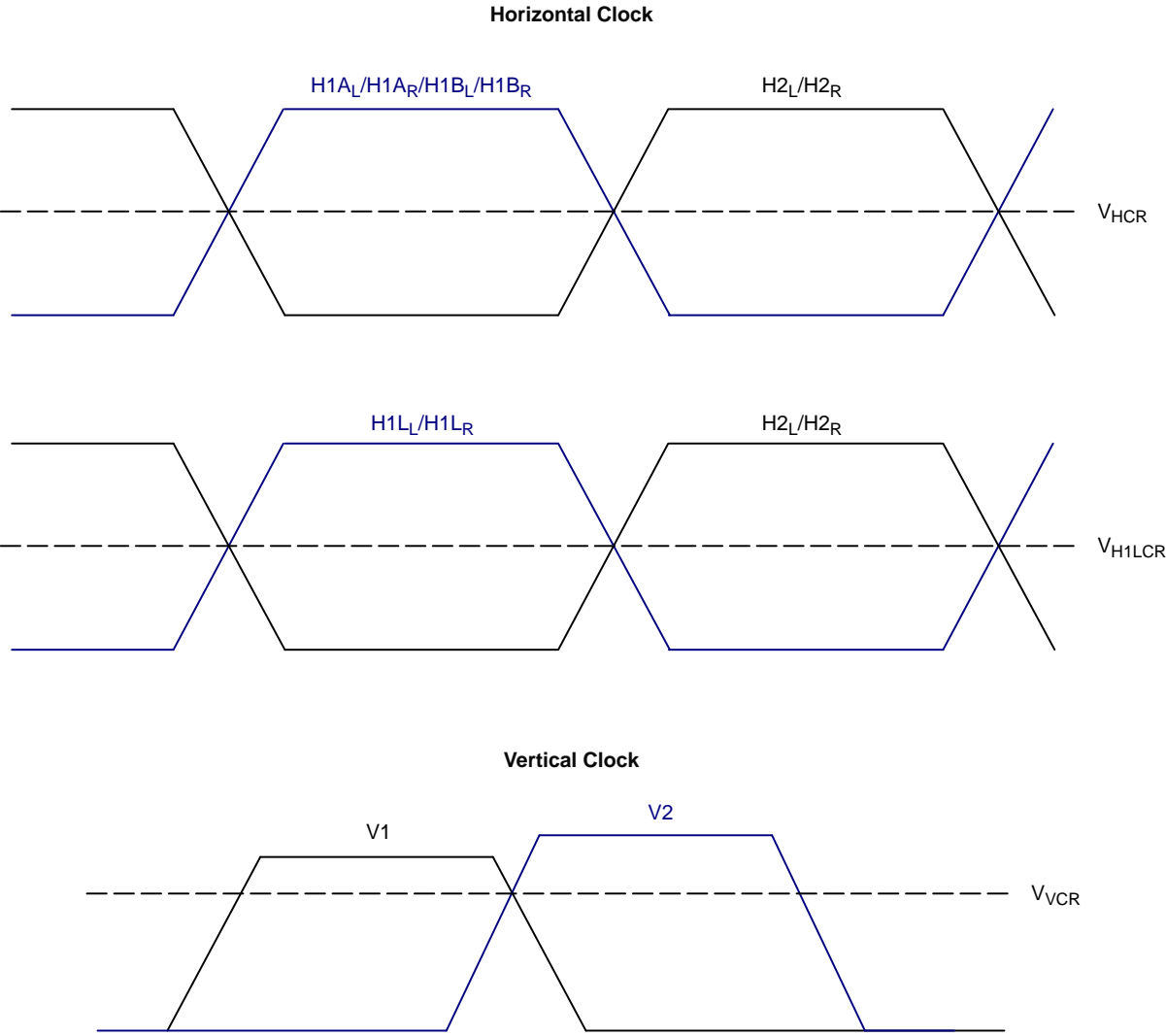


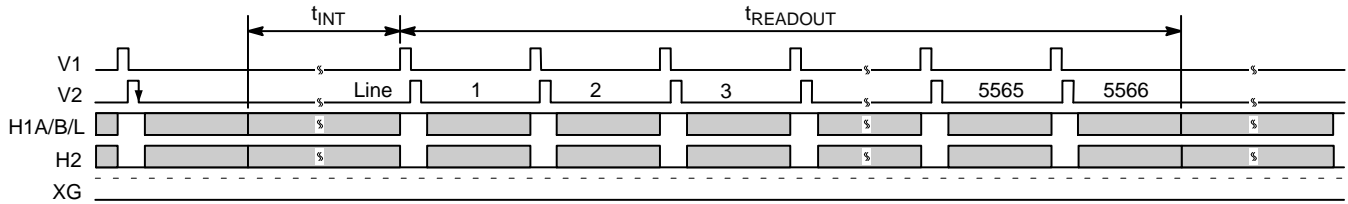
Figure 11. Timing Edge Alignment

## Frame Timing

Dual split timing reads the pixels out of VOUTLA and VOUTRA. H1B may be grounded in this operating mode.

Dual-Parallel Split timing reads pixels out of all four outputs with even lines reading out of VOUTLA and VOUTRA and odd lines reading out of VOUTLB and VOUTRB.

Frame Timing – Dual Split



Frame Timing – Dual-Parallel Split

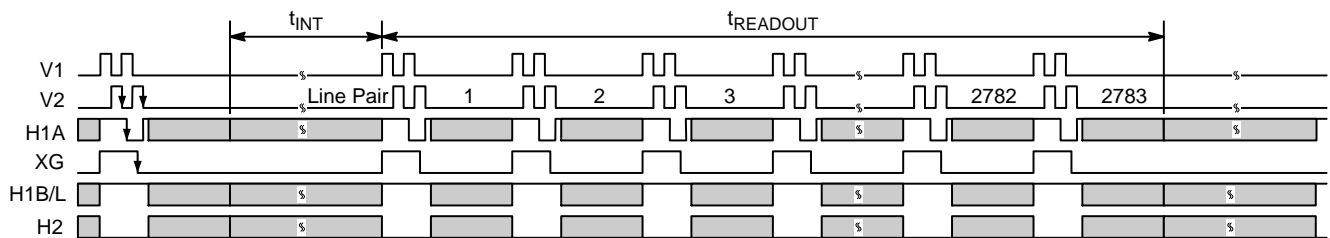


Figure 12. Frame Timing

## Frame Timing Detail

Vertical Clocks

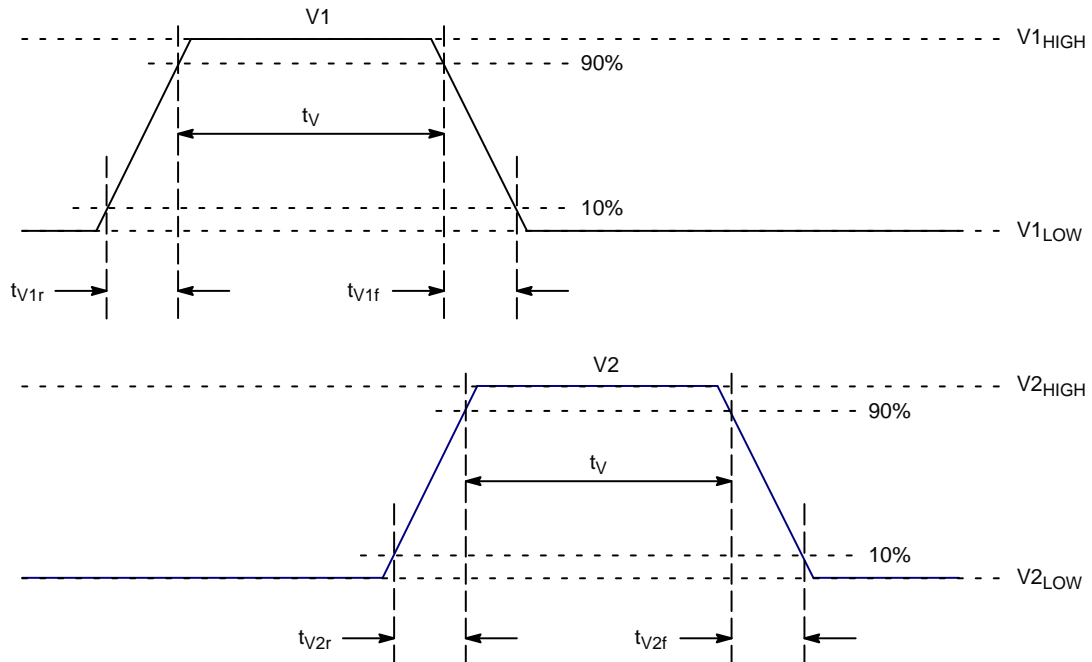


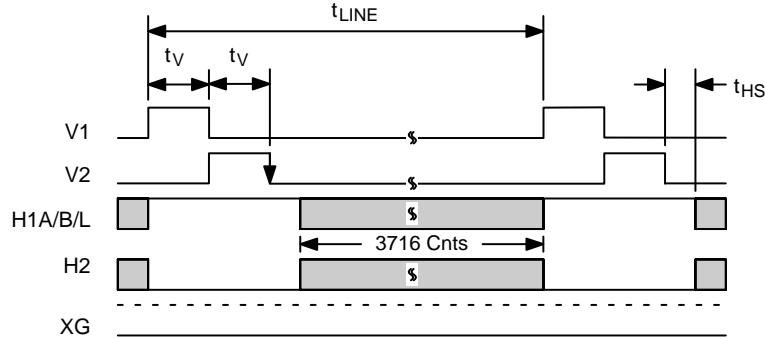
Figure 13. Frame Timing Detail

### Line Timing (Each Output)

XG is held low unless the Dual-Parallel Split timing is required. While operating in Dual-Parallel Split mode, full resolution rows are passed from V2 ( $t_{D1}$ ), through

H1A ( $t_{D2}$ ), and then passed through XG ( $t_{D3}$ ) and into H1B. During this time, a second, full resolution, row will load into H1A at the second falling edge of V2 following the characteristic delay  $t_{HD}$ .

Line Timing – Dual Split



Line Timing – Dual-Parallel Split

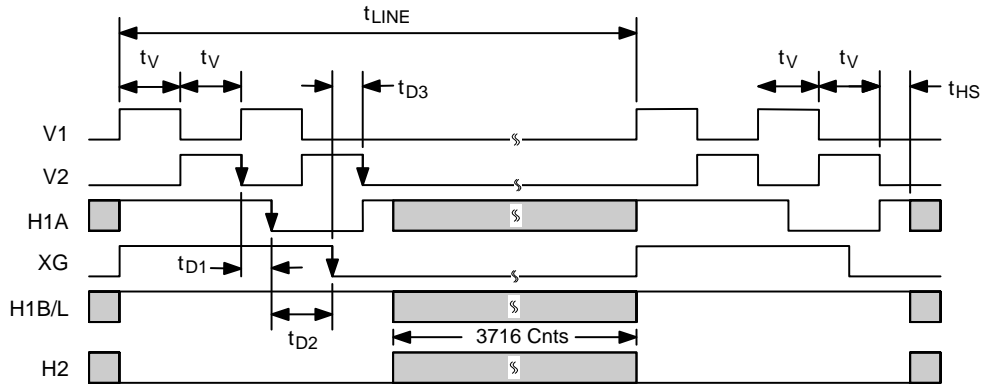


Figure 14. Line Timing

## Pixel Timing

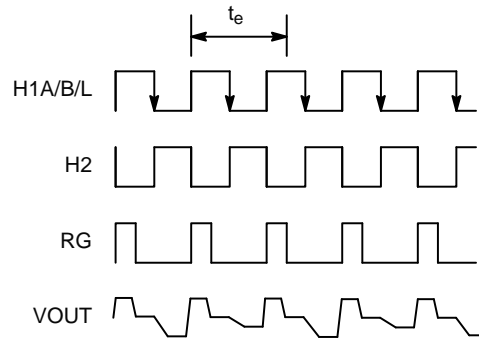


Figure 15. Pixel Timing

## Pixel Timing Detail

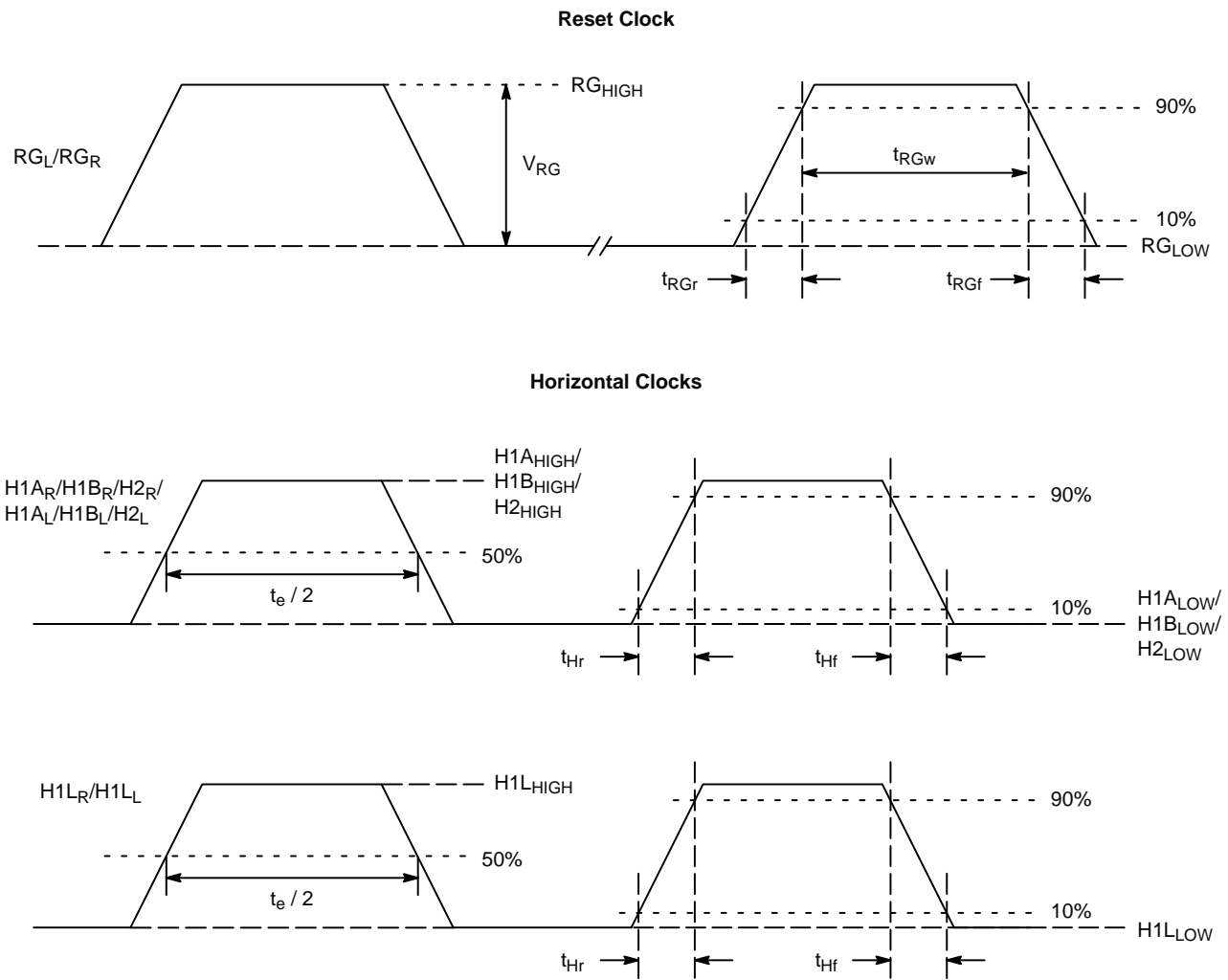


Figure 16. Pixel Timing Detail

MODE OF OPERATION

Pulse Flush Gate Timing

The PFG clock resets all pixels in the array (except the FDG row). Charge transfer out of the pixel is fully completed only after V2 has been clocked low as shown.

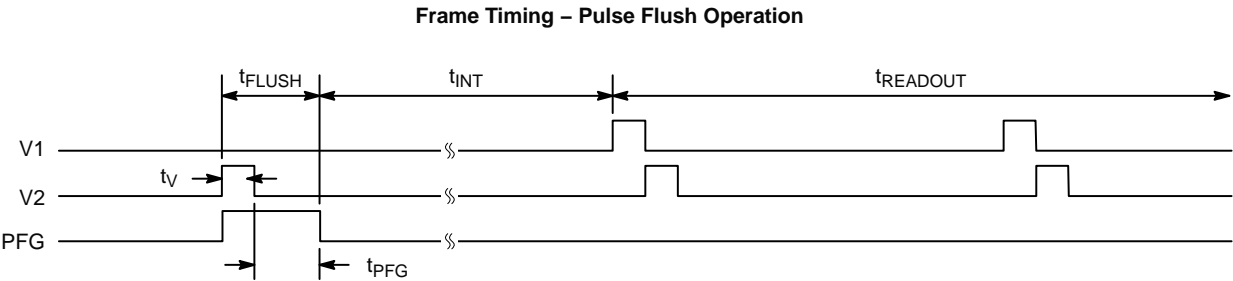


Figure 17. Pulse Flush Gate Timing

Fast Dump Gate (FDG) Timing

The FDG clock only resets pixels that happen to be in the FDG row. Charge transfer out of the pixel is fully completed only after V2 has been clocked low plus the characteristic

time period ( $t_{\text{FDG}}$ ). The position of the FDG row is illustrated in Figures 19–21, including the timing required for a simple 1 line dump operation.

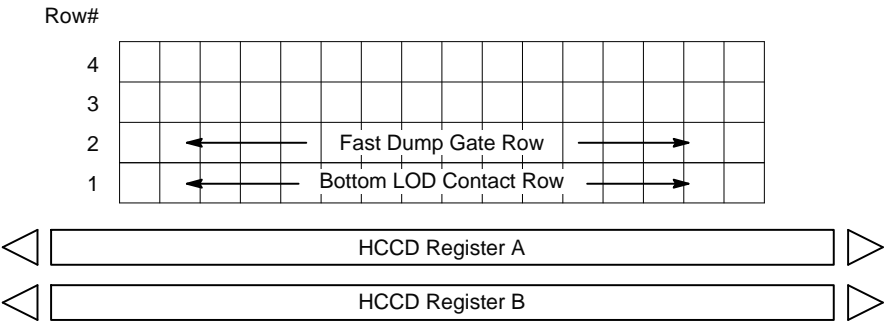


Figure 18. Fast Line Dump Layout

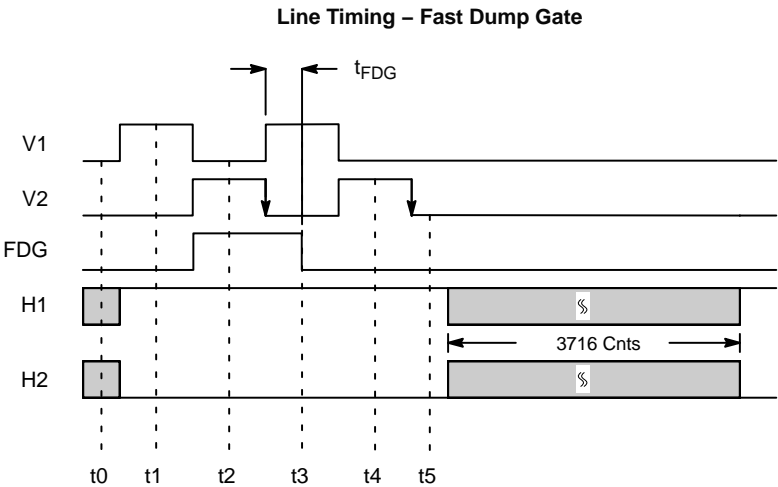


Figure 19. One Line Dump Timing Example

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## Line Timing – Fast Dump Gate (3 Line Dump)

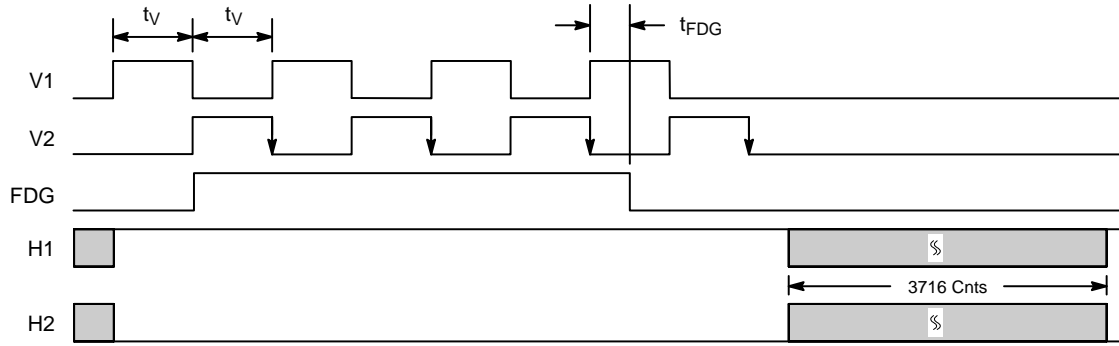
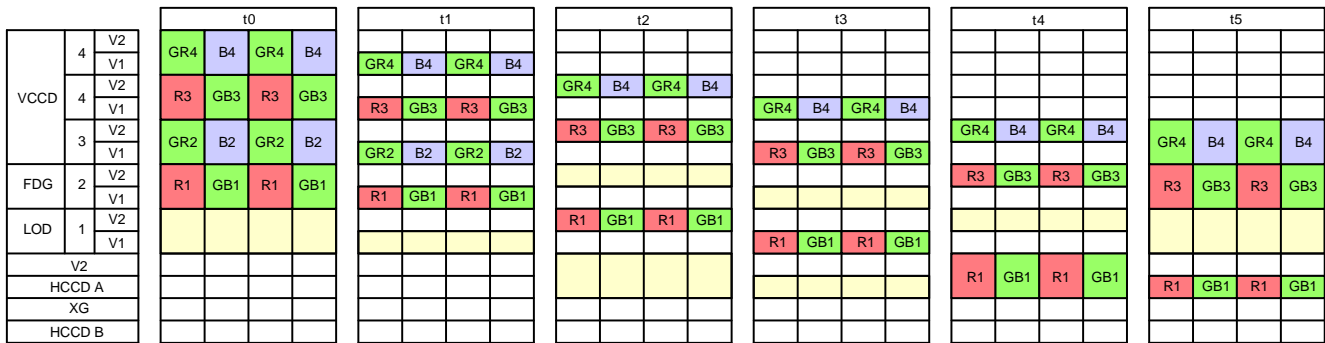


Figure 20. Line Dump Timing Example



NOTE: Areas highlighted in yellow represent pixels drained of charge.

Figure 21. One Line Dump Pixel Illustration Using Color Filter Designation

## STORAGE AND HANDLING

Table 11. STORAGE CONDITIONS

| Description                  | Symbol   | Minimum | Maximum | Units |
|------------------------------|----------|---------|---------|-------|
| Storage Temperature (Note 1) | $T_{ST}$ | -20     | 70      | °C    |

1. Long-term storage toward the maximum temperature will accelerate color filter degradation.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from [www.onsemi.com](http://www.onsemi.com).

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from [www.onsemi.com](http://www.onsemi.com).

For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from [www.onsemi.com](http://www.onsemi.com).

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from [www.onsemi.com](http://www.onsemi.com).

For information on Standard terms and Conditions of Sale, please download [Terms and Conditions](http://www.onsemi.com) from [www.onsemi.com](http://www.onsemi.com).

## MECHANICAL DRAWINGS

## Completed Assembly

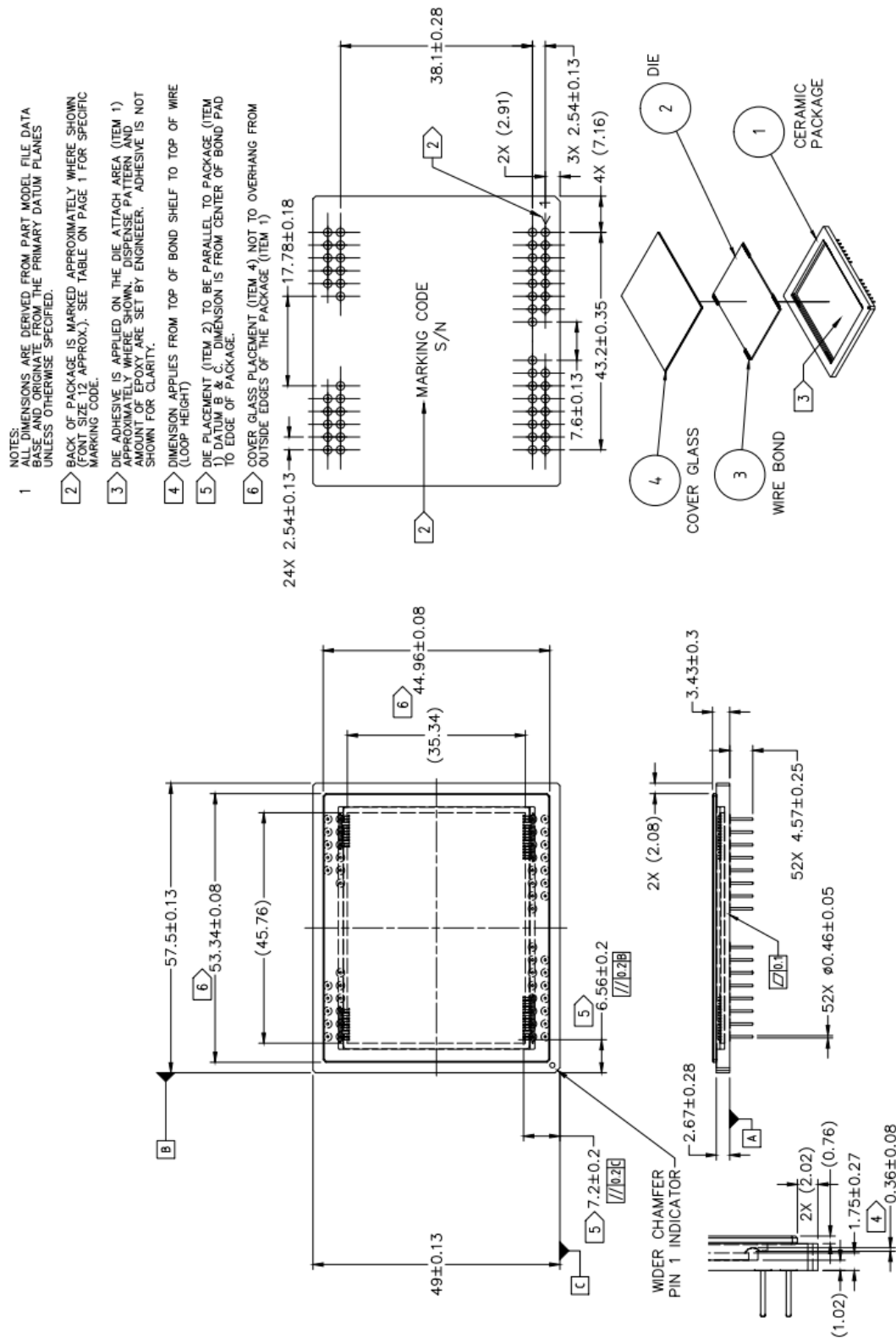


Figure 22. Completed Assembly Drawing



## Alignment Marks

The 98 + 48 mark should be used if alignment to die surface is required.

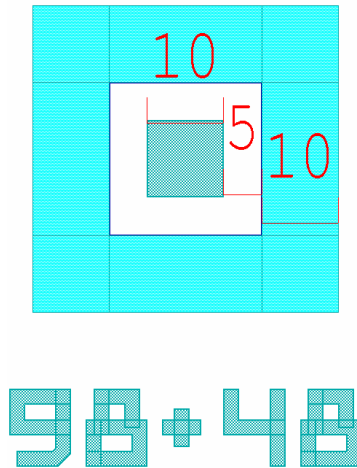
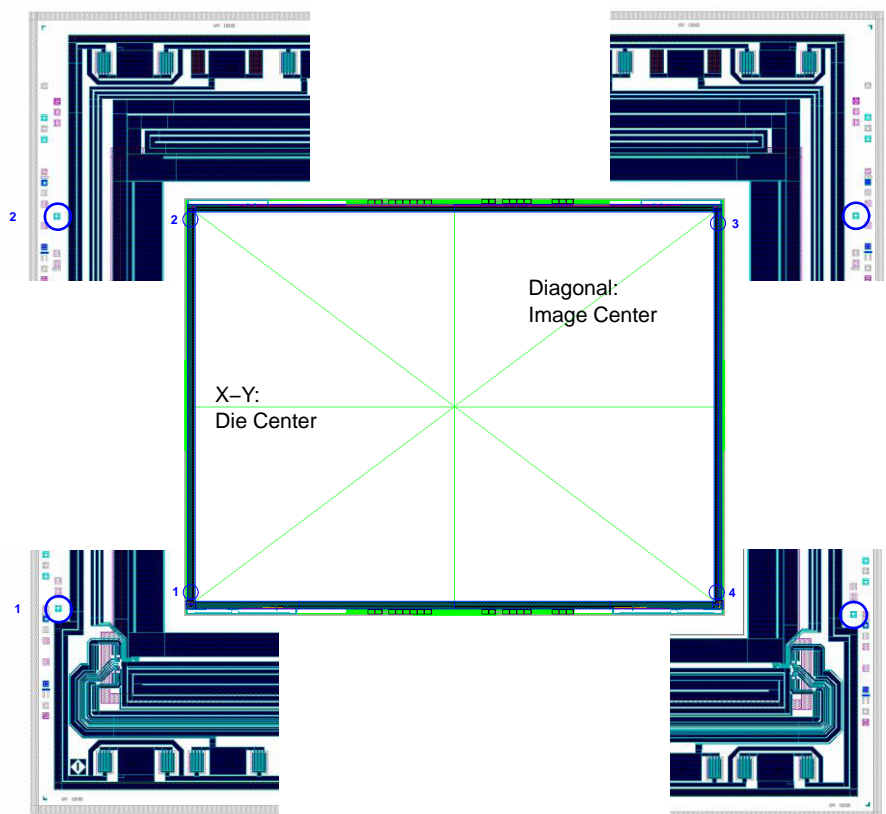


Figure 23. Individual Alignment Mark “98 + 48” (1 of 4)



NOTE: Image center is  $-0.55 \mu\text{m}$  (X) and  $34.05 \mu\text{m}$  (Y) from Die center.

Figure 24. Location of Recommended Alignment Marks (4 Locations)

## KAF-40000

Locations of marked alignment marks are listed in the table below with respect to the die center. Locations are listed in  $\mu\text{m}$  from the die center.

**Table 12.**

| Alignment Mark | X Location | Y Location |
|----------------|------------|------------|
| 1              | -22700     | -16340     |
| 2              | -22700     | 16340      |
| 3              | 22700      | 16340      |
| 4              | 22700      | -16340     |

Locations of marked alignment marks are listed in the table below with respect to the image center. Locations are listed in  $\mu\text{m}$  from the image center.

**Table 13.**


| Alignment Mark | X Location | Y Location |
|----------------|------------|------------|
| 1              | -22699.45  | -16374.05  |
| 2              | -22699.45  | 16305.95   |
| 3              | 22700.55   | 16305.95   |
| 4              | 22700.55   | -16374.05  |

### Cover Glass Specification

1. Substrate material Schott D263T eco or equivalent.
2. 10  $\mu\text{m}$  max. scratch/dig specification on the glass. No defect in the glass that exceeds 10  $\mu\text{m}$  in any X-Y dimension.
3. Multilayer anti-reflective coating.

**Table 14.**

| Wavelength | Total Reflectance |
|------------|-------------------|
| 420-450    | $\leq 2\%$        |
| 450-630    | $\leq 1\%$        |
| 630-680    | $\leq 2\%$        |

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