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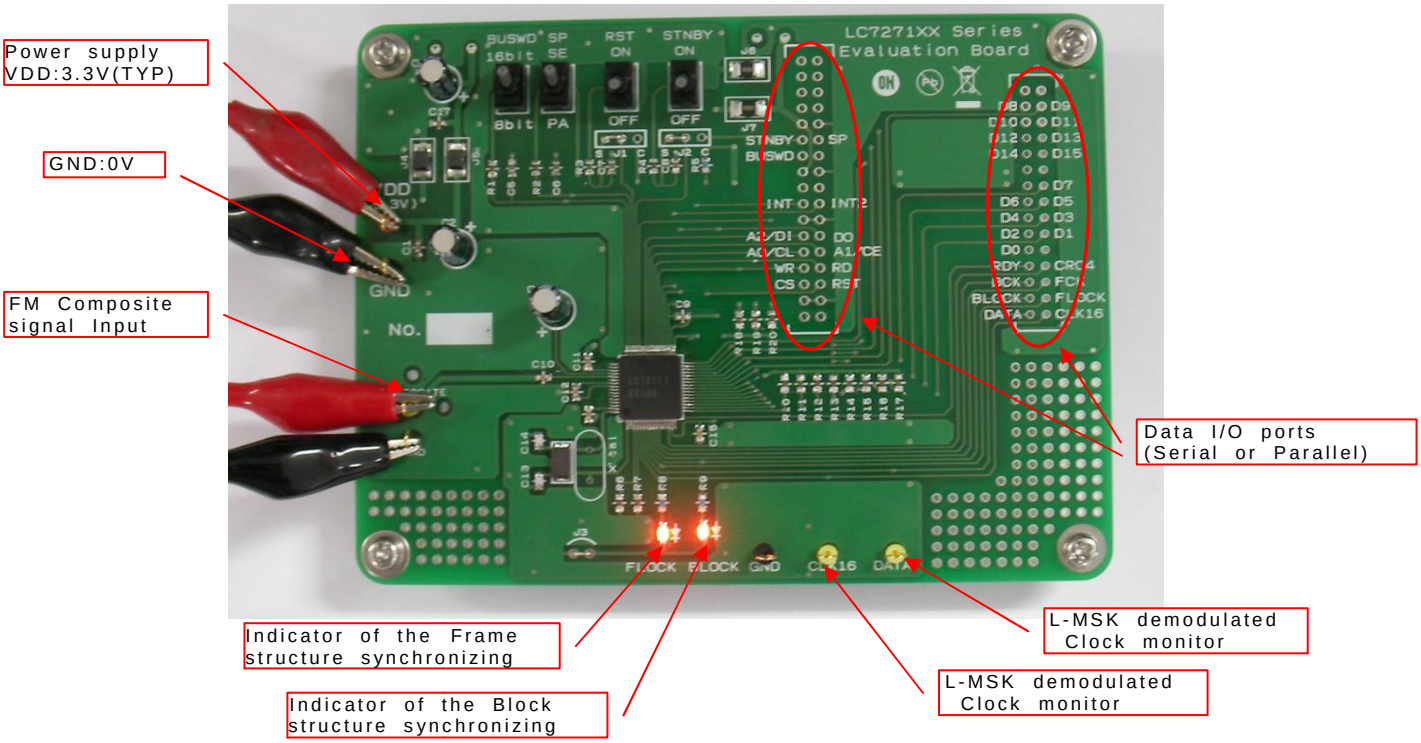
Test Procedure for the LC72717PWGEVB Evaluation Board

Evaluation board (120mm ×90mm)



Overview

This is evaluation board to evaluate LC72717PWGEVB.

FM composite signal is input into a composite terminal on board. Input level follows specifications of each LSI. When the DARC signal is included in FM composite signal, LED on an evaluation board lights up.
This indicates that LSI has received the DARC signal normally.
If CLK16 and DATA are connected to a DARC encoder, measurement of a bit error rate is possible.

Take in error correction data

Error correction data is available with personal computer by our serial data format CCB or parallel interface format. Operating procedure of CCB and general parallel format are mentioned in datasheet of each LSI. For connection with a controller, the test pin is prepared.
Pull-up resistor of DO must be adjusted to compound with clock transfer rate.

Toggle SW(SP) select a parallel interface and a serial interface.PA is a parallel interface.SE is a serial interface.

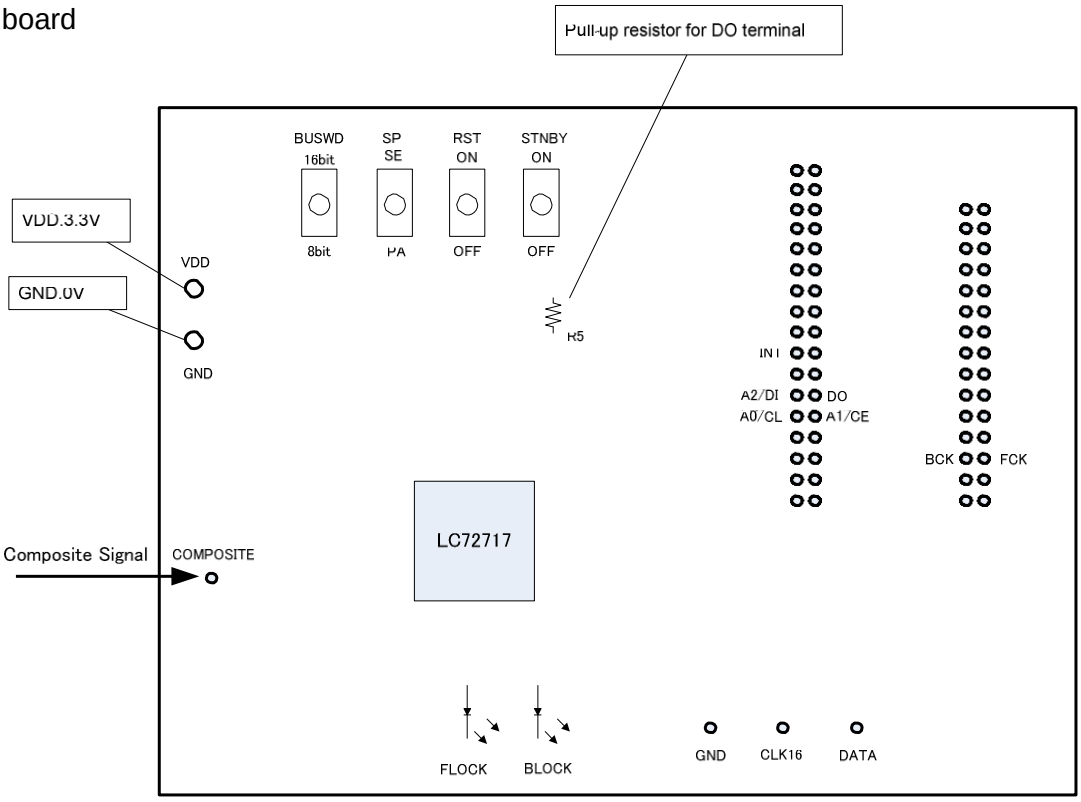
When a parallel interface is selected,toggle SW1(BUSWD) is valid.

About CCB format

CCB (Computer Control BUS) format is serial bus format of our original. Address of equipment is assigned to LSI corresponding to CCB in principle. Other than FM multiplex LSI, our manufacture corresponding to CCB format such as PLL or electronic volume can set it up on same bus.

On the real data input-output procedure that CCB format was used for, it is mentioned in each LSI specification document.

Illustration of LC72717PW evaluation board



How to use:

1. Connect the power supply to VDD and GND. (+2.7V to +3.6V,Typ 3.3V)
2. Input composite signals to the check pin(COMPOSITE).
3. Toggle Switch-RST is operated(OFF→ON→OFF) and LSI is initialized.
4. If the LC72717PW detects DARC signal in composite signal and the input level of a composite signal is adjusted properly, BLOCK and FLOCK output level turn "H". And the LED-FLOCK and LED-BLOCK light up.

Toggle switch is connected to Switch-RST and Switch- STNBY terminal. "ON" side on board notation is the active side. RST terminal is active low and STNBY terminal is active high.

LED is connected to FLOCK, BLOCK terminal. When each signal of BLOCK and FLOCK became "H" level, this LED turns on. That is when frame structure synchronization or block structure synchronization established it

(1) FLOCK:Frame synchronization flag output
BIC is in the head of a block. There are four singular points of BIC in one frame.
A frame synchronization is established when the singular point of BIC distinguishes to the right timing.

(2) BLOCK:Block synchronization flag output
A block synchronization is established when BIC that shows the head of each block is able to distinguish correctly.

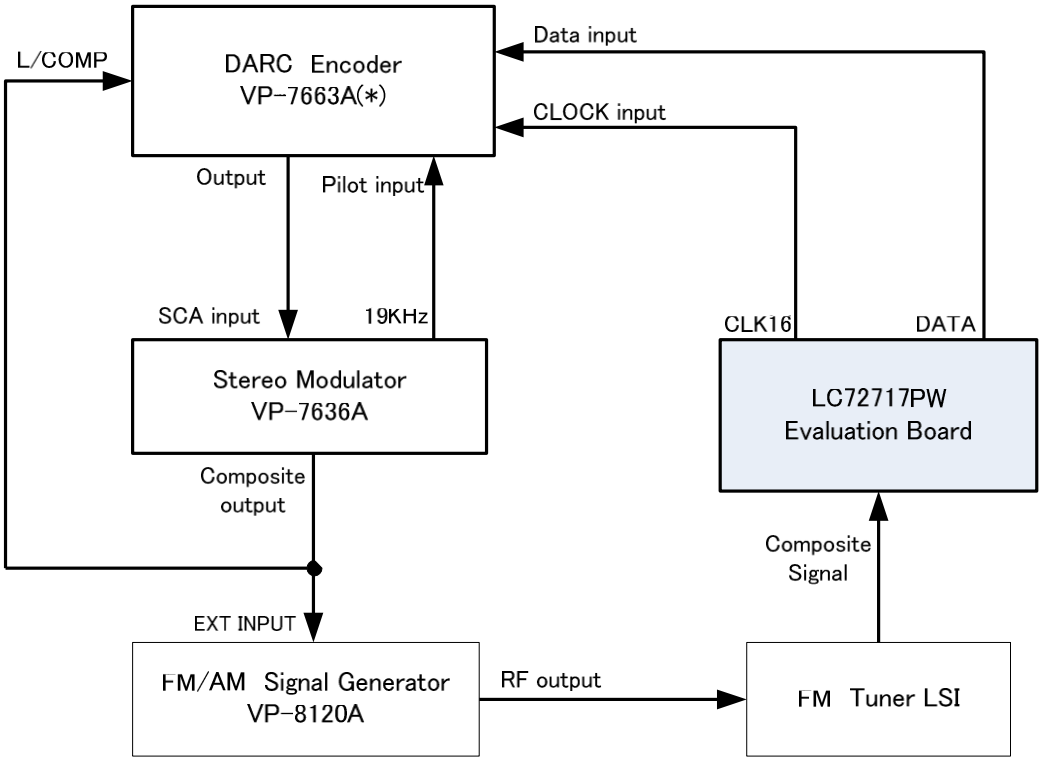
That two LEDs light up shows

the following.
DARC signal is included in the composite signal from FM tuner, and composite signal is inputted properly,and frame structure is distinguished correctly, and it is shown that the LC72717PW is operating normally.

[Note] : The initial value of LSI is frame structure of Method-B.
In order to set FLOCK to H level, DARC signal needs to be frame structure of Method-B.

In case controlling this board with micro computer or personal computer, four connections of CCB and INT signal connection are necessary at least. FLOCK, BLOCK, CLK16 and DATA terminal use it for a check for the operating situation of this LSI. Of course, for the positive use with control software, controller may be connected to.

Reference : Bit error rate measurement

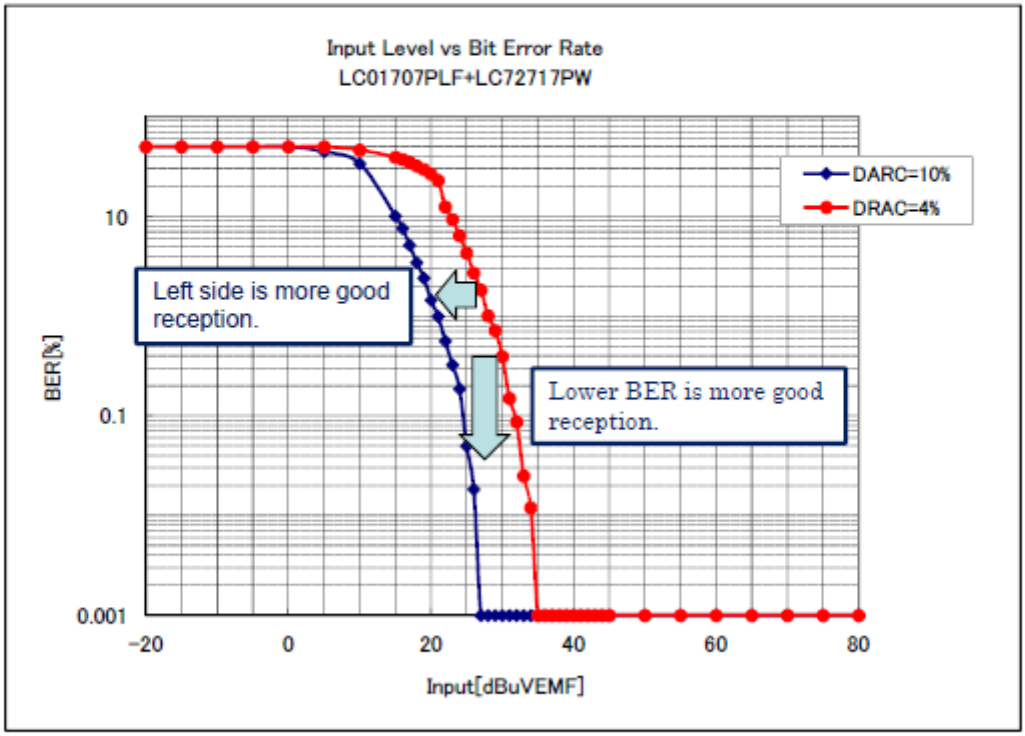


(*)DARC encoder(VP-7663A) is no longer in production.

Reference data

FM Tuner LSI used LC01707PLF.
The bit error rate of LC72717PW is as shown below.

Condition:
(1)DARC=10%
VDD=3.3V、fc=83.0MHz、Modulation＝75kHz、L=R:80%、Pilot=10%、Tone=1KHz
(2)DARC=4%
VDD=3.3V、fc=83.0MHz、Modulation＝75kHz、L=R:2.0%、Pilot=10%、Tone=1KHz



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An INT signal is outputted when the DARC signal is properly inputted into LC72 717PW.

Each output signal is explained below.

FCK:Frame start signal output BCK:Block start signal output

INT:Interrupt output for external microcomputer

In the evalution board, this INT signal is output only when the output data concerned meets all of three conditions as follows:

(1)Data whose error correction is completed and for which layer 2 CRC detects no error (2)Data received during block and frame synchronizations (3)Data in the data packet

When an INT signal is outputted, the data after an error correction can be read by using a microcomputer.

For details, please check by a data sheet.