ON Semiconductor®

Test Procedure for the LC72725KVSGEVB Evaluation Board

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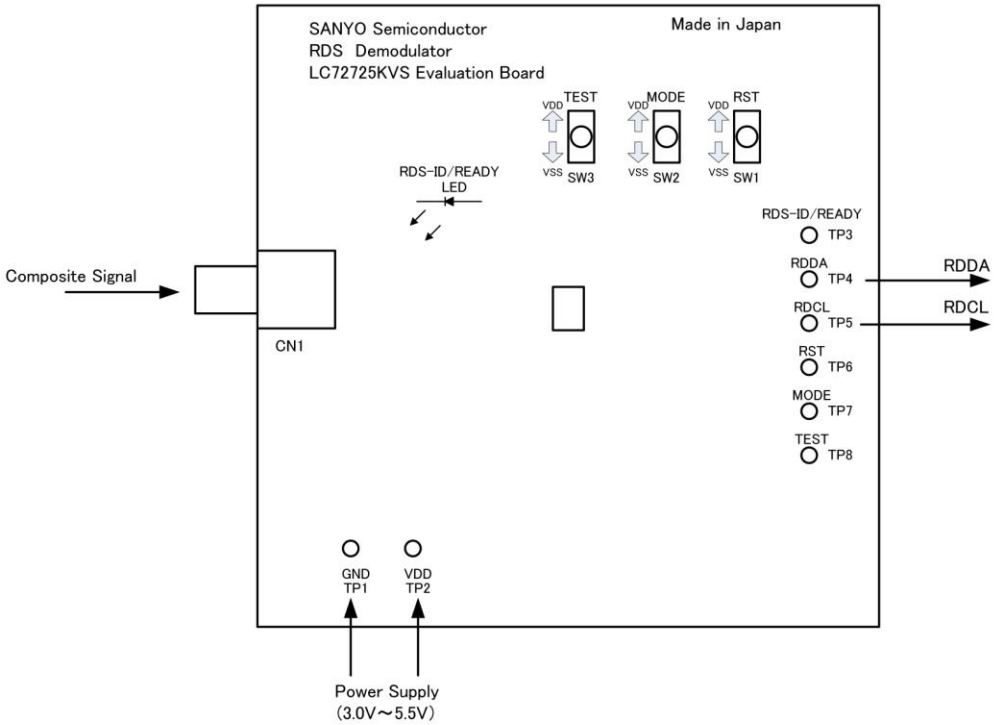
Fig.1 Illustration of LC72725KVS evaluation board



How to use:

1. Connect the power supply to VDD (TP2) and GND (TP1).
   (+3.3V to +5.5V)

2. Input composite signals to the BNC connector (CN1).

3. Toggle SW1 (RST) and SW2 (MODE) and SW3 (TEST) to “VSS” side.

4. If the LC72725KVS detects RDS signal in composite signal, RDS-ID output level turns "H". And the LED lights up.

5. Connect RDCL and RDDA with RDS encoder (as shown in Fig.2) to measure error rate.

Appendix

Description of SW1 and SW2 and SW3:

(1)SW3 (TEST)

SW3=VDD: Standby mode is on when MODE (SW2) is switched to "VSS" side (Crystal circuit is stopped.).

SW3=VDD: LSI test mode is on when MODE (SW2) is switched to "VDD" side.

(Basically, customer cannot switch SW2 to VDD side.)

SW3=VSS: Once RDS signal is received, the signal is output from RDCL and RDDA, respectively.

(2)SW2 (MODE)

SW2=VDD: Slave mode is on when TEST is switched to "VSS" side. RDS clock must be input to RDCL externally. RDS-ID/READY is set to READY output port.

SW2=VSS: Once the RDS signal is received, the signal is output from RDCL and RDDA, respectively.

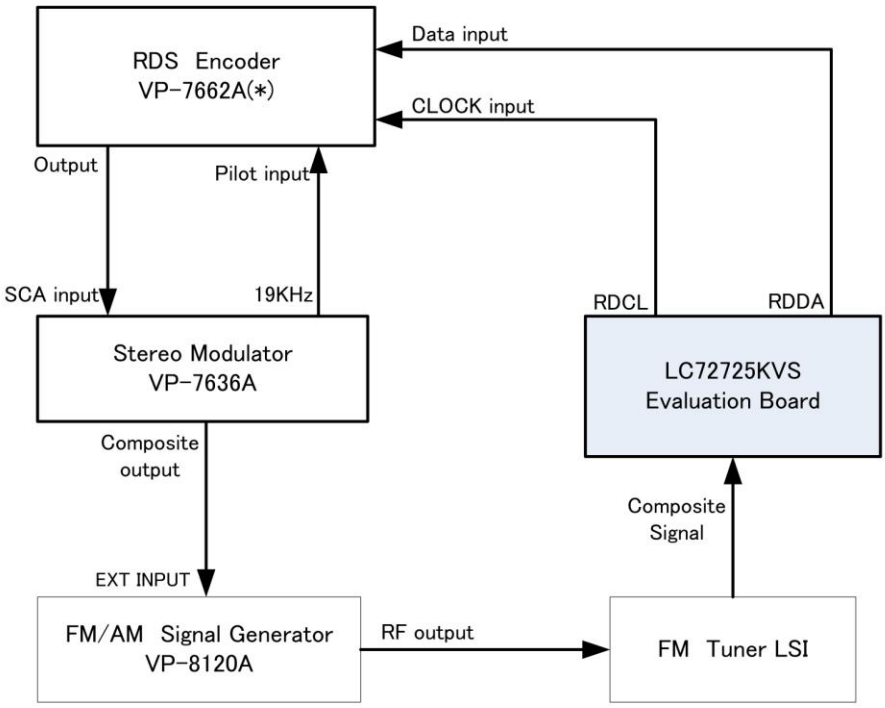
(3)SW1 (RST)

SW1=VDD: RDS-ID and internal buffer are reset. Once the RDS signal is received, the signal is output from RDCL and RDDA.

→ The internal circuit is reset.

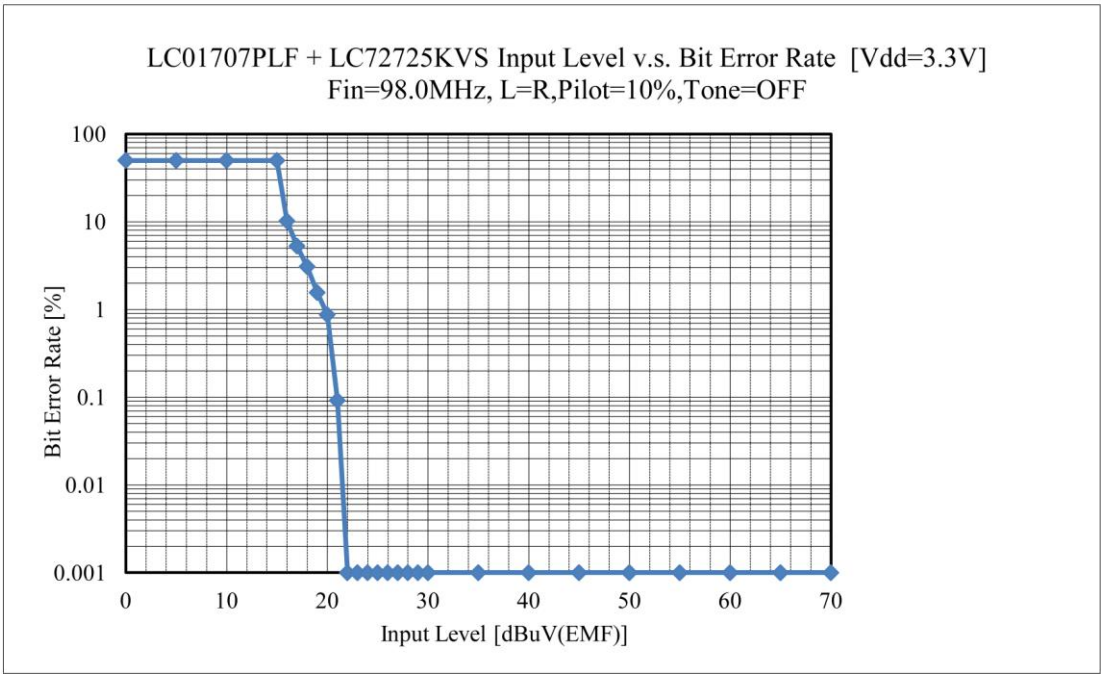
SW1=VSS: Once the RDS signal is received, the signal is output from RDCL and RDDA.

Fig.2 Bit error rate measurement



(*) RDS encoder(VP-7662A) no longer in production. An equivalent model is MEGURO MSG-2174.

Reference data

FM Tuner LSI used LC01707PLF.

The bit error rate of LC72725KVS is as shown below.