

# MC100LVEL33

## 3.3 V ECL ÷4 Divider

### Description

The MC100LVEL33 is an integrated ÷4 divider. The LVEL is functionally equivalent to the EL33 and works from a 3.3 V supply.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple LVEL33's in a system.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

### Features

- 630 ps Typical Propagation Delay
- 4.0 GHz Typical Maximum Frequency
- ESD Protection:
  - ◆ > 4 KV Human Body Model
  - ◆ > 200 V Machine Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 3.0$  V to 3.8 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to  $-3.8$  V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity:
  - ◆ Level 1 for SOIC-8
  - ◆ Level 3 for TSSOP-8
  - ◆ For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 130 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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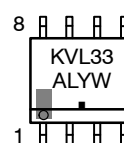


**SOIC-8 NB**  
**D SUFFIX**  
**CASE 751-07**

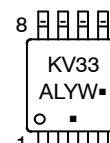


**TSSOP-8**  
**DT SUFFIX**  
**CASE 948R-02**

### MARKING DIAGRAMS\*



**SOIC-8**



**TSSOP-8**

A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
M = Date Code  
■ = Pb-Free Package

(Note: Microdot may be in either location)

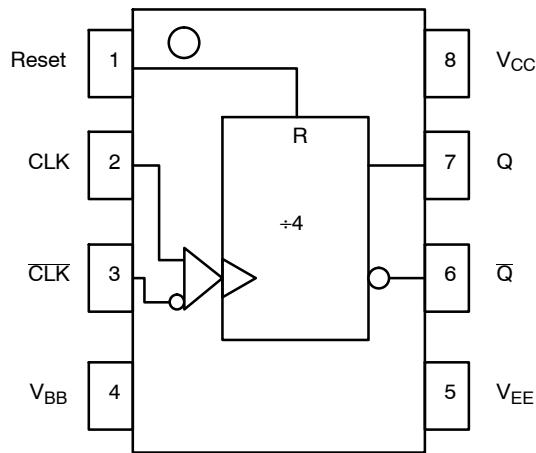
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

| Device           | Package                | Shipping†        |
|------------------|------------------------|------------------|
| MC100LVEL33DG    | SOIC-8 NB<br>(Pb-Free) | 98 Units / Tube  |
| MC100LVEL33DR2G  | SOIC-8 NB<br>(Pb-Free) | 2500 Tape & Reel |
| MC100LVEL33DTG   | TSSOP-8<br>(Pb-Free)   | 100 Units / Tube |
| MC100LVEL33DTR2G | TSSOP-8<br>(Pb-Free)   | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC100LEVEL33



**Table 1. PIN DESCRIPTION**

| PIN                                | FUNCTION                               |
|------------------------------------|--|
| CLK*, $\overline{\text{CLK}}^{**}$ | ECL Differential Clock Inputs          |
| Q, $\overline{\text{Q}}$           | ECL Differential Data $\div 4$ Outputs |
| Reset*                             | ECL Asynch Reset                       |
| V <sub>BB</sub>                    | Reference Voltage Output               |
| V <sub>CC</sub>                    | Positive Supply                        |
| V <sub>EE</sub>                    | Negative Supply                        |

\* Pins will default LOW when open due to internal 75 k $\Omega$  resistor to V<sub>EE</sub>

\*\* Pins will default to 1/2 V<sub>CC</sub> when open due to internal resistors: 75 k $\Omega$  to V<sub>EE</sub> and 75 k $\Omega$  to V<sub>CC</sub>

**Figure 1. Logic Diagram and Pinout Assignment**

**Table 2. MAXIMUM RATINGS**

| Symbol           | Parameter  | Condition 1                                    | Condition 2  | Rating             | Unit                        |
|------------------|--|--|--|--------------------|-----------------------------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |  | 8 to 0             | V                           |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |  | -8 to 0            | V                           |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> $\leq$ V <sub>CC</sub><br>V <sub>I</sub> $\geq$ V <sub>EE</sub> | 6 to 0<br>-6 to 0  | V                           |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |  | 50<br>100          | mA                          |
| I <sub>BB</sub>  | V <sub>BB</sub> Sink/Source                        |  |  | $\pm 0.5$          | mA                          |
| T <sub>A</sub>   | Operating Temperature Range                        |  |  | -40 to +85         | $^{\circ}\text{C}$          |
| T <sub>stg</sub> | Storage Temperature Range                          |  |  | -65 to +150        | $^{\circ}\text{C}$          |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | SOIC-8 NB<br>SOIC-8 NB   | 190<br>130         | $^{\circ}\text{C}/\text{W}$ |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | SOIC-8 NB  | 41 to 44 $\pm 5\%$ | $^{\circ}\text{C}/\text{W}$ |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | TSSOP-8<br>TSSOP-8   | 185<br>140         | $^{\circ}\text{C}/\text{W}$ |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | TSSOP-8  | 41 to 44 $\pm 5\%$ | $^{\circ}\text{C}/\text{W}$ |
| T <sub>sol</sub> | Wave Solder (Pb-Free)                              | < 2 to 3 sec @ 260 $^{\circ}\text{C}$          |  | 265                | $^{\circ}\text{C}$          |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# MC100LEVEL33

**Table 3. LVPECL DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1))

| Symbol      | Characteristic  | -40°C       |      |            | 25°C        |      |            | 85°C        |      |            | Unit          |
|-------------|---|-------------|------|------------|-------------|------|------------|-------------|------|------------|---------------|
|             |   | Min         | Typ  | Max        | Min         | Typ  | Max        | Min         | Typ  | Max        |               |
| $I_{EE}$    | Power Supply Current  |             | 33   | 37         |             | 33   | 37         |             | 35   | 39         | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)  | 2215        | 2295 | 2420       | 2275        | 2345 | 2420       | 2275        | 2345 | 2420       | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)-  | 1470        | 1605 | 1745       | 1490        | 1595 | 1680       | 1490        | 1595 | 1680       | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | 2135        |      | 2420       | 2135        |      | 2420       | 2135        |      | 2420       | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | 1490        |      | 1825       | 1490        |      | 1825       | 1490        |      | 1825       | mV            |
| $V_{BB}$    | Output Voltage Reference  | 1.92        |      | 2.04       | 1.92        |      | 2.04       | 1.92        |      | 2.04       | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3)<br>$V_{PP} < 500\text{ mV}$<br>$V_{PP} \geq 500\text{ mV}$ | 1.2<br>1.4  |      | 2.9<br>2.9 | 1.1<br>1.3  |      | 2.9<br>2.9 | 1.1<br>1.3  |      | 2.9<br>2.9 | V             |
| $I_{IH}$    | Input HIGH Current  |             |      | 150        |             |      | 150        |             |      | 150        | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current<br>Other<br>CLK   | 0.5<br>-600 |      |            | 0.5<br>-600 |      |            | 0.5<br>-600 |      |            | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and  $1\text{ V}$ .

**Table 4. LVNECL DC CHARACTERISTICS** ( $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

| Symbol      | Characteristic  | -40°C        |       |              | 25°C         |       |              | 85°C         |       |              | Unit          |
|-------------|---|--------------|-------|--------------|--------------|-------|--------------|--------------|-------|--------------|---------------|
|             |   | Min          | Typ   | Max          | Min          | Typ   | Max          | Min          | Typ   | Max          |               |
| $I_{EE}$    | Power Supply Current  |              | 33    | 37           |              | 33    | 37           |              | 35    | 39           | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)  | -1085        | -1005 | -880         | -1025        | -955  | -880         | -1025        | -955  | -880         | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)   | -1830        | -1695 | -1555        | -1810        | -1705 | -1620        | -1810        | -1705 | -1620        | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | -1165        |       | -880         | -1165        |       | -880         | -1165        |       | -880         | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | -1810        |       | -1475        | -1810        |       | -1475        | -1810        |       | -1475        | mV            |
| $V_{BB}$    | Output Voltage Reference  | -1.38        |       | -1.26        | -1.38        |       | -1.26        | -1.38        |       | -1.26        | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3)<br>$V_{PP} < 500\text{ mV}$<br>$V_{PP} \geq 500\text{ mV}$ | -2.1<br>-1.9 |       | -0.4<br>-0.4 | -2.2<br>-2.0 |       | -0.4<br>-0.4 | -2.2<br>-2.0 |       | -0.4<br>-0.4 | V             |
| $I_{IH}$    | Input HIGH Current  |              |       | 150          |              |       | 150          |              |       | 150          | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current<br>Other<br>CLK   | 0.5<br>-600  |       |              | 0.5<br>-600  |       |              | 0.5<br>-600  |       |              | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and  $1\text{ V}$ .

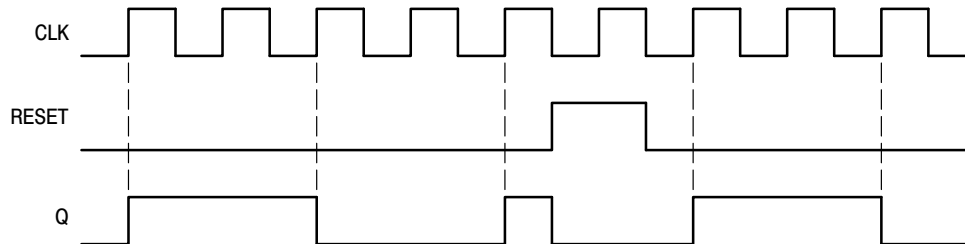
# MC100LEVEL33

**Table 5. AC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

| Symbol                 | Characteristic  | -40°C             |            |                   | 25°C              |            |                   | 85°C              |            |                   | Unit |
|------------------------|---|-------------------|------------|-------------------|-------------------|------------|-------------------|-------------------|------------|-------------------|------|
|                        |   | Min               | Typ        | Max               | Min               | Typ        | Max               | Min               | Typ        | Max               |      |
| $f_{\max}$             | Maximum Toggle Frequency  | 3.4               |            |                   | 3.8               | 4.0        |                   | 3.8               |            |                   | GHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CLK to Q (Diff)<br>CLK to Q (SE)<br>Reset to Q | 530<br>530<br>500 | 630<br>655 | 730<br>780<br>700 | 570<br>570<br>520 | 670<br>695 | 770<br>820<br>720 | 650<br>650<br>580 | 750<br>775 | 850<br>900<br>780 | ps   |
| $t_{RR}$               | Reset Recovery  | 300               |            |                   | 300               |            |                   | 300               |            |                   | ps   |
| $t_{\text{skew}}$      | Duty Cycle Skew (Note 2)  |                   |            | 20                |                   |            | 20                |                   |            | 20                | ps   |
| $t_{\text{JITTER}}$    | Cycle-to-Cycle Jitter   |                   | 0.5        | < 1.0             |                   | 0.5        | < 1.0             |                   | 0.5        | < 1.0             | ps   |
| $V_{PP}$               | Input Voltage Swing<br>(Differential Configuration)                 | 150               |            | 1000              | 150               |            | 1000              | 150               |            | 1000              | mV   |
| $t_r$<br>$t_f$         | Output Rise / Fall Times Q (20%–80%)                                | 120               |            | 320               | 120               |            | 320               | 120               |            | 320               | ps   |

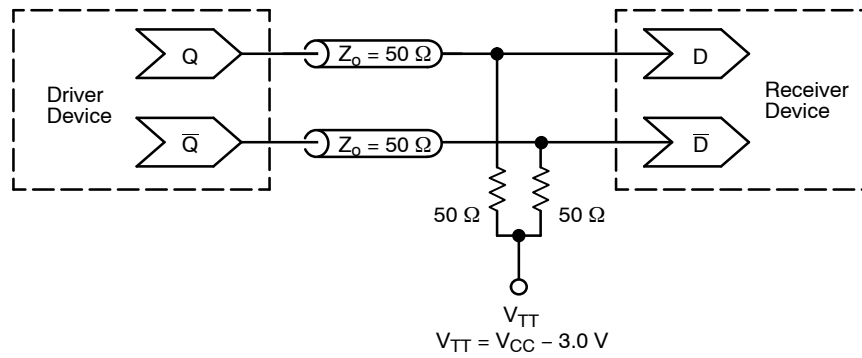
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Duty cycle skew is the difference between  $T_{PLH}$  and  $T_{PHL}$ .



**Figure 1. Timing Diagram**

## MC100LVEL33



**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

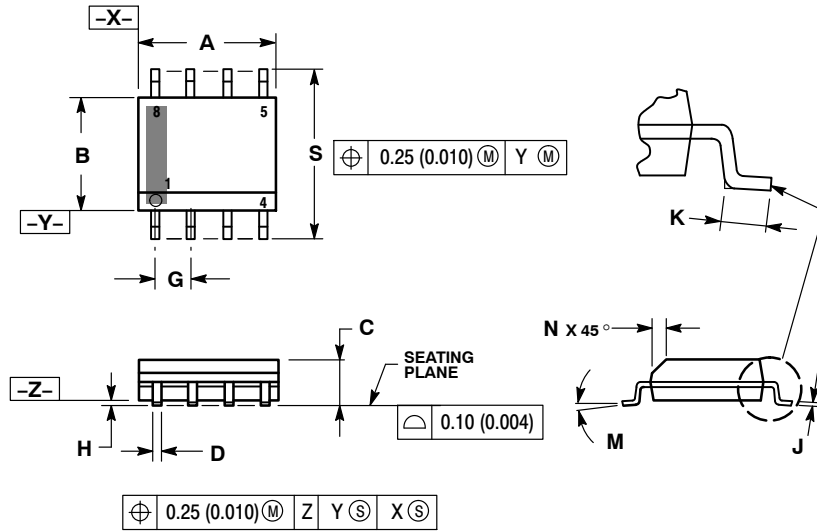
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC100LVEL33

## PACKAGE DIMENSIONS

SOIC-8 NB  
D SUFFIX  
CASE 751-07  
ISSUE AK

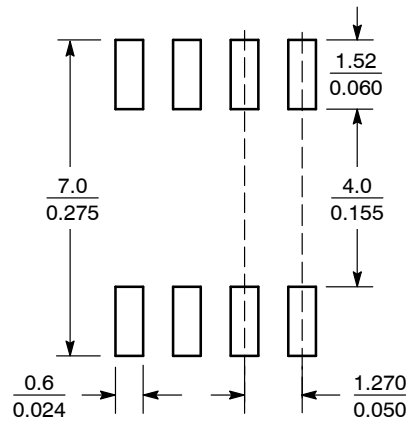


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*



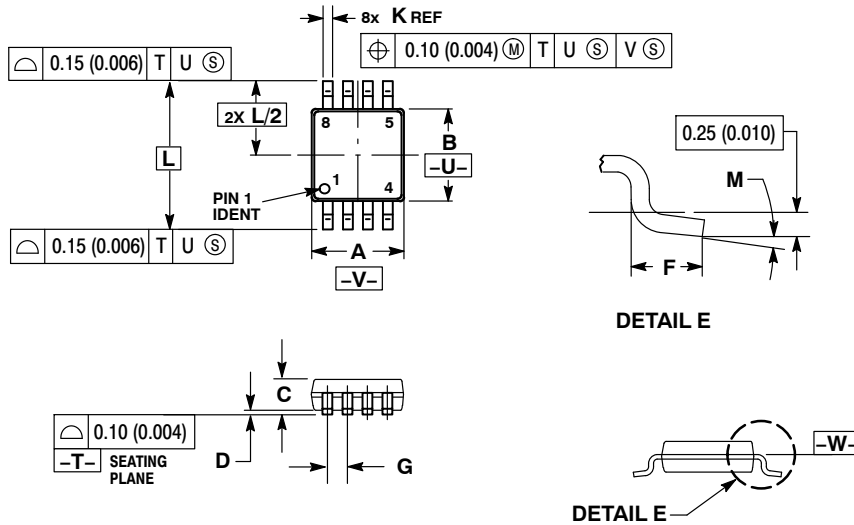
SCALE 6:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC100LVEL33

## PACKAGE DIMENSIONS


TSSOP-8  
DT SUFFIX  
CASE 948R-02  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |

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